# A Bus Encoding Method for Crosstalk and Power Reduction in *RC* Coupled VLSI Interconnects

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### *ABSTRACT*

*The performance factors such as propagation delay, power dissipation and crosstalk in RC modelled interconnects are major design issues for the System on-chip (SoC) designs in current Deep Submicron (DSM) era. The crosstalk effect is a consequence of coupling and switching activities that is encountered when there is a transition as compared to previous state of wire and or when there are transitions in adjacent wires. Therefore, minimization or elimination of switching and coupling activities is crucial in enhancing the performance of SoC designs. There are several methods for the reduction of power dissipation, crosstalk and delay. The encoding method is most effective and popular method for enhancing the behaviour of on-chip buses. This paper proposes encoding scheme to achieve overall reduction in transitions. The reduction in transition improves the performance in terms of reduced power dissipation, coupling activity and delay in on-chip buses. This encoding method is implemented using VHDL. The result evidently demonstrates reduction in transitions which consequently improves the overall performance of on-chip buses.*

### *Keywords*

*Coupling, VLSI, SoC, Bus Encoding, Interconnects*

## 1. INTRODUCTION

The feature size of integrated circuits has been consistently reduced in the pursuit of improved speed, power, silicon area and cost characteristics. Semiconductor technologies with feature sizes of several tens of nanometres are currently in development. As per International Technology Roadmap for Semiconductors (ITRS), the future nanometre scale circuits will contain more than a billion transistors and operate at clock speeds well over 10GHz. Distribution of robust and reliable power and ground lines; clock; data and address; and other control signals through interconnects in such a high-speed, highly-complex environment, is a challenging task. The function of wiring systems or interconnects is to distribute clock and other signals and to provide power/ground to and among the various circuits/systems functions on the chip. The performance parameters i.e. time delay and power dissipation of a high-speed chip is highly dependent on interconnects, which connect different macro cells within a VLSI chip.

DOI : 10.5121/vlsic.2012.3203

In current DSM (Deep Submicron) technology, coupling and self capacitance plays an important role for deciding the behaviour of on-chip interconnects. Due to the coupling and self capacitance, crosstalk, delay and power consumption problems will arise. The above problems are highly dependent on the frequency of signal used, length of interconnects, data signal etc. Interconnects can be modelled as $RC$ or $RLC$ transmission line. The effect of inductance plays an important role as the length and used frequency signal increases. [1-4, 8-16] This paper considers $RC$ network for the implementation and study of the behaviour of interconnects due to coupling capacitance.

The components that affect the behavior of the on-chip bus are internal parasitic capacitances of the transistors, interconnect capacitances and input capacitances of the fan-out gates.

The most common methods to reduce crosstalk, propagation delay and power are:

- Insertion of repeaters
- Insertion of shielding between adjacent wires
- Minimizing spacing between signal and ground lines.
- Isolating clocks and other critical signals from other lines (larger line spacing) or isolation with ground traces.
- In backplane or wire-wrap applications, use twisted pair for sensitive applications such as clocks and asynchronous set or clear functions. While using ribbon or flat cable, make every other line a ground line.
- Introduction of intentional delay among coupled signal transmission.
- Bus Encoding methods
- The use of tight geometry in most systems can reduce crosstalk significantly although it cannot eliminate it entirely. Some preventive design measures can be used to minimize crosstalk.
- Using maximum allowable spacing between signal lines.
- Terminating signal lines into their characteristic impedance.

The Bus encoding method is widely used technique to reduce dynamic switching power and the effects of crosstalk (signal noise, delay) during data transmission on buses [15]. Low power encoding techniques aim to transform the data being transmitted on buses in such a manner so that the self and coupling switching activity on buses are reduced. Crosstalk aware encoding techniques can also modify the switching patterns of a group of wires to reduce crosstalk coupling effect. These techniques are quite effective in reducing power consumption, improving transmission reliability, and increasing system performance. For any encoding scheme, the encoder and decoder functions are the inverse of each other. Bus encoding schemes can be classified according to several criteria, such as the amount of extra information needed for coding (redundant or irredundant coding), and the method of encoding implementation (hardware, software, or a combination of the two), Type of code used (algebraic, permutation, or probability based), the degree of encoding adaptability (static or dynamically adaptable encoding), the targeted capacitance for switching reduction (self, coupling or both). Encoding techniques are often aimed at power reduction, signal transmission delay reduction and reliability improvement, or a combination of these due to the reduction in the transition. Certain optimizations such as crosstalk reduction can have multiple benefits associated with them such as power reduction, signal delay reduction and noise reduction.

This paper presents an encoding method for the reduction of coupling transitions. The crosstalk is classified into different types [1, 2, 15, 16] depending upon the transitions of the signal in the wire. The proposed encoding scheme also reduces data lines hence, reduces the redundancy and power consumption. It also considers the worst case crosstalk effects due to transitions in the group of lines.

## 2. Estimation of Power and Crosstalk in *RC* Bus Model

The total power consumption in the VLSI chip comprises of dynamic power, short circuit power, static power and leakage power. It can be simply described as summation of all these components i.e.

$$P_{Dissipation} = P_{Static} + P_{Dynamic} + P_{Leakage} + P_{Shortckt} \qquad (1)$$

The capacitance of interconnect can be classified as coupling capacitance and self-capacitance. The coupling capacitance is the capacitance between the adjacent data lines while the self-capacitance refers to the capacitance between the substrate and the wire itself. The dynamic power in VLSI chip decides the behaviour of chip and is highly dependent on the load capacitance and coupling capacitance i.e. bus line signal transitions. Dynamic power dissipation on a coded bus thus can be defined as following equation

$$\begin{aligned} P_{D,Coded} &= (\alpha_{cl} \times C_L + \alpha_{cc} \times C_C) \times {V_{DD}}^2 \times f \\ &= (\alpha_{cl} + \alpha_{cc} \times \lambda) \times C_L \times {V_{DD}}^2 \times f) \qquad (2) \end{aligned}$$

where, $C_L$, $C_c$, $V_{DD}$, $f$ and $\lambda$ is the load capacitance, coupling capacitance, supplying voltage, clock frequency and capacitance ratio defined as: $\lambda = C_c/C_L$ respectively. $\lambda$ is dependent on the technology which is being used, hence its value depends on the physical parameters. $\alpha_{cl}$ is the value of average switching activity for the load capacitance. For un-encoded buses $\alpha_{cl}$ is 1. $\alpha_{cc}$ is the value of average coupling activity for the coupling capacitance. For un-encoded buses $\alpha_{cc}$ is 1. Hence for un-encoded data the power dissipation can be defined by following equation

$$P_{D,un-coded} = (1 + \lambda) \times C_L \times {V_{DD}}^2 \times f \qquad (3)$$

Effective crosstalk capacitance is determined by

$$C_{eff} = C_c \times \frac{\Delta V_2 - \Delta V_1}{V_{DD}} + C_C \times \frac{\Delta V_2 - \Delta V_3}{V_{DD}} \qquad (4)$$

where, $\Delta V_2$ is voltage variation of the centre wire. $\Delta V_1$ and $\Delta V_3$ are voltage variations in the adjacent wires. $V_{DD}$ is power supply voltage which equals rail-to-rail signal voltage in CMOS circuits. $C_{eff}$ is effective coupling capacitance variation [1, 2].

The coupling between the groups of the three wires is classified into five types depending upon the nature of transitions of signals in the wire that are Type-0, Type-1, Type-2, Type-3 and Type-4. The Type-0 coupling occurs when all of the 3-bit wires are in the same state transition. A transition from 000 to 111 (i.e. ↑↑↑) causes a Type-0 coupling. For Type-0, coupling capacitance is zero. Type-1 coupling occurs when there is a transition in one or the two wires (including the centre wire) and the third wire remains quite. There are eight possibilities by which Type-1 condition occurs. The coupling capacitance in this case is $C_C$. A Type-2 coupling occurs when the centre wire is in the opposite state transition with one of its adjacent wires while the other wires undergo the same state transition as the centre wire i.e.100 to 011. Ten different conditions are possible for Type-2 coupling. The coupling capacitance is $2C_C$ in this case. A Type-3 coupling occurs when the central wire undergoes the opposite state transition with one of the two wires while the other wires are quiet i.e. 010 to 001. Coupling capacitance in the case of Type-3 coupling is $3C_C$ and there are four possibilities that cause Type-3 coupling. For a Type-4 coupling, all three wire transitions are in the opposite states with respect to each other. Two conditions cause Type-4 coupling with a coupling capacitance effect of $4C_C$. All the five Types of couplings are shown in Table-1 [2].

**Table.1.** Crosstalk Types for a 3-Bit Bus Considering *RC* Model of Interconnect [2].

| Type-0 | Type-1 | Type-2 | Type-3 | Type-4 |
|---|---|---|---|---|
| −−− | −−↑ | −↑− | −↑↓ | ↑↓↑ |
| ↓↓↓ | −↑↑ | ↑−↑ | −↓↑ | ↓↑↓ |
| ↑↑↑ | ↑−− | ↑−↓ | ↑↓− | |
| | ↑↑− | ↑↑↓ | ↓↑− | |
| | −−↓ | ↑↓↓ | | |
| | −↓↓ | −↓− | | |
| | ↓−− | ↓−↓ | | |
| | ↓↓− | ↓−↑ | | |
| | | ↓↓↑ | | |
| | | ↓↑↑ | | |

*↑: switch from “0” to “1”, ↓: switch from “1” to “0”, -   : no transition*

It can be concluded from the above description that power and crosstalk is highly dependend on the transitions of the signal in the wires. If the number of transitions is reduced by encoding methods, the dynamic power dissipation as well as crosstalk will also be reduced. Different encoding methods are proposed by different researchers. The efficient encoding proposed by *Burleson et al.* [3], which include the concept of counting the number of transitions, with respect to the previous states of group of lines. Data is transmitted in original form or in inverted form depending on the number of state transition of the lines as compared to previous states.

## 3. Encoding Method

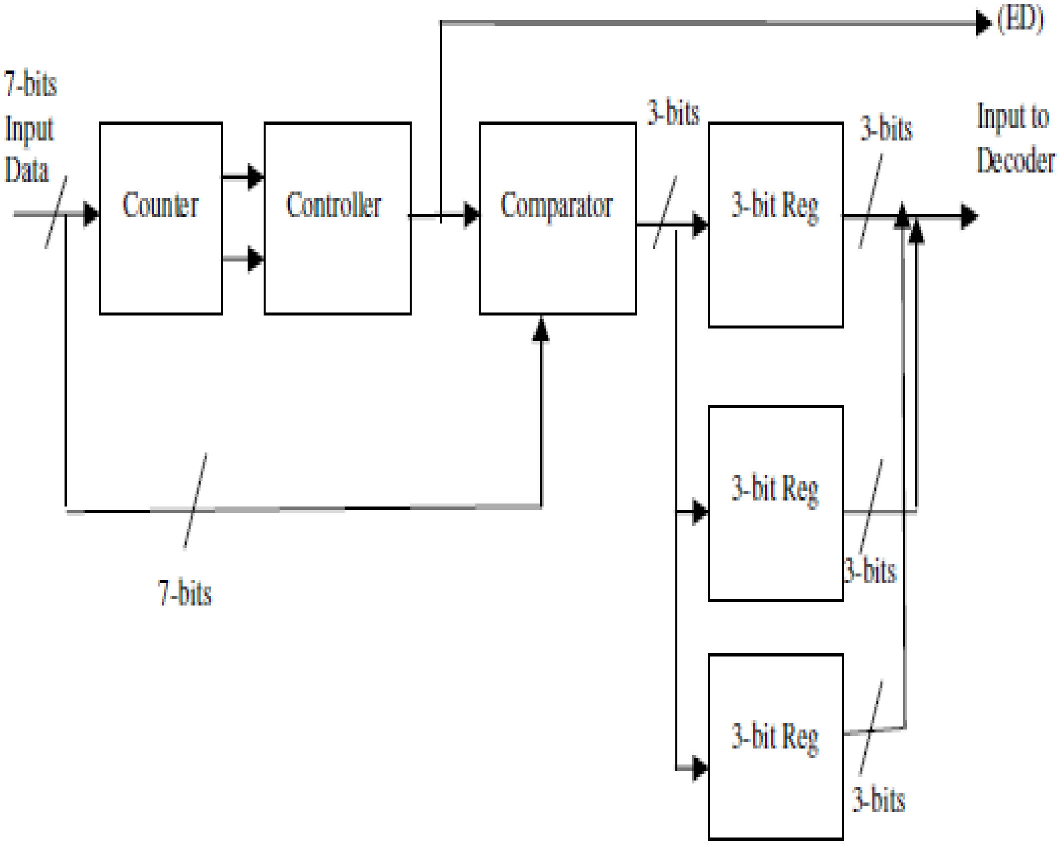

**Fig. 1.** Block Diagram of Encoding Method

The block diagram of proposed encoder is shown in Fig.1 that consists of counter, controller, comparator and three 3-bit register. Each module of the encoding method is explained in later sections. The encoder transforms the bus line signals for the reduction or elimination of the worst case crosstalk by reducing the 7-bit lines into 4-bit lines. The encoder deals with the coupling transitions among the group of seven bits. It identifies the higher number of 0's and 1's in counter and controller modules. Output line of controller is set according to higher number of 1's or 0's. The comparator module compares the input 7-bit data lines with the output line of the controller to identify the flips in the line.

Firstly, the number of 1's and 0's are counted using a counter module. If the number of 1's is more than the number of 0's, the comparator module sets output line in high state i.e. 1. If the number of 0's are more than the number of 1's, the comparator module sets output line in low state i.e. 0. There are two best cases possible; either all lines are in one state or all lines are in zero state. Maximum three flips are possible in comparator module due to the counter and controller modules. These flip positions are stored in three 3-bit registers.

The single output line of controller is compared with initial 7-bit input line and finds the flipped bit positions. The number of flipped bits could be 0 i.e. best case when all the inputs are either '0' or '1', or 1 or 2 or 3 i.e. worst case. After identification of the flipped bits positions, these positions are stored in the 3-bit registers. The number of the registers is chosen to be three in order to work for the best as well as the worst cases. The best case is one when all the input lines are '0' or '1'. In this case all the registers are empty as there is no change in any of the bits. Thus, there is significant reduction in crosstalk as all three registers have same null value. Otherwise, the value of the registers can vary from zero to maximum three. The seven bits data lines are taken as inputs to the encoder, so, three bits have taken to indicate the flip bit positions in the seven lines. All the equivalent positions for these 8 combinations are shown in Table.2**.** Each of the register value sends in three different clock cycles. At each clock cycle, contents of one register are sent to the decoder. Next register contents are sent in the next clock cycle and so on. Since the maximum flips that can be possible are three so maximum three clock cycles are required for decoding the 7-bit line at decoder side.

**Table 2.** Register Values Indicating the Positions of Flipping

| Register Value | Flipped I/P Line Position |
|---|---|
| 000 | 0 |
| 001 | 1 |
| 010 | 2 |
| 011 | 3 |
| 100 | 4 |
| 101 | 5 |
| 110 | 6 |
| 111 | 7 |

## 3.1 Counter Module

The counter module is for the determination of the number of 0's and 1's in the input sequence of seven bit lines. The input to the counter module is 7-bit input. Each of these lines is selected and then compared with '0' and '1'. Two variables are initialized for storing the values of the number of 0's and 1's in the input sequence. The first variable stores the value of the number of 0's and the other one store the number of the 1's in the input sequence. These two lines are then fed into the controller module along with two variables and are passed to the controller.

## 3.2 Controller

As seen in Fig.1 the two output lines of the counter represents the number of 1's and 0's. These two inputs are fed to the controller. The Controller decides for the number of occurrences of 0's and 1's as provided by counter module. This module decides the output as '0' or '1' based on the input value. If number of 0's is higher as compared to the number of 1's the output of the controller will be '0'. If number of 1's is higher as compared to the number of 0's the output of the controller will be '1'.

### 3.3 Comparator

The single output line is fed to the comparator along with the initial 7-bit inputs. This single output line is compared with each of the initial 7-bits. This is to compare whether the value of the bit is the same or different from the single line. The output signal from the controller is XORed with each of the seven input lines to identify the flipping. This module identifies the flipped positions and stored in the 3-bit register for the decoding purpose.

### 3.4 Registers

This module is used for storing the position of flipped bit identified by the comparator module. This ascertains the proper interpretation of the input bits where a 000 value in the register stands for the $0^{th}$ bit position, 001 represents the 1st bit and likewise 111 represents $7^{th}$ position as shown in the Table.2. These three registers are meant for the simultaneous storage of the flipped bit positions. These lines along with the single input equivalent line from the controller are transmitted to the decoder. The encoder provides the output in four lines for the decoding purpose i.e. one line from the controller and the other three lines from the register. Three clock cycles are needed for complete decoding of the input sequence.

## 4. Decoder

The decoder of the proposed encoding method is shown in Fig.2. The decoder of the proposed encoding method consists of the three 3-bit registers, splitter, inversion module and line identifier. The four lines from the encoder are fed to the decoder. In the first clock cycle the contents of the first register from encoder are stored in the first register of the decoder and so on. As we know the maximum flips that can be possible are three, so maximum three clock cycles are required for complete decoding of the 7-bit data. Although, we can also use single 3-bit register in the encoder and decoder side instead of three 3-bit registers, three registers are used for the compensation of delay generated by the clock cycles for the transmission of flipped bit positions to decoder side.

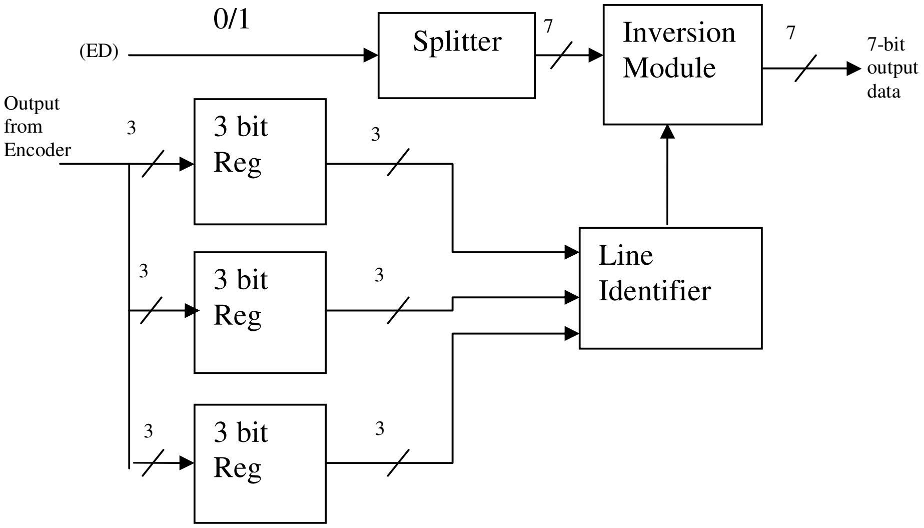

**Fig. 2.** Decoder of Encoding Method

The output line taken from the comparater of encoder side is fed to the spliter module of the decoder. The splitter module splits the 1-bit input line to seven bits of output lines. All the seven output lines have similar value as that of the input i.e. if the input to the spliter is '1' then output of the splitter is of seven lines having value of each line as '1'. Similarily when input of the splitter is '0' all the seven lines will have output value '0'. The line identifier module takes the input from the three 3-bit registers sequentially. The sequence is managed by the clock cycle. Line identifier gets the content of 3-bit register and identifies the line to be flipped as per Table 2. These identification indications are then fed to the inversion module. The inversion module inverts the indentified line. In next turn this process is repeated. And after three iterations the final decoded data of seven bits is taken as the output of the decoder.

## 5. Simulation and Results

Encoder and decoder are implemented in VHDL[5]. The encoder described in the previous sections had a 7-bit input sequence, primarily targetting for reduction in crosstalk and power dissipation. The designed encoder reduces the 7-bit input sequence to a 4-bit output sequence which reduces the redundancy. The number of wires is reduced by 57.14%. Therefore, redundancy is also reduced by 57.14%. However, in other encoding schemes, redundancy increases by 25%. The proposed encoding scheme not only reduced the redundancy but also reduces the power consumption. On implementation of encoding mechanism, it is observed that the crosstalk reduces by 35 to 40%. The encoder is tested on the random 7-bit sequences and it was found that the worst case crosstalk reduced by 40%. This encoding method reduces the power dissipation and crosstalk. Whereas, a three clock delay is introduced. This delay can therefore be allowed as the overall implementation is better than the initial input sequence transmission method. Hence, it is evident that this method is acceptable. This encoder considers only the coupling transitions in the input 7-bit sequence.

## 6. Conclusion

The proposed method of bus encoder significantly eliminates or reduces the worst case crosstalk. Reduction of crosstalk is because of the reduction in the number of lines from 7 bits to 4 bits as an output of the Encoder. This reduces the crosstalk effectively by 35 to 40 percent. The transitions in the state of buses decide the behaviour of the switching and coupling activities. It is shown that reduction in the coupling and switching activity reduces the dynamic power dissipation and crosstalk. Thereby, the power dissipation is also reduced as compared to the initial input sequence. Hence, the overall performance of the VLSI chip is improved. For all possible 128 combinations of the input sequence the output is seen manually and via the implemented mechanism. It is finally found that the method is implemented successfully and serves its purpose to a great extent.

## 7. ACKNOWLEDGEMENTS

Special thanks to Mr. Kanwaljeet Kathait, Ms. Sushila Mishra, and their group members for their valuable efforts and cooperation.

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