CELL STABILITY ANALYSIS OF CONVENTIONAL 6T DYNAMIC 8T SRAM CELL IN 45NM TECHNOLOGY

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ABSTRACT:-

A SRAM cell must meet requirements for operation in submicron/nano ranges. The scaling of CMOS technology has significant impact on SRAM cell -- random fluctuation of electrical characteristics and substantial leakage current. In this paper we present dynamic column based power supply 8T SRAM cell and comparing the proposed SRAM cell with respect to conventional SRAM 6T in various aspects. To verify read stability and write ability analysis we use N-curve metric. Simulation results affirmed that proposed 8T SRAM cell achieved improved read stability, read current, and leakage current in 45nm Technology comparing with conventional 6T SRAM using cadence virtuoso tool.

Key Words:-

SRAM, Leakage Current, N-curve, Read stability, Write-ability, Cadence, Virtuoso, 45nm Technology.

1. INTRODUCTION

For nearly 40 years CMOS devices have been scaled down in order to achieve higher speed, performance and lower power consumption. Static Random Access Memory (SRAM) continues to be one of the most fundamental and vitally important memory technologies today. As process technology is scaled down, threshold voltage and leakage current variations are increased [1]. In the conventional 6T cell, it is difficult to find an optimum design because the both read stability and write margin must be considered. At low supply voltage 6T cell worsen in read stability. Leakage power is a high priority consideration due to feature scaling in high performance processor design. In today's processors, the leakage power of cache was a major source of power dissipation because cache occupies more than 50% of the chip area [2]. Low leakage SRAM design leakage SRAM design has been an active area of research over the past years. Low Power and high-stability have been the main themes of SRAM designs in the last decade [8].

In this paper, we use dynamic cell supply 8T SRAM cell to address the above problems. We compare the conventional 6T and proposed 8T SRAM cell with respect to read stability and leakage.

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The rest of the paper is organized as follows:

Section 2 presents stability analysis using N-curve. Section 3 reviews the basic operation of conventional 6T SRAM cell. Section 4 presents the operating principles of proposed cell and its circuit implementation. Section 5 presents Cadence design flow. Section 6 presents simulation results. Section 7 represent conclusion of the paper.

2. STABILITY ANALYSIS USING N-CURVE

Normally stability of the SRAM bit cell measured by the Static Noise Margin (SNM) and the Write Trip Point (WTP). According to [3], in this paper SRAM bit cells were analyzed using the N-Curve which is the inline tester. N-Curve gets information about both read stability, write stability at one simulation process.

2.1 READ STABILTY

The cell becomes less stable with lower supply voltage, increasing leakage currents and increasing variability, all resulting from technology scaling. The stability is usually defined by the SNM as the maximum value of DC noise voltage that can be tolerated by the SRAM cell without changing the stored bit. Locating the smallest square between the two largest ones delimited by the eyes of the butterfly curve determines graphically the SNM shown in Fig1 [9].

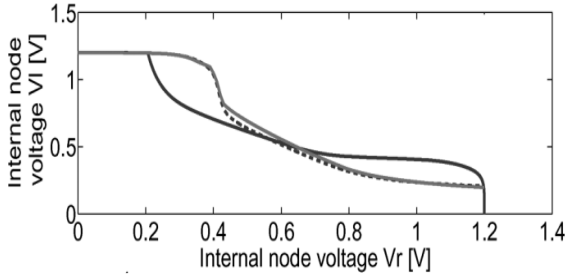

Figure 1: SNM.

The drawback of the SNM is the inability to measure the SNM with automatic inline testers, due to the fact that after measuring the butterfly curves of the cell the static current noise margin (SINM) still has to be derived by mathematical manipulation of the measured data. An alternative definition for the SRAM read stability is based on the N-curve of the cell, which is measurable by inline testers. The combined voltage and current information provided by the N-curve (Fig.2) allows to overcome the limitations of scaling described for the SNM.

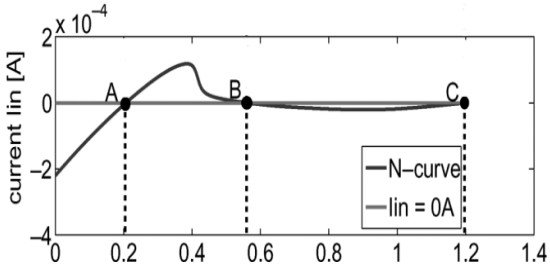

Figure 2: N-curve of the cell.

The voltage difference between point A and B indicates the maximum tolerable DC noise voltage of the cell before its content changes. This voltage metric is the static voltage noise margin (SVNM). The additional current information provided by the N-curve, namely the peak current located between point A and B, can also be used to characterize the cell read stability [3]. This current metric is the static current noise margin (SINM).

For better read stability, SVNM and SINM must be high value.

2.2 WRITE STABILTY

Besides the read stability for the SRAM cell, a reasonable write-trip point is equally important to guarantee the write-ability of the cell without spending too much energy in pulling down the bit-line voltage to 0 V. The SRAM N-curve can also be used as alternative for the write-ability. Since, it gives indications on how difficult or easy it is to write the cell. The negative current peak (Fig 2) between point C and B or the write-trip current (WTI) is the amount of current needed to write the cell when both bit-lines are kept at VDD. Similarly, the voltage difference between point C and B or the write-trip voltage (WTV) is the voltage drop needed to flip the internal node "1" of the cell with both the bit-lines clamped to VDD.

The N-curve current information is critical for designing a cell in nanometer technologies. Moreover, it allows overcoming the read stability limit of 0.5VDD. Finally, to find the stability of the system we should consider the SVNM, SINM, WTV and WTI [3].

3. CONVENTIONAL 6T SRAM CELL

3.1 CONSTRUCTION

Fig 3 shows the conventional 6T SRAM cell which has two back to back connection of inverters using N1, P1, N2, P2 to store the single bit either '0' or '1'. N3, N4 transistors are called as access transistors. WL is used to turn ON the access transistors. BL, /BL are bit lines.

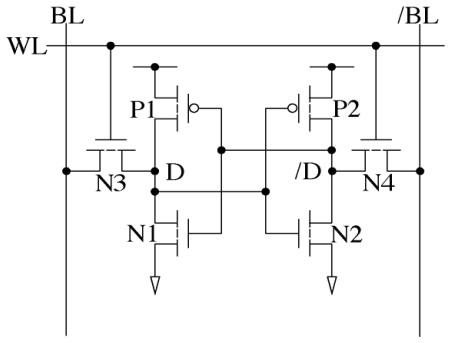

Figure 3. conventional 6T SRAM cell.

3.2 OPERATION

An SRAM cell has three different states it can be in: standby where the circuit is idle, reading when the data has been requested and writing when updating the contents. The SRAM to operate in read mode and write mode should have "readability" and "write stability" respectively. The three different states work as follows [5] [7]:

- **Standby**: If the word line is not asserted, the access transistors N3 and N4 disconnect the cell from the bit lines. The two cross coupled inverters formed by P1-N1, P2-N2 will continue to reinforce each other as long as they are connected to the supply.

- **Reading:** Assume that the content of the memory is a 1, stored at D. The read operation is done by using the sense amplifiers that pull the data and produce the output. The row decoders and column decoders are used to select the appropriate cell or cells from which the data is to be read and are given to the sense amplifiers through transmission gate.

- **Writing:** The start of a write cycle begins by applying the value to be written to the bit lines. If we wish to write a 0, we would apply a 0 to the bit lines, i.e. setting BL bar to 1 and BL to 0. A 1 is written by inverting the values of the bit lines. WL is then asserted and the value that is to be stored is latched in. Note that the reason this works is that the bit line input-drivers are designed to be much stronger than the relatively weak transistors in the cell itself, so that they can easily override the previous state of the cross-coupled inverters.

4. PROPOSED 8T SRAM CELL

4.1 CONSTRUCTION

The proposed SRAM cell consists of 8 transistors, N1-N5 and P1-P3, as shown Fig.4. Four transistors N1, N2, P1, P2 form a cross-couple structure to store data. Four transistors P3 and N3-N5 are access to the internal nodes D and /D of the cell. N3 and N4 connect the cell internal nodes D and /D of the cell. N3 and N4 connect the cell internal nodes to the BLs while P3 and N5 form an inverter to control the voltage of node C1. The source terminal of P3 is connected to a column select (CS) line while gates of P3 and N5 are connected to WL. Unlike conventional design, the sources of P1 and P2 are connected to dynamic cell supply(*cell_supply*) line which is raised to the higher voltage during read operation to obtain a higher noise margin [4].

4.2 OPERATION

Like a conventional 6T SRAM bit cell, it has three modes of operations*: standby, read and write* as follows [4]:

Standby: During standby, *Cell_Supply* voltage is kept at VDD to maintain a high noise margin.at the same time WL is pre-charged high while all CS is pre-charged low. As a result, transistor N5 of cell is turned on to pre-charge node C1 to ground. Thus, both access transistors N3 and N4 turned off, isolating the storing element from any BL disturbances. Also, BLs are pre-charged to VDD to prepare for the next read/write operation.

Reading: read operation starts by raising CS from ground to VDD and *Cell_Supply* is raised from VDD to VDD2. VDD2 must be higher than VDD to improve noise margin of cell during read operation. At the same time WL is pulled to low to drive node C1 to VDD and hence turning on N3 and N4. Once N3 and N4 are turned on to read the cell data, subsequent circuit operation same as the conventional 6T SRAM.

Writing: Write operation of the proposed design is much simpler than its read operation. Write operation starts by asserting CS line to VDD while the WL is pulled down. Meanwhile, one of the BLs is pulled to ground while other kept at VDD. When node C1 is charged up to VDD, both N1 and N2 are turned on and input data is written into memory similar to conventional 6T SRAM.

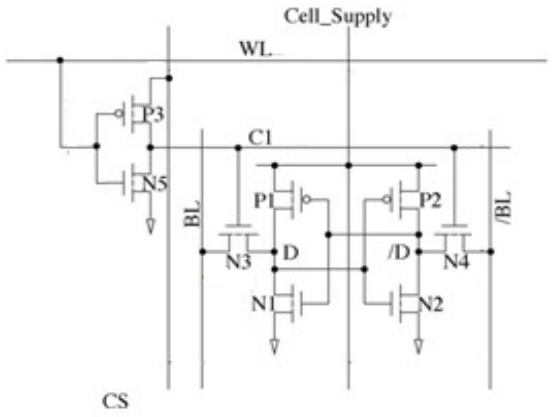

Figure 4. proposed 8T SRAM cell

5. CADENCE DESIGN FLOW

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Cadence design Systems is electronic design automation software and engineering Services Company that offers various types of design and verification tasks that include [6]:

- **Virtuoso Platform** - Tools for designing full-custom integrated circuits, includes schematic entry, behavioral modeling (Verilog-AMS), circuit simulation, full custom layout, physical verification, extraction and back-annotation. Used mainly for analog, mixed-signal, RF, and standard-cell designs.

- **Encounter Platform -** Tools for creation of digital integrated circuits. This includes floor planning, synthesis, test, and place and route. Typically a digital design starts from Verilog netlists.

- **Incisive Platform -** Tools for simulation and functional verification of RTL including Verilog, VHDL and System C based models. Includes formal verification, formal equivalence checking, hardware acceleration, and emulation.

The proposed work is done in Virtuoso platform using gpdk45 nm technology. The flow of design is as shown below.

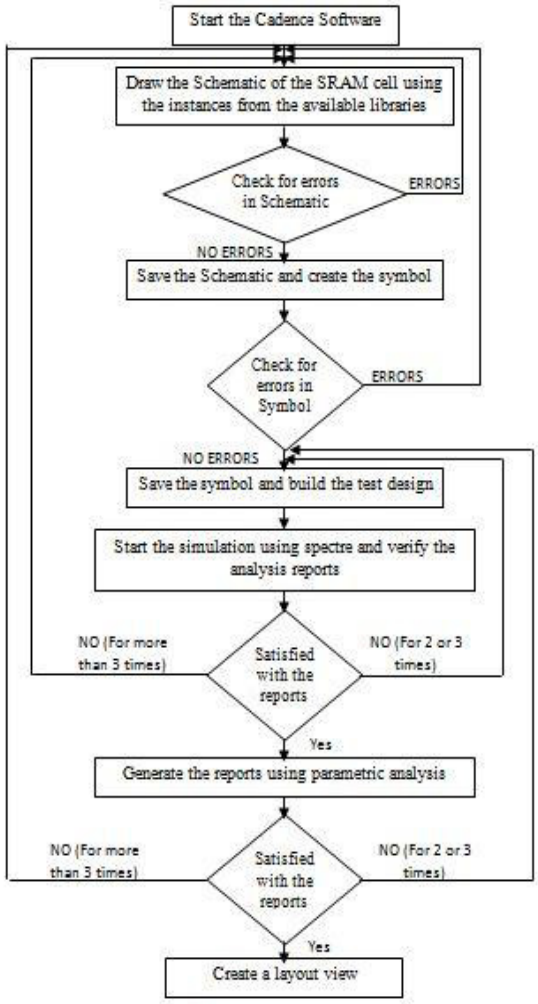

Figure 5. cadence virtuoso design flow.

Using above flow design of both conventional and proposed system in cadence virtuoso schematic tool was done. Fig 6 & Fig 7 shows the schematic for conventional 6T and proposed 8T using cadence virtuoso schematic editor. After that we create symbols for both and analysis those cells in various aspects.

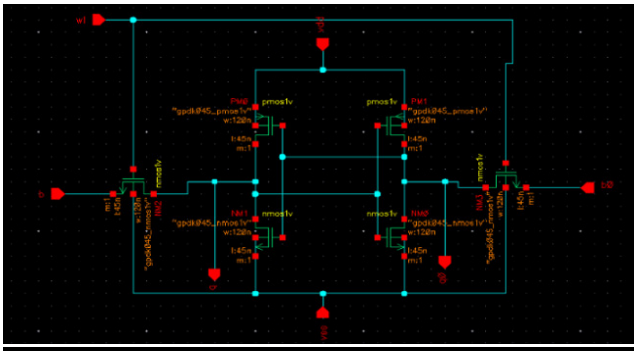

Figure 6. Conventional 6T SRAM cell design in cadence.

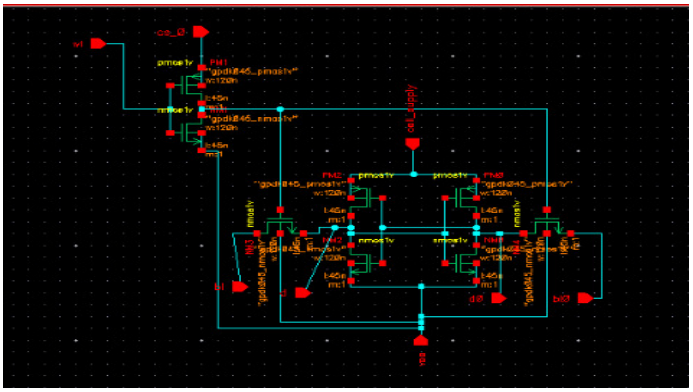

Figure 7. proposed 8T SRAM cell design in cadence.

6. SIMULATION RESULTS

Cadence spectra simulation of DC analysis gave good results in 45nm technology. The results are shown in below Table 1. Below table shows the comparison between conventional 6T, proposed SRAM bit cell using N-curve. Here analysis was done based on DC simulation results by giving inputs as a dc signals to know the stability of the SRAM cell.

	Conventional SRAM 6T	**Proposed SRAM 8T**
CMOS Process	45nm/1V	45nm/1V
Read/write process	Differential	Differential
SVNM	325mV	668.6mV
SINM	35.61 µA	98.16 µA
WTV	475mV	487.8mV
WTI	-10.47µA	-48.35µA
Leakage current	10.026fA	5.21143fA
Read current	5.39421pA	99.5612µA

Table1. Summary of conventional 6T, Dynamic 8T SRAM Cell

SRAM bit cell N-Curve analysis results:

The read stability is analysed with respect to N-curve as shown in fig 8 & fig 9. Procedure to get N-curve is we need to select the dc simulation, after that by taking /D as variable input node from 0 to vdd, D as a output node measure /D node current which is in Y- axis with respect to input voltage would gives Fig.8. By observing Fig 8 measured SVNM,SINM,WTV,WTI values.

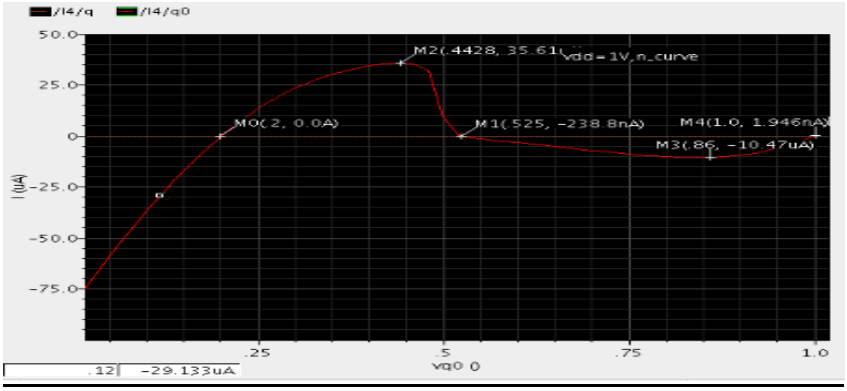

Figure 8. Conventional 6T SRAM cell N-curve.

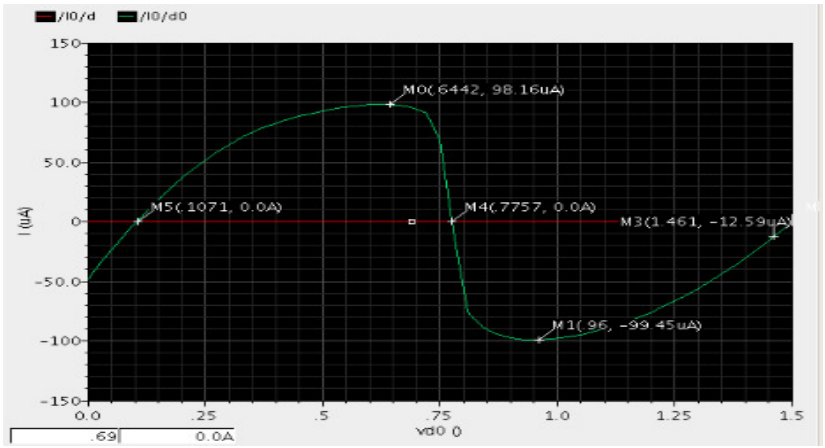

Figure 9. Proposed 8T SRAM cell N-curve.

SRAM bit cell internal noise voltage analysis results:

Fig 12 & fig 13 shows the internal voltage variations in read operation which is used to observe the variation in dc curve. Procedure to get below wave form is a one of the dc simulation for that add variable dc voltage in between the back to back inverter as shown in fig 10 , fig 11.

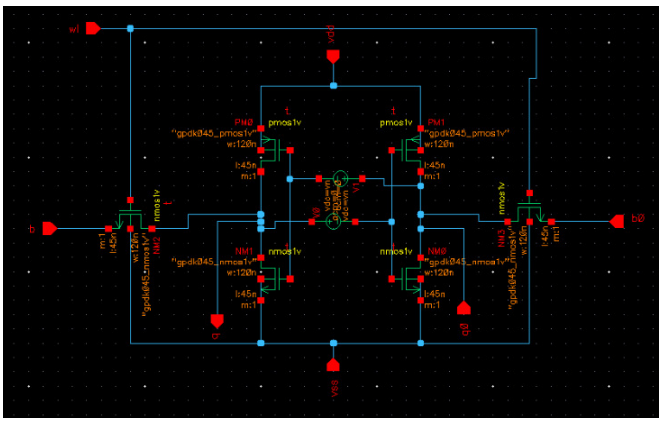

Figure 10. schematic to internal tolerable noise voltage measure in conventional 6T SRAM bit cell.

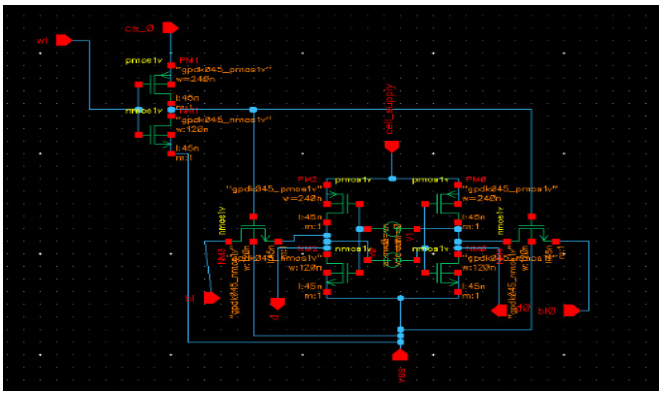

Figure 11. schematic to internal tolerable noise voltage measure in dynamic 8T SRAM bit cell.

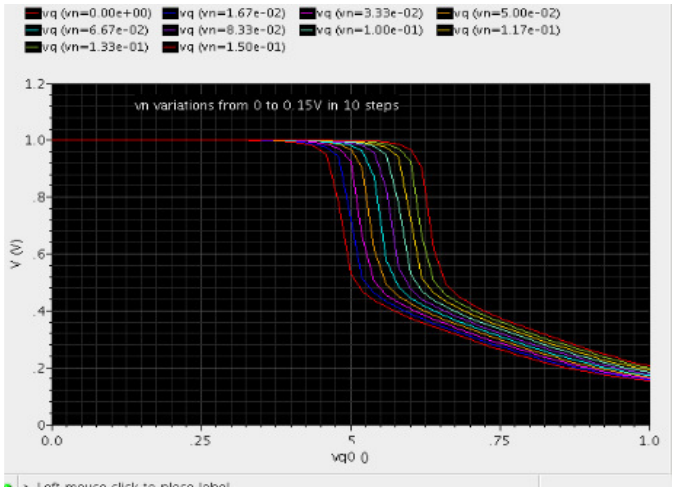

Figure 12. internal voltage Vn variations in read operation of 6T.

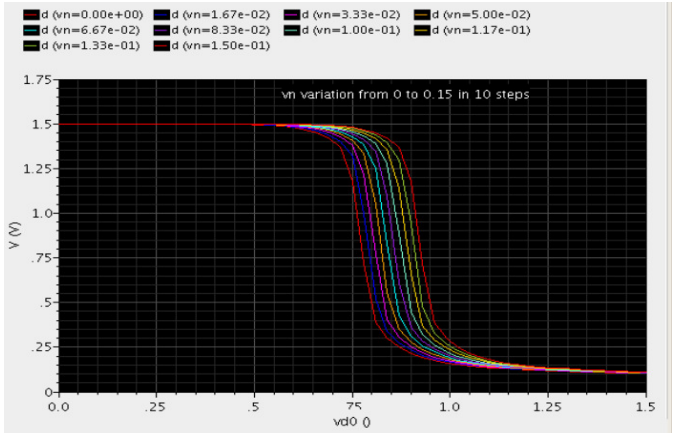

Figure 13. internal voltage Vn variations in read operation of 8T.

SRAM bit cell leakage current analysis results:

Below fig.14 & fig. 15 shows the leakage current calculation process in read operation. This is also DC simulation. Procedure to get leakage current is create block or symbol for bit cell then connect the nmos transistor source to leakage node, apply 0 dc voltage to the gate of the nmos transistor and connect remaining nodes of the circuit to ground.

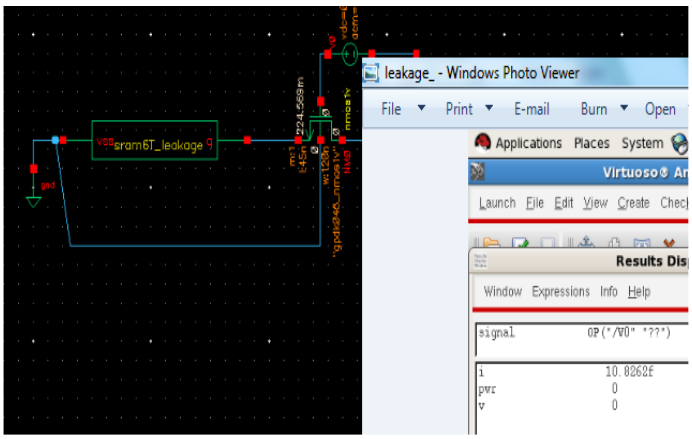

Figure 14. leakage current of 6T SRAM cell in read operation.

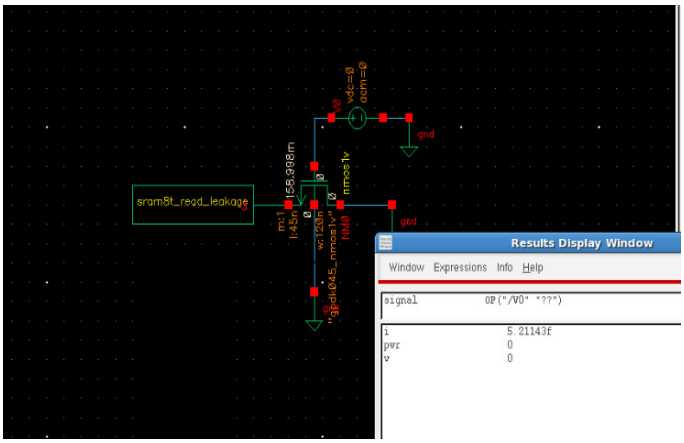

Figure15. Leakage current of 8T SRAM in read operation.

7. CONCLUSION

A fully differential 8T SRAM with a column-based dynamic supply has been proposed. Analyse both conventional 6T and proposed SRAM using N-curve. The proposed SRAM 8T cell has achieved improved read stability, read current and leakage current. N-curve metric was best method to analysis the cell stability it contains both voltage and current information. So, we can analysis the cell stability correct way. Above results prove that half of the leakage current was reduced and read stability of proposed cell achieve double amount approximately with comparing SRAM 6T cell.

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