SCOPE OF REVERSIBLE ENGINEERING AT GATE-LEVEL: FAULT-TOLERANT COMBINATIONAL ADDERS

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Abstract

Reversible engineering has been one of the thrust areas ensuring that continual process of the innovation trends that explore and sustain the resources of the nature. This reversible engineering is used in many fields like quantum computing, low power CMOS design, nanotechnology, optical information processing, digital signal processing, cryptography, etc. These are the digital domain implementations of Reversible and Fault-Tolerant logic gates. Any arbitrary Boolean function can be synthesized by using the proposed parity preserving reversible gates. Not only the possibility of detecting errors is induced inherently in the proposed high speed adders at their output side but also it allows any fault that affects no more than a single signal that is detectable. The fault tolerant reversible full adder circuits are realized by using two IG gates only. The derived fault tolerant full adder is used for designing other arithmetic- logic circuit by using it as fundamental building block. The proposed reversible gate is designed to have less hardware complexity and efficiecyt in terms of gate count, garbage outputs and constant input. In this paper, we design BCD adder using carry select logic, Carry-select and Bypass adders using FG gates, and newly designed TG gates.

Keywords

Delay, Miniaturization, Reversibility

1. INTRODUCTION

The process in which a product or system can be analysed in order to see how it works, to produce a similar version of the product or system more cheaply is referred to as Reverse engineering. Also the very instinct of human conception of driving ideas of future relying upon the past ideas propel the current area of the current topic under discussion, the Reversible and Fault-Tolerant Logic Gates design.

Based on Einstein's theory of "Traveling Back to Time" we develop the most amiable design of the reversible logic gates for the digital logic systems, which are a promising future in almost all areas of science and technology.

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Similar to that analogy, the Conventional Irreversible Gates such as simple AND, OR, XOR etc., are neither logically nor physically reversible.

Information loss = energy loss

- Fault-tolerant circuits that ensure the parity preservation through-out the circuit, are made use to reduce errors.
- Reversible logic circuits are those where the input vector can be recovered from output vector i.e., where the loss of information is avoided.
- Irreversible logic circuits dissipate heat whereas the reversible gates do not dissipate heat.

The first and important condition for any gate or device is said to be logically reversible if its input and output be uniquely retrievable from each other. The second condition for physical reversibility is that a device can run backwards also and it has to satisfy that no heat is dissipated according to the second law of thermodynamics.

Hence it can be seen that a reversible logic gate is an n-input, n-output logic device with one-to-one mapping helps to determine the outputs from the inputs and the inputs can be uniquely recovered from the outputs. Also to make the number of inputs is made equal to the number of outputs, Extra inputs or outputs are added whenever they seem to be necessary. The most important constraint on the design of a reversible logic circuit is that the fanout for the reversible logic gates is not allowed. Also, always the reversible circuit is designed using minimum number of reversible logic gates. The designed circuit has to produce minimum number of garbage outputs and the minimum number of constant inputs must be used which is a key requirement to achieve optimization.

The system process can be run in backward direction is supported by reversible logic. The system will not dissipate any energy until the system is able to return to its initial stage from its final state even if anything occurs in between. This was proved by C.H.Bennett[1] in 1973. The most promising computing technology application is the employment of reversible logic operations so that the information does not erase. Thus, they dissipate (virtually) zero heat.

Let us consider a reversible system in general before discussing it in detail. For any system to be reversible, it must be able to operate in a backward direction. This ability allows us to extract the inputs from the outputs of the system. The reversible circuits can be referred to as lossless circuits since there is no energy or information loss. When extremely low power consumption or low heat dissipation is desirable the reversible logic gates are used in areas of applications like low power VLSI Design, VLSI technology, Nanotechnology, Communications, Optical Computing, etc. As the quantum evolution is inherently reversible, Reversible logic has been found to be very useful in quantum computing.

According to R.Landauer's[2] research in the 1960s, the amount of energy or heat dissipated for every irreversible bit operation is given by (KT)*ln(2), where K is the Boltzmann's constant($1.3807*10^{-23}$ JK^{-1}) and T is the operating temperature. For T is equal to room temperature i.e., 300 K, (KT)*ln(2) is approximately $2.8*10^{-21}$J, which is small but non-negligible. Reversible circuits are the gates having same no. of inputs/outputs known as its width with 1-to-1 vectors of inputs/outputs mapping. Hence vector input states can be reconstructed uniquely from output states of the vector. Control lines are used in reversible gates to feed its reversible circuits from work bits i.e. ancillary bits. In a combinational reversible circuit, all gates are reversible as there is no fan-out or feedback.

Interest in reversible computation arises from the desire to reduce heat dissipation, thereby allowing: higher densities, higher speed, ability to retrieve back the inputs from outputs, reduction of power consumption and finally to increase the ease of error rectification.

DESIGN CONSTRAINTS [7] [17]

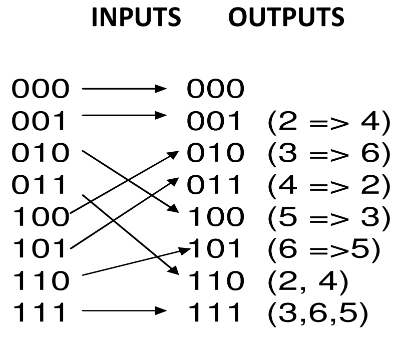
- Same number of outputs as that of inputs.
- Unique input to output pattern.
- Hardware complexity – A reduced model.
- Garbage outputs minimized.
- Gate count should be minimum.
- Constant value for inputs ['0' or '1'].
- Fan-out ='0'.

The paper is organized as follows. Section 2 presents the Basic reversible gates along with the new gate constructed used for simulation and synthesis. The circuits that are synthesized are presented in section 3. The possibilities for future implementations are described in section 4. Finally, we conclude in section 5.

2. BASIC GATES - BASIC REVERSIBLE GATES USED:

1. 4*4 IG Gate.
2. 3*3 F2G Gate.
3. 3*3 FG Gate.
4. 3*3 NG Gate.
5. 3*3 TG Gate.

Reversible circuits or gates are those which have one-to-one mapping between vectors of inputs and outputs. This allows the vector of output states to be used to reconstruct the vector of input states. Reversible logic can be obtained by the following relation as shown below:



2.1 IG GATE

This paper includes a 4*4 parity preserving reversible gate, IG[11], as depicted in Fig. 3. The gate is one-through, which means one of the input variables is also used as the output variable.

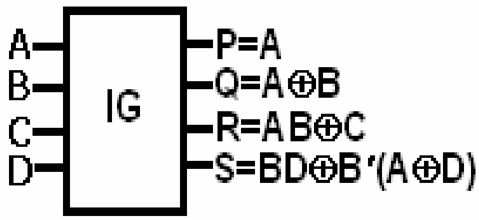


Fig 1: 4*4 IG Gate.

The truth table of this IG gate is shown in Table.1., which shows that this gate allows to uniquely determine the input pattern corresponding to particular output pattern.

As the Reversible IG gate is parity preserving. This property can be verified by comparing the input parity **A** XOR **B** XOR **C** XOR **D** to the output parity **P** XOR **Q** XOR **R** XOR **S**. This Reversible IG gate is universal as it can be used to implement any arbitrary Boolean function.

Table I: Truth Table For Parity Preserving IG GATE.

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	1
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	1
1	0	1	0	1	0	1	0
1	0	1	1	1	0	1	1
1	1	0	0	1	1	0	0
1	1	0	1	1	1	0	1
1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1

2.2 F2G GATE

A 3*3 Double Feynman gate [18][3].The input vector is I (A, B, C) and the output vector is O (P, Q, R). The outputs are defined as

P = **A**

Q= **A** xor **B**

R=**A** xor **C**

Then the Quantum cost of double Feynman gate is 2.

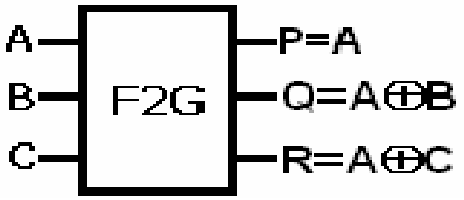


Fig 2: 3*3 Feynman Double Gate

Feynman Double gate is used as the fault tolerant copying gate when the input lines B and C are set to some constants may be ‘0’ or ‘1’ or as a combination of both ‘0’ and ‘1’.

Table II :Truth Table For FEYNMAN DOUBLE GATE.

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

2.3 FREDKIN GATE

Fredkin gate [4], shown in Fig.3, is a (3, 3) reversible gate which realizes P, Q and R where (A,B,C) is the input vector and (P, Q, R) is the output vector. As Fredkin gate is designed to be its own inverse, it is also a self-reversible gate. It is a conservative gate because the hamming weight of an input is same as its output.

This gate uses the input ‘A’ as the control input, i.e., if A = ‘0’, then the outputs have to be simply duplicates of the inputs; else A = ‘1’, and the output must have interchange of the B and C input lines.

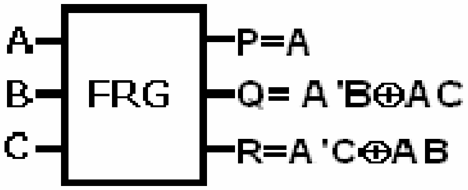


Fig 3: 3*3 FREDKIN GATE.

Fredkin gate also named as FG gate which is known as a universal reversible gate, i.e., This gate is used to construct the basic logic gates or blocks like AND, OR, NOT reversible gates. Also the other gates like NAND, NOR, XOR and XNOR reversible gates can be constructed by setting some of the inputs prior to use.

Table III: Truth Table For FRG GATE

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

2.4 NEW TG GATE

The proposed New TG gate is another gate that acts as the input value duplicator. It is basically a 3*3 reversible gate. This gate is represented as shown in Fig.4, the outputs are defined as

P=A
Q=B
R=AB xor C

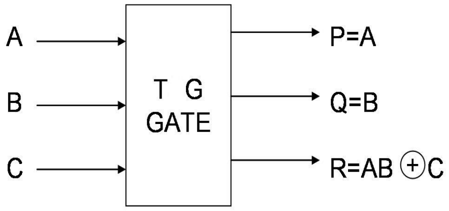


Fig 4: 3*3 New TG GATE

The truth table of the 3*3 New TG gate is as provided in the Table. IV. This satisfies the conditions imposed for reversibility.

Table IV: Truth Table Of New TG GATE

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	1
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

2.5 NEW GATE

The New Gate[7] is as shown in Fig.5 is another gate which implements all the basic operations like a universal gate i.e., all other gates can be derived from this gate using the inputs and outputs in either directions to implement any logic circuit. This gate is represented as shown in Fig.4, the outputs are defined as

P=A
Q=AB xor C
R=A'C' xor B'

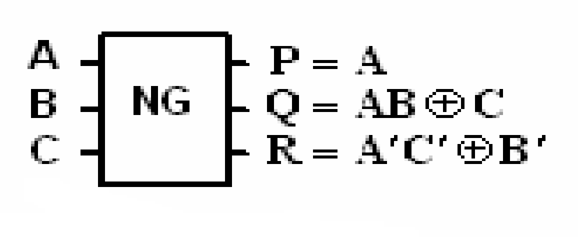


Fig 5: 3*3 NEW GATE

The truth table of NG gate that satisfies all of the parity preserving properties required for reversibility is provided in Table V.

Table V: Truth Table Of NEW GATE

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	0	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	1	1	1
1	1	0	1	1	0
1	1	1	1	0	0

3. CIRCUITS SYNTHESISED

Addition is not only common arithmetic operation, but it is also the most time-critical operation. As a result, a wide range of adder architectures have been developed that allow a designer to trade off complexity in terms of the gate count, hardware complexity, fan-out, etc for performance of Arithmetic and Logic Units. Some of the multi-bit adder architectures are usually broken into smaller adder blocks[8]. To optimize computation time, the length of these blocks can be varied based on the propagation delay of the circuits.

The block based adders include the carry bypass adder which will determine Propagate (P) and Generate (G) values for each block rather than each bit, and the pre-generated sum and carry values for either possible carry input to the block can be obtained by carry select adder.

The following are the various adders based on the Reversible logic.

1. CSA (Carry-Select Adder)
2. BCD (Binary-Coded-Decimal)

3. BCD Adder with Carry-Select Logic
4. Carry-Bypass Adder.
5. 16-bit Carry-Bypass Adder

Starting from the existing Fault-Tolerant Full adder using universal parity preserving 4*4 IG gate, the discussion is made.

FTFA

Fault tolerant logic synthesis [11][10][7][12] of reversible full adder Circuit[9] requires that its individual gate unit must be fault tolerant reversible gates. A fault tolerant reversible full adder circuit requires at least three garbage outputs and two constant inputs. The fault tolerant reversible full adder circuit presented is given below:

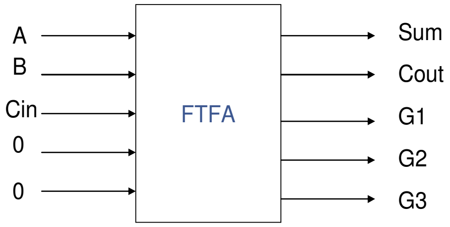


Fig 6: Block Diagram Of FAULT TOLERANT Full Adder.

The internal structure appears as below with two IG gates leading to the Fault-tolerant full adder circuit.

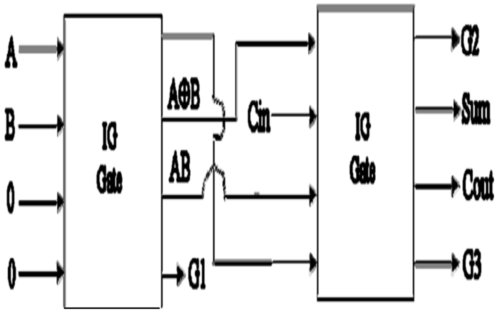


Fig 7: FAULT-TOLERANT REVERSIBLE Full Adder Circuit.

3.1 CARRY SELECT ADDER

The carry-select adder [11][10] gives better result than that of carry skip adder as it is faster in processing the output result. In carry skip scheme, carry is skipped only for a particular condition, i.e. when either of the input is one. Hence the delay will be less as the output carry does not propagate in ripple fashion from one stage to another stage. Also this delay can be further reduced by selecting a pre-computed sum and carry outputs depending on the selected input carry signal binary value. The carry select concept can be better understood from the Fig.8. The basic problem faced in speeding up carry propagation is the fast processing of late carry input. As the input carry can have only two possible binary values i.e., ‘0’ and ‘1’, then two results are possible; one when the input carry is zero and the other when input carry is one (S_{0i}, C_{0i+1} and S_{1i}, C_{1i+1}) respectively.

The outputs of adder can be pre-computed and selected for sum and carry that depend on the late input carry (Ck) that is dependent upon the applied input carry. Selection of the final sum and carry is done by using the following equations:

Si = Ck.S0 i + Ck.S1i (1)
Ci+1 = Ck.C0i+1 + Ck.C1i+1 (2)

Hence, the resulting carry select adder scheme uses two full adders (i.e., represented by FA), one input having Ck = ‘0’ and the other input having Ck = ‘1’ and two multiplexers with two inputs to one output are used for each sum bit and output carry selection.

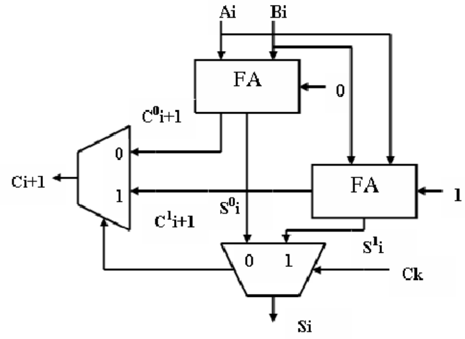


Fig 8: CARRY SELECT SCHEME.

The proposed CSA with reversible gates is given as follows:

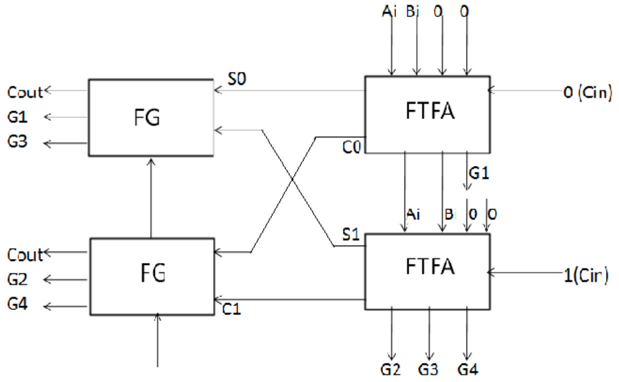


Fig 9: CARRY SELECT ADDER USING REVERSIBLE GATES.

Here, in the design of Carry-Select Adder the Fredkin Gate is made use as a multiplexer to select the final outputs with the enable as external carry.

3.2 BCD ADDER

In electronic systems and computers, binary-coded decimal (BCD) is a 4-bit digital encoding method for decimal numbers in which each digit is represented by its corresponding binary sequence. In BCD, a numeral is usually represented by four bits which represent the decimal ranging from 0 through 9. Other bit patterns are sometimes used for magnitude or other indications like error, overflow, etc.

Uncompressed BCD consumes a byte for each represented numeral, whereas compressed or packed BCD typically carries two numerals in a single byte by taking advantage of the fact that four bits will represent the full numeral range from 0 to 9.

The main advantage of BCD adder is ease of machine- and human-readable formats conversion. Also it allows the decimal quantities to be represented in a more precise machine-format, which is easy to convert decimal digits for printing the data, to display the data in the machine, and to perform faster decimal calculations.

As compared with the typical binary formats, BCD's main drawbacks are a small increase in the circuit complexity which is required to implement basic mathematical operations and less efficient usage of storage facilities i.e., the memory usage.

The subtle conversion and rounding errors that are inherent to floating point binary representations cannot be tolerated in applications like financial, commercial, and industrial computing. Hence, even though BCD is not as widely used, decimal fixed-point and floating-point formats are still important and continue to be used in the above fields.

These reversible BCD circuits[18][3][20][19] are basis of the decimal ALU of primitive Quantum CPU. Complexity of the circuit is less.

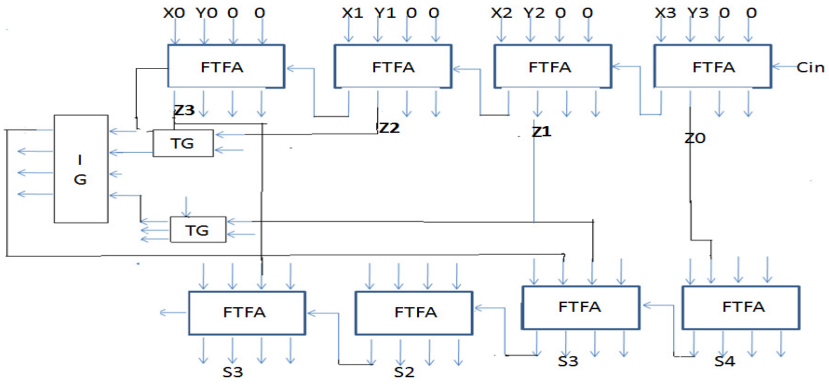


fig 10: BCD ADDER

3.3 BCD ADDER WITH CARRY-SELECT LOGIC

Reversible Logic Implementation of Carry-Select BCD Adder, in this BCD adder[2], the carry select concept is implemented using five reversible gates which form a block. To compute sum and carry for the two possibilities of carry-in, two FTFA gates are used which act as full adders. One of the input bits is given to a Feynman gate[6][7] to duplicate it, as fan-out is not allowed in reversible logic. Depending on the input carry the output sum and carry are selected by using Fredkin gates instead of using multiplexers in the design.

The usual BCD operation is performed by using FTFA and New gates for the design of BCD adder. The reversible logic gates based implementation of carry select BCD adder is shown in fig.11, and this gives the results as (i). the number of reversible gates used = 27 and (ii). the number of garbage outputs produced = 39.

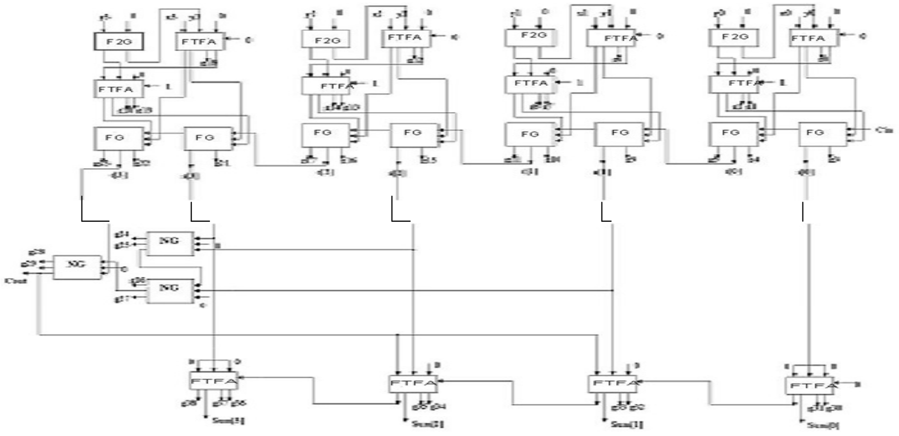


Fig 11. BCD ADDER USING CARRY-SELECT SCHEME.

3.4 CARRY-BYPASS ADDER

This adder is the fundamental block in any arithmetic unit and speed limiting circuit in digital system. One of the fastest and efficient architecture in terms of area and power dissipation. Propagation delay is reduced compared to ripple carry adder.

The two addend bytes are split into blocks of n bits. The output carry of each block is dependent on the input carry only if, at least one addend has a 1 bit for each of the n bits of the block. The output carry $Cout_{i+n-1}$, for the block corresponding to bits i to i+n-1 is obtained from a multiplexer, wired as follows:

- SEL = $(A_i + B_i)(A_{i+1} + B_{i+1})...(A_{i+n-1} + B_{i+n-1})$
- A = $C_{ripple,i+n-1}$ (the carry output for the ripple adder summing bits i to i+n-1)
- B = $C_{out,i-1}$

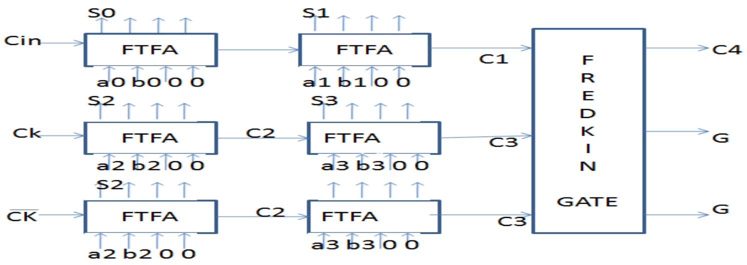


Fig.12: 4-BIT CARRY-BYPASS ADDDER

3.5 16-BIT CARRY-BYPASS ADDER

The proposed model for the 16-bit Carry-bypass adder developed using the existing FTFA, FG and IG gates along with the designed 4-bit Carry-bypass Adder. This adder with new gate performs well for reversibility with a delay of 39.878nSec when compared to other gates.

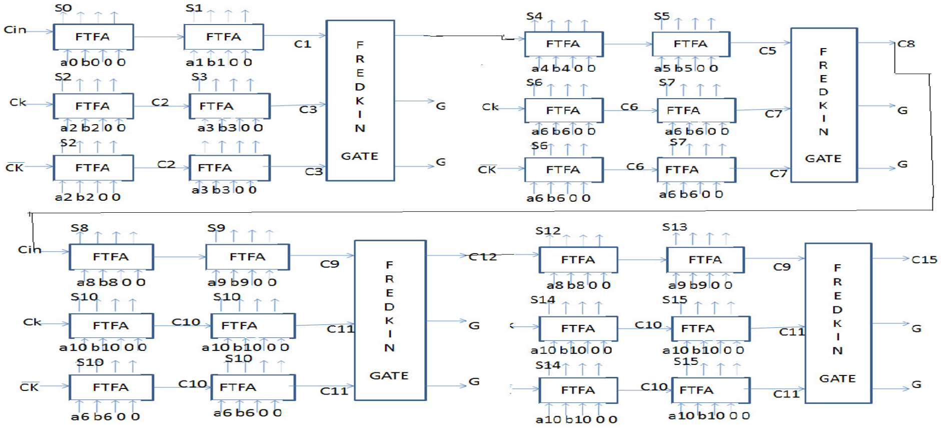


Fig 13: 16-BIT CARRY-BYPASS ADDER.

4. FUTURE SCOPE

The current development of Combinational Adder circuit synthesis at Gate level can be even improved for sequential circuits using the reversible logic synthesis design criteria for it. Also the same circuits can be even improved using the further recent gates that provide a better reduced power dissipation and delay. And so the building block of the Computers ALU (Arithmetic and Logic Unit) and even other circuit components like multipliers, shifters, etc can be implemented. Also these reversible logic circuits are used in many applications like in the areas of digital image processing and communications for enabling the storage and hence to retrieve back the same information that is being stored. As the wide range of applications of reversible adders are laptops, handheld, wearable computers, spacecrafts, implanted medical devices, wallet Smart cards and tags.

5. CONCLUSION

The focus of this paper is towards the design of the fault-tolerant and high speed reversible logic circuits for the BCD, Carry-select adders with an efficient parity preserving reversible NG circuit has been presented. The proposed parity preserving reversible New TG gate is better than the existing reversible gates in terms of hardware complexity, gate count, garbage outputs, unit delay and constant inputs. Finally, this paper presents a novel implementation and realization of fault tolerant reversible circuits and demonstrates its superiority than the existing designs in terms of computational complexity. All the circuits are synthesized and verified using Xilinx 10.1SE software tool.

Computers are intrinsically probabilistic machines, constrained by reliability of their algorithms and component parts. They throw away millions of bits, billions of times every second. They are based on irreversible logic devices, which have been recognized as being fundamentally energy-inefficient for several decades. Truly, the only way we might ever get around this limit is by using reversible computing for the nanoscaled devices. Synthesis of more parity-reserving reversible circuits with less hardware along with full adders are now being developed and studied.

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