An approach to design Flash Analog to Digital Converter for High Speed and Low power Applications

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ABSTRACT

This paper proposes the Flash ADC design using Quantized Differential Comparator and fat tree encoder. This approach explores the use of a systematically incorporated input offset voltage in a differential amplifier for quantizing the reference voltages necessary for Flash ADC architectures, therefore eliminating the need for a passive resistor array for the purpose. This approach allows very small voltage comparison and complete elimination of resistor ladder circuit. The thermometer code-to-binary code encoder has become the bottleneck of the ultra-high speed flash ADCs. In this paper, the fat tree thermometer code to-binary code encoder is used for the ultra high speed flash ADCs. The simulation and the implementation results shows that the fat tree encoder performs the commonly used ROM encoder in terms of speed and power for the 6 bit CMOS flash ADC case. The speed is improved by almost a factor of 2 when using the fat tree encoder, which in fact demonstrates the fat tree encoder and it is an effective solution for the bottleneck problem in ultra-high speed ADCs.The design has been carried out for the 0.18um technology using CADENCE tool.

KEYWORDS

TIQ, FAT TREE TC-BC ENCODER, CMOS, ANALOG TO DIGITAL CONVERTER.

1. INTRODUCTION

The flash Analog to Digital converter architecture is the good solution for high Speed Analog to Digital converter designs, but from a power dissipation and area perspective it is not efficient for the resolution of more than 8 bits. As long as the resolution level is kept Small, the comparator count will be reasonable. The Comparator structure is the most critical part in full-flash type architectures. Some of the problems of the conventional comparator structures used in A/D designs are [1]:

1. Large transistor area for higher accuracy
2. DC bias requirement

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3. Charge injection errors
4. Metastability errors
5. High power consumption
6. Resistor or capacitor array requirement.

The Threshold Inverter Quantizer (TIQ), based on systematic transistor sizing of a CMOS Inverter in a full-flash scheme, eliminates the resistor array implementation of conventional Comparator array flash designs [2]. Therefore no static power consumption is required for quantizing the analog input signal, making the idea very attractive for battery-powered applications. However there are some disadvantages in the TIQ approach. They are, It is a single ended structure, It requires 2^n-1 different area sized quantizer designs, and It requires a separate 5V reference power supply voltage for analog part only due to poor power supply rejection ratio. Also It has slight changes in linearity measures (DNL, INL) and the maximum analog signal range due to process parameter variations. These problems can be handled by front end signal conditioning circuit .It requires S/H at the analog input to increase the performance and to reduce the power consumption during metastable stage.

The comparator is the most important part in the ADC architectures. It's main function is to convert input voltage Vin into logic 1 or logic 0 by comparing the reference voltage V_{ref} with V_{in}. If V_{in} is greater than V_{ref} , the comparator output voltage is 1 else it is 0.The TIQ comparator will use two cascaded inverters as comparators for high speed and low power consumption.

Mathematically, the midpoint voltage V_{mid} is given by,

$V_{mid}=(r(V_{dd}-\_V_{tp}\_)+V_{tn}) / (1+r)$ with $r=(Kp/Kn)1/2$

where V_{tp} and V_{tn} represent the threshold voltages of the PMOS and NMOS devices respectively [2]. At the first inverter, the analog input signal quantization level is set by V_{mid},depending on the W/L ratios of the PMOS and NMOS. The second inverter is used to increase voltage gain and to prevent an unbalanced propagation delay.

The TIQ flash ADC requires 2^n-1 different size comparators. However choosing the needed V_{mid} for comparators and generating the selected comparators with a custom layout are difficult jobs. For example, a 10-bit flash ADC would need 1023 TIQ comparators, too many for manual layout designs, while other ADCs use a single comparator design and simply duplicate it for 2^n-1 times. However, a customized program has been developed [2] that automatically generates the TIQ comparators with an optimal selection approach.

A CMOS inverter consists of one PMOS and one NMOS transistor, with the inverter switching threshold voltage, depending upon the transistor sizes. If the length of both the PMOS and NMOS are fixed, then different inverter threshold voltages can be obtained by simply varying the transistor widths. There are two design methods for the TIQ comparator for the V_{mid} values.

One method, called the Random Size Variation (RSV) technique, can obtain the 2^n-1 reference voltages by selecting the inverter width from the full range of 3-D surface without considering the relation of adjacent comparators. The other method, called the Systematic Size Variation (SSV) technique, considers the relation of comparators in selection of the inverter size. Perhaps the most critical issue for the Threshold Inverter (TI) comparator based ADC is the process variation [3]. One solution is to add a programmable pre-amplifier to the analog input of the ADC to dynamically fine-tune the offset, gain, and linearity. Another solution is to perform digital signal processing on the ADC output to correct the offset, gain, and linearity.

The thermometer code-to-binary code encoder(tc-bc) has become the bottleneck of the ultra-high speed flash ADCs[4].The fat tree thermometer code-to-binary code encoder is highly suitable for the ultra-high speed flash ADCs. The main advantage of the fat tree encoder over the other encoders is the high encoding speed. Also the fat tree encoder consumes less power compared with other encoders.The speed is improved by almost a factor of 2 when using the fat tree encoder.

This paper presents 6-bit flash Analog to Digital Converter at 0.18u technology, which uses TIQ concept for the generation of the reference voltages in Quantized Differential Comparator and encoder design, which is based on the Fat Tree Encoder Design.

2. A 6-BIT FLASH ADC

Figure 1. shows the block diagram of proposed Flash ADC.The comparators compare the input voltage with internal reference voltages, which are determined by the transistor sizes of the Quantized Differential Comparator.

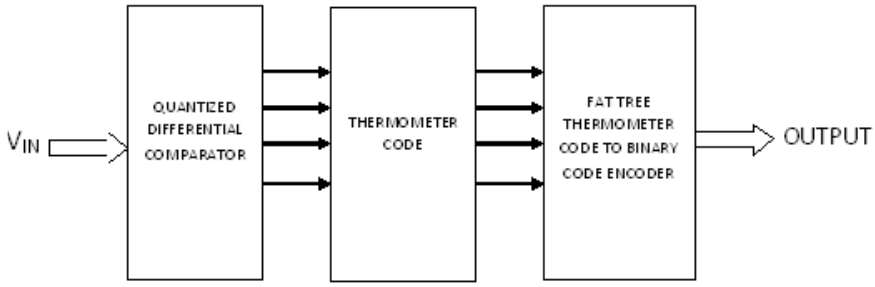


Figure 1. Block diagram of the proposed Flash ADC

The output of the comparator is logic 1 or logic 0 depending on the applied input voltage. In the conventional differential voltage comparator [8, 9], the transistor sizes are matched and the input V_b is taken from V_{ref} generated by the resistor ladder circuit.

Therefore all the comparators of n-bit flash ADC are identical. On the other hand, we use different transistor sizes of the transistor M2 of the differential pair to create an offset voltage in Quantized Differential Comparator.

In addition, the voltages at V_2 and V_b are constants and input voltage is applied to the V1 terminal (Figure 2). In addition to this, 2^n-1 different sizes of comparators are needed for the flash ADC implementation. To get sharp Voltage Transfer Characteristic (VTC) curves the inverter is used at the output of the differential amplifier.

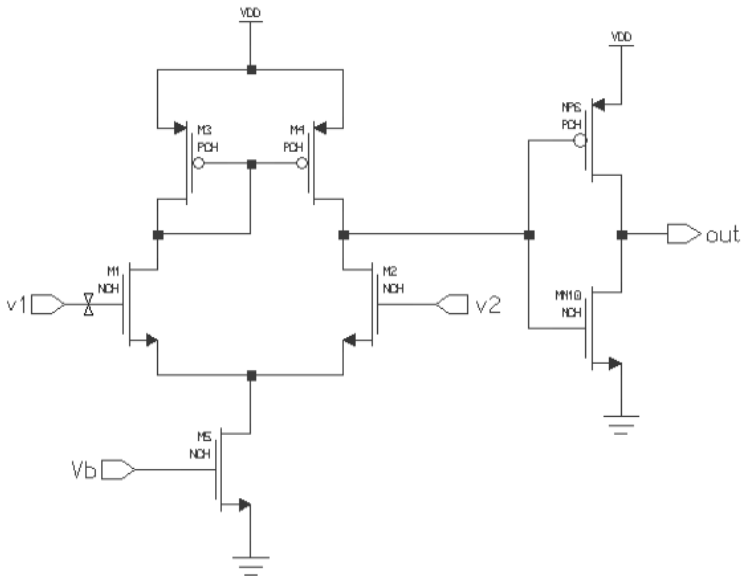


Figure2.Quantized Differential Comparator

To design n-bit flash ADC, requires 2^n-1 equal quantization voltages, and those many number of Quantized Differential Comparators. A thermometer code has been developed to generate the different sizes of transistors for different reference voltages of the comparators and the device sizes have been picked up from the data generated to match the requirements. After the comparators produce a thermometer code, it is converted to binary code.The TC-to-BC encoding is carried out in two stages in the fat tree encoder.The first stage converts the thermometer code to one-out-of-N code. The one-out-of-N code is same as an address decoder output. This code conversion is done in N bit parallel using N gates. Figure. 3 shows the two stage fat tree TC-to-BC encoder.

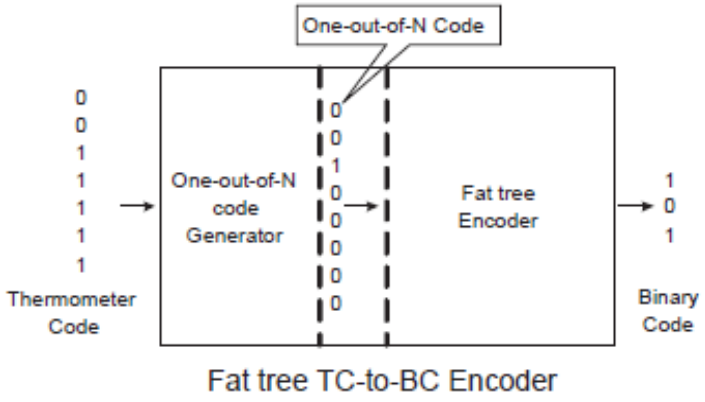


Fig.3 The two stage fat tree TC-BC encoder

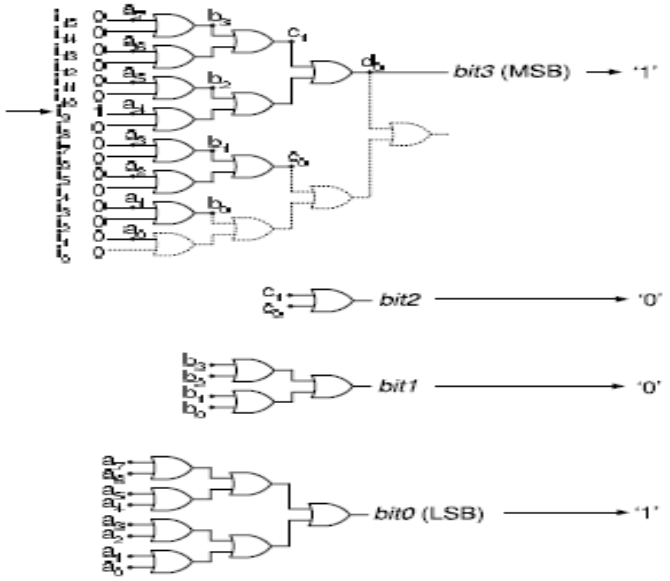
The second stage converts the one-out-of-N code to binary code using the multiple trees of OR gates. Figure 3 shows an example of a 4 bit ADC case. A 16 bit one-out of- N code is presented to the leaf nodes of the tree and 4 bit binary code output is produced at the root nodes of the trees.

One may superimpose one tree over the other tree and imagine a 3-D visualization of the trees in Figure .4.

An edge count of a node increases as the tree height increases ,so it is named as a fat tree. Algorithmically, the fat tree circuit signal delay is $O(\log_2 N)$ .But for other encoders this signal delay is different, for example the ROM circuit signal delay is O(N),and the Wallace tree encoder [5] signal delay is $O(\log_{1:5} N)$.Therefore, the fat tree circuit is the fastest speed circuit.

From Figure. 4 we can understand that there are three OR gate delays from any leaf node to any root node. The signal delay from the N - 1 inputs to the n outputs is uniform in the fat tree encoder. This is an important property allowing high speed wave pipelining without the pipeline registers. Apart from the speed, the fat tree of OR gates is an all digital circuit and it does not require a clock signal.

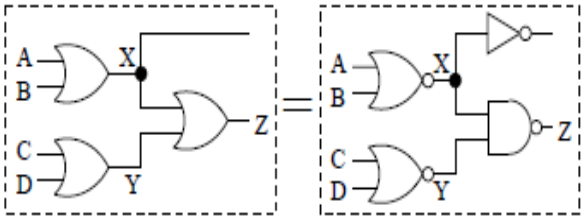
The fat tree circuit is more noise tolerant than other encoder circuits. Full static CMOS implementation of the OR gates eliminates any static power consumption otherwise necessary in circuits with pull-up resistors.Therefore, the fat tree circuit is less power consuming circuit.



bit0 = a0 + a1 + a2 + a3 + a4 + a5 + a6 + a7 = 1
bit1 = b0 + b1 + b2 + b3 = 0
bit2 = c0 + c1 = 0
bit3 = d0 = 1

Fig.4.An example of a 4-bit ADC case

For a more efficient implementation in CMOS, we can replace the OR gates with NOR and NAND gates using the DeMorgan's theorem, shown in Figure. 5.



$$Z = \overline{XY} = \overline{\overline{(A+B)} \bullet \overline{(C+D)}} = (A+B)+(C+D)$$

Fig.5.Fat tree logic implementation

3. SYSTEM PERFORMANCE

The proposed Quantized comparator and fat tree encoder based flash ADC has been designed for TSMC 0.18u technology using CADENCE. The proposed approach has been validated through extensive HSPICE simulations. Simulation results are given in Figure .6.

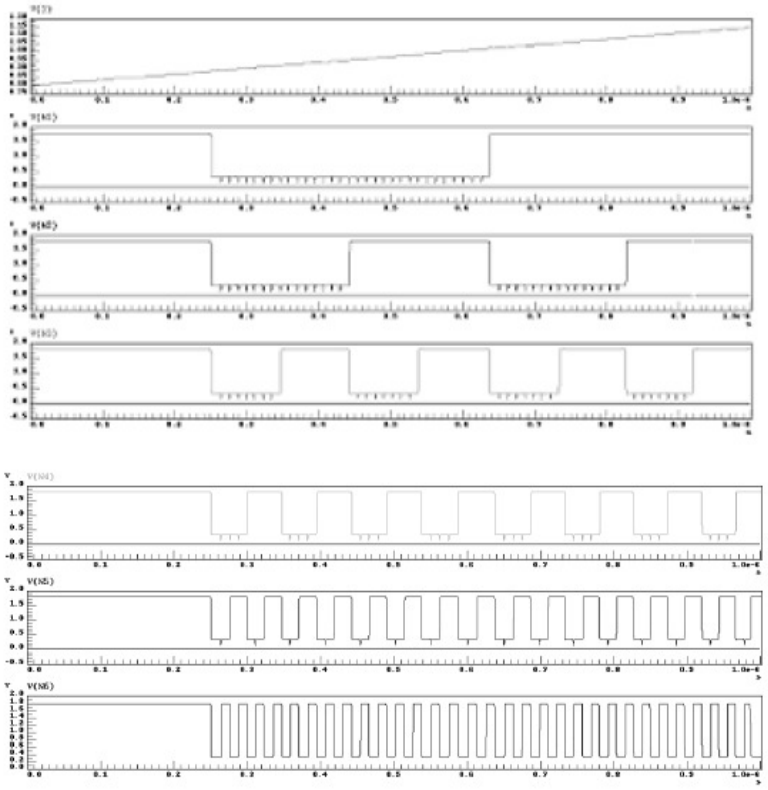


Figure 6. Simulation results for the 6-bit flash ADC using the Quantized Differential Comparator

ADCs	Technology	Power Dissipation
Proposed CMOS	0.18μm	36.98mW
6-bit TIQ[2]	CMOS 0.25 μm	59.91mW
6-bit Flash[5]	GaAs 0.5 μm	970mW
6-bt Flash[7]	CMOS 0.6 μm	380mW
6-bit Flash[8]	CMOS 0.4 μm	400mW
6-bit Flash[9]	CMOS 0.6 μm	330mW

Table 1. The proposed ADC power dissipation in comparison to other ADCs in the literature.

Table.1 gives the comparison with other ADCs.

4. CONCLUSION

A flash ADC design, based on a Quantized Differential Comparator and fat tree encoder approach has been proposed. The design has been carried out for 0.18u technology and validated through HSPICE simulation circuit topologies and simulation results have been presented. Since the reference voltages are generated internally the power dissipation is reduced. The results obtained are encouraging and indicate that the proposed approach can be promising one for battery driven applications such as SOCs. The speed is improved by almost a factor of 2 when using the fat tree encoder, which in fact demonstrates the fat tree encoder, is an effective solution for the bottleneck problem in ultra-high speed ADCs.

5. REFERENCES

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