THRESHOLD VOLTAGE CONTROL SCHEMES IN FINFETS

V. Narendar[1], Ramanuj Mishra[2], Sanjeev Rai[3], Nayana R[4] and R. A. Mishra[5]

Department of Electronics & Communication Engineering, MNNIT-Allahabad
Allahabad-211004, (U.P)-India

[1]narendar.vadthiya@gmail.com
[2]ramanujmishra1@gmail.com
[3]srai@mnnit.ac.in
[4]nayana.r.r@gmail.com
[5]ramishra@mnnit.ac.in

ABSTRACT

Conventionally polysilicon is used in MOSFETs for gate material. Doping of polysilicon and thus changing the workfunction is carried out to change the threshold voltage. Additionally polysilicon is not favourable as gate material for smaller dimensional devices because of its high thermal budget process and degradation due to the depletion of the doped polysilicon, thus metal gate is preferred over polysilicon. Control of workfunction in metal gate is a challenging task. The use of metal alloys as gate materials for variable gate workfunction has been already reported in literature. In this work various threshold voltage techniques has been analyzed and a novel aligned dual metal gate technique is proposed for threshold voltage control in FinFETs.

KEYWORDS

Dual-Metal gate (DMG), FinFET, Gate Workfunction, Independent-Gate (IG), Short channel Effects (SCEs), Threshold voltage (VT).

1. INTRODUCTION

CMOS technology dimensions have been continuously scaling, that it has reached its fundamental limits such as carrier mobility degradation because of impurity, severe gate tunneling effect with decreasing oxide thickness, high p-n junction leakage current as the junction becoming shallower [1]. FinFET [2] is an innovative MOS device structure which gives superior performance because they are less effected by short channel effects (SCEs) [3] can be built using standard bulk planar CMOS processing, can be practically analyzed for analog as well as digital applications and considered to be the best candidates for sub-65 nm scaling of MOSFETs.

As variation of threshold voltage is very vital in digital as well as analog applications such as MT-CMOS, DOMINO logics, SRAMs [15], in this paper we are trying to analyze and compare various threshold voltage control schemes for FinFET. In this work 32nm FinFET is designed by Sentaurus structure editor [4] of Sentaurus TCAD. The simulations were performed by using Sentaurus device simulator [5] of Sentaurus TCAD.

Since the size of transistor in IC is continuously scaling, it is worthwhile to consider the challenges that CMOS industry is facing and to discuss how to address them. Switching power (power required to switch a transistor on or off) is equal to 0.5*Cg*VDD2 [6] where Cg is gate capacitance and VDD is power supply voltage. CMOS scaling has traditionally involved reduction of both the gate length LG (which proportionally reduces CG) and VDD. As VDD is reduced for the same off-state current IOFF (and therefore the same threshold voltage VT), the on-state current ION drops due to reduced gate overdrive (VGS – VT) .So for better on state current, the value of Vt also decreases with VDD but at the same time low Vt increases the on state current and hence the static power dissipation. Either way, VDD scaling is necessary in order to reduce power density on an IC, since increased power density leads to heat which reduces device performance (due to reduced mobility) and further increases standby power consumption (due to increased thermal leakage). Thus, to the device designer, the present and future goal of CMOS scaling is to keep ION as high as possible while scaling VDD. The FinFETs suffers from short channel effects in the sub 50 nm regime due to reduction in threshold voltage because of Vt-Rolloff. For high speed switching operation, threshold voltage should be low at the same time low threshold voltage results in high on state current but for low threshold voltage IOFF is high. So the lower limit of the threshold voltage is set by the amount of off-state leakage current. In order to meet the tradeoff between speed and I off and considering the power supply constraints the VT is set accordingly. On state and off state currents of MOSFET directly depends on threshold voltage. For higher threshold voltage on state current will be lower and at the same time the off state current is lower for higher threshold voltage. Ratio of Ion and Ioff is known as figure of merit for MOSFETs. Higher value of ION/ IOFF is desirable. High on state current results in higher current drive. Lower off state current results in low static power dissipation.

Threshold voltage of NMOS directly depends on workfunction difference between the gate and the channel. This difference is called gate barrier. Variation in gate barrier has very dominant effect in threshold voltage of MOSFET. In this work different characteristic along with threshold voltage is measured.

In this work we have analyzed independent gate FinFET [6] for threshold voltage variations. Threshold voltage of MOSFET depends on depletion region charge. The idea is to vary this charge by applying constant DC bias on one gate and using second gate as input terminal. By applying different gate bias DC voltage on this gate we can vary the depletion region charge of MOSFET and a significant variation in overall threshold voltage is achieved. If we tie both gate of IG-FinFET [13] we will have a connected gate DG-FinFET. Characteristics of DG-FinFET under different gate barrier are also done. Simultaneously different parameters of both configurations also extracted.

Another method of channel under/over lapping is also proposed for threshold voltage variation. We used gate length of 32nm in this work. Threshold voltage of FinFET depends on channel length and relative position of channel with respect to gate (gate contact). Threshold voltage analysis along with other parameter is done. As we increase channel under lap towards drain

/source region threshold voltage increases. Using different channel overlapping desired threshold voltage can be achieved.

For threshold voltage optimization, variation of gate barrier in TG-FinFET is a superior method than IG-FinFET mode of operations. So a novel aligned dual metal gate FinFET structured is proposed. Molybdenum and tungsten are metal with different gate workfunctions. Metals are aligned as shown in Figure 4 .Metals alloy for threshold voltage control [7], [8] is reported in previous works. By changing the content of individual metal in alloy different workfunctions can be obtained. Here instead of making alloy we applied separate gates of tungsten and molybdenum along the channel. Tungsten has lower work function that molybdenum. We made TG-FinFET using molybdenum as gate contact metal and measured its characteristics. Again we repeat the experiment using tungsten as gate contact metal. Threshold voltage of tungsten gate (VT-TN) FinFET is found to be lower than threshold voltage (VT-MO) of molybdenum gate FinFET. By using both metals simultaneously as gate contact of FinFET we can achieve the threshold voltage with in VT-TN and VT-MO. Effective gate length of FinFET is 32nm out of which X nm is molybdenum gate length and (32-X) nm is Tungsten gate length. This whole device is acting as two FinFET connected in series. One FinFET is Molybdenum gate and other one is tungsten gate FinFET. Threshold voltage of molybdenum gate FinFET is higher than tungsten gate FinFET. Overall threshold voltage lies between these threshold voltages. We can achieve different value of threshold voltage by varying value of 'X'. Threshold voltage for different values of X is calculated and other standard parameters like I_{ON}, I_{OFF}, DIBL and subthreshold threshold slope are also extracted.

2. DEVICE STRUCTURES AND SIMULATION SETUP

Figure 1 shows the 2-D schematic top view of FinFET. Figure 5 shows the 3-D view of SOI-FinFET device. Device dimensions are shown in Table 1. In this work we have performed simulation on different devices designed by Sentaurus structure editor .All simulation has been performed on 3-D FinFET structures. Before simulation TCAD tool is properly calibrated. Calibration of tool is very vital for FinFET simulations as current flow in actual FinFETs will be dominated by {1 1 0} plane. Sufficient mesh refinements were applied to the fin region and the inversion layer regions to capture the inversion layer quantization.

For triple gate MOSFET simple structure is considered which is shown in Figure 1. All gates are electrically connected in TG-FinFET and all side of gates contributing effectively in current flow. Transfer characteristics of this device are studied for different metal gate work functions. Since threshold voltage of devices depends on gate barrier we have gotten different threshold voltages for different gate barriers. Simultaneously other important parameters subthreshold slope, DIBL, on state current and off state currents also measured.

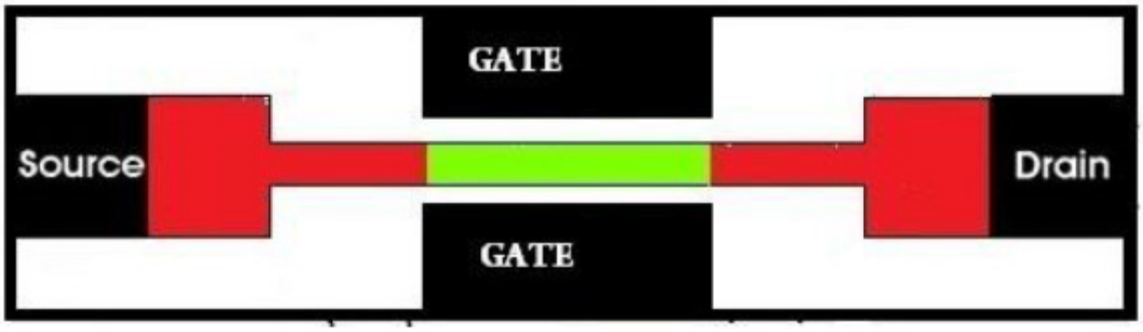


Figure 1. Top view of DG/TG FinFET all gates are electrically connected

In second part of this work N-type independent gate FinFETs (IG-FinFETs) have been designed and characterized. Here IG-FinFET [10] is a double gate FinFET in which a first gate is used as input terminal and second gate is for controlling the threshold voltage of device. Using one gate to adjust threshold voltage allows device designers to utilize intrinsic device bodies, avoiding the random dopant fluctuation scaling limit [9].Variation in threshold voltage with back gate (second gate) bias is examined simultaneously other vital parameters are also extracted. Device diagram and schematic top view is shown in Figure 2. DG-FinFET with connected gate is also studied.

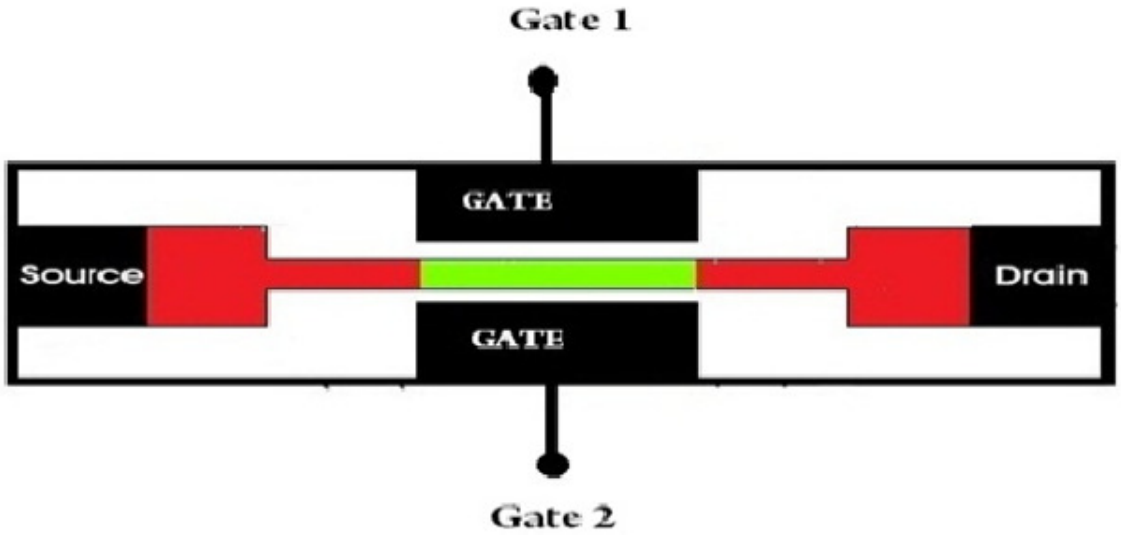


Figure 2 Top view of IG-FinFET

Analysis of threshold voltage under different channel lapping is studied. Top view of channel lapping is shown in Figure 3. Here ΔLg is channel extension towards source/drain. This extension is symmetric so effective channel length is Lg+2ΔLg. extension of drain and source into channel referred as channel underlap and extension of channel towards drain/source is called channel overlap. Value of ΔLg is positive for channel overlap and negative for channel under lap.

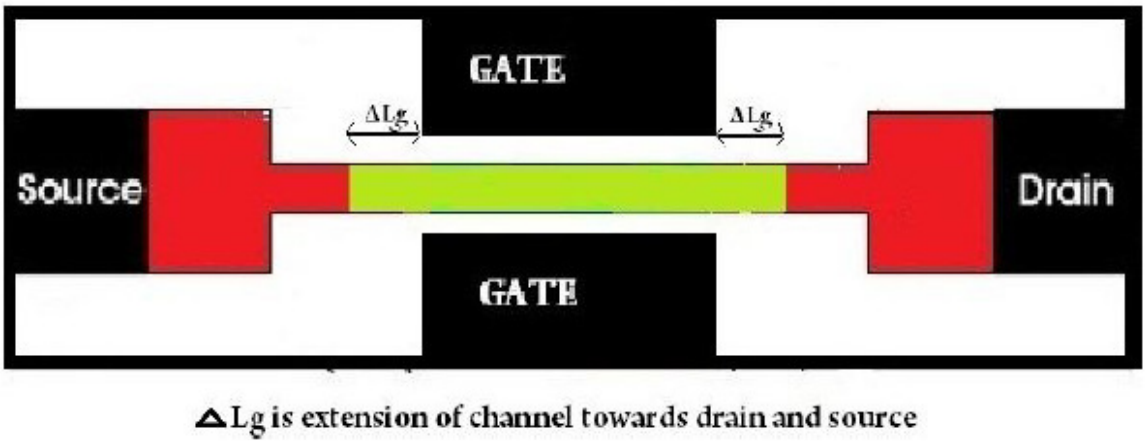


Figure 3 Top view of extended channel FinFET

In final part of this work a novel dual metal gate FinFET is designed and characterized. We propose a new aligned metal-gate CMOS technology that uses a combination of two metals to vary threshold voltages for both n- and p-MOSFET‟s. Molybdenum is used as first gate metal and tungsten is used as second gate metal. For different length of individual metal over gate oxide different threshold voltage has been reported ,simultaneously different characteristics such as on state current, off state current, SS, DIBL are also measured. Figure 4 shows top schematic view of dual metal gate FinFET. Effective gate length is 32nm. Along the length of gate (X) nm molybdenum is deposited and in remaining (32-X) nm length tungsten is deposited. Device has design and studied for different value of 'X'.

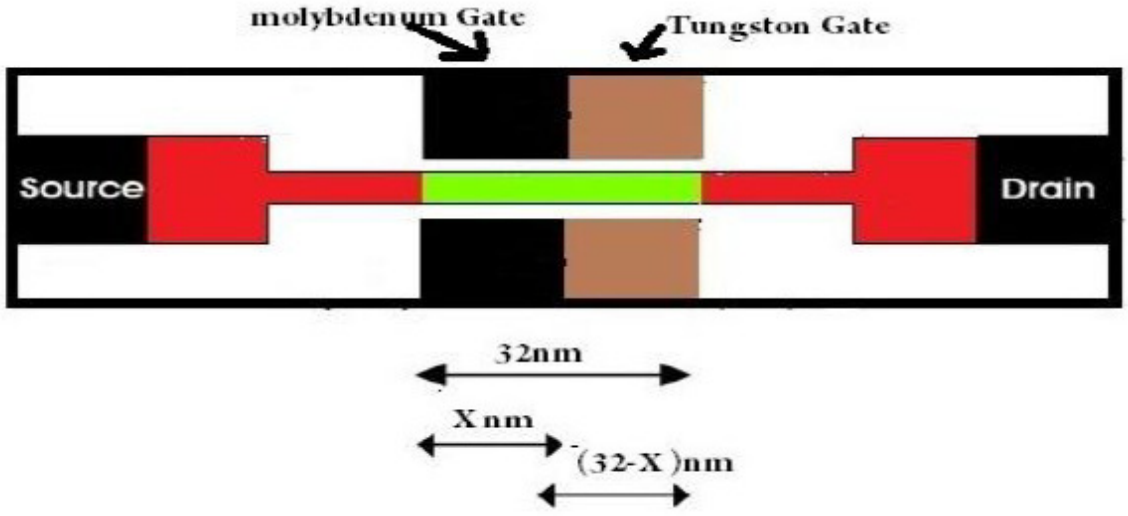
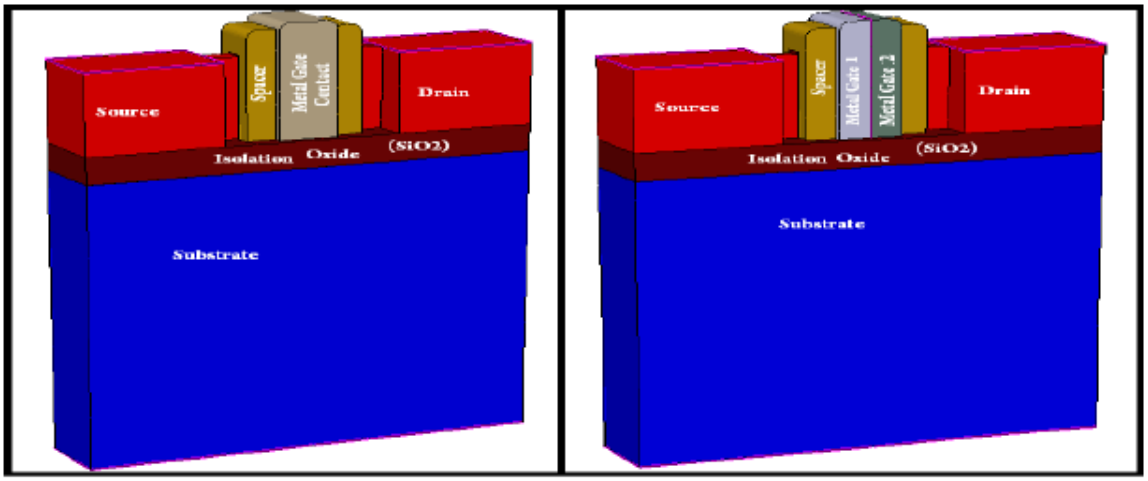


Figure 4 Top view of Dual Metal Gate FinFET

Table 1. Device specifications

Parameters	Value	Parameters	Value
Lg(Gate length)	32nm	V_{DD}	1V
W_{FIN} (Fin width)	10nm	Channel doping	$1x10^{18}$ cm^{-3}
H_{FIN} (Fin hight)	60nm	DRAINS/SOURCE DOPING	$1x10^{20}$ cm^{-3}
T_{OX} (gate oxide thickness)	1.1nm	Gate oxide	SiO2
Spacer length	16nm	N- type dopant	Phosphorus
SiO2 thickness (SOI Isolation oxide)	20nm	P- type dopant	Boron
Spacer material	Si3N4	Gate contact material	Metal



(a)3-D view of simulated SOI FinFET (b) 3-D view of simulated Dual Metal Gate FinFET

Figure 5 3-D views of SOI FinFET and Dual Metal Gate FinFET

3. DEVICE SIMULATION AND RESULTS

3.1. Tri gate FinFET

The device diagram of tri-gate FinFET has been shown in Figure 5, transfer characteristics of FinFET has been shown in Figure 6 and subthreshold characteristics of FinFET has also been shown in Figure 8.The threshold voltage variation has been shown in Figure 7 for different values of gate barrier. The threshold voltage of an n-channel MOSFET is classically given [11] by

$$V_{th} = \phi_{MS} - \frac{Q_{ss}}{C_{ox}} + 2\phi_F + \frac{qN_a x_{d\max}}{C_{ox}}$$

Where ϕms is the workfunction difference between the gate and the silicon and called it as gate barrier. The Barrier specification in the gate definition defines the workfunction difference between the metal and an intrinsic reference semiconductor. Relation between gate barrier and ϕms is given by following equations [11], [12]

$$\Phi ms = \phi m-(\phi si-\phi f)$$

$$\Phi ms = \phi m-\phi si+\phi f$$

$$\Phi ms = Gatebarrier+\phi f$$

Above equations clearly indicate the dependence of threshold voltage on gate barrier. For higher threshold voltage the value of barrier should be high. A wide range of threshold voltage can be achieved by varying gate barrier. The threshold voltage of device is found to be higher for high barrier. Table 2 contains values of threshold voltages and subthreshold slope for different gate barrier voltages.

Table 2.

Gate barrier (V)	Threshold voltage (V)	Subthreshold Slope (mV/dec)
-0.2	-0.217	63.19
-0.1	-0.124	62.71
0.0	-0.025	62.49
0.1	0.092	62.51
0.2	0.199	62.22

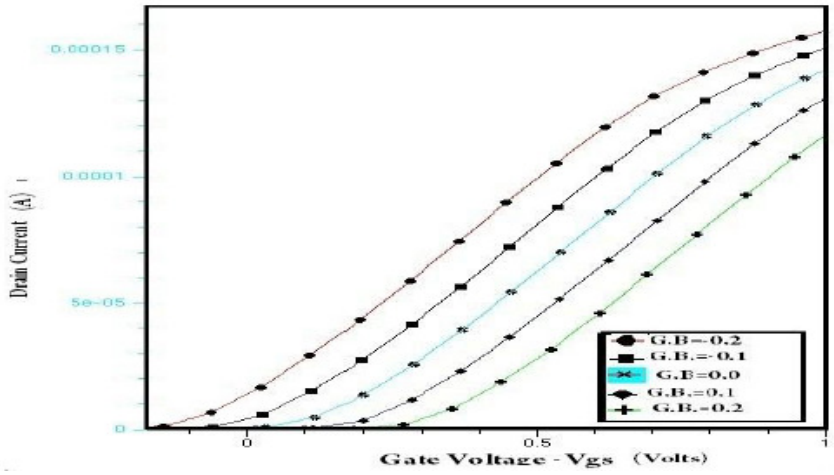


Figure 6 Transfer characteristics of TG-FinFET

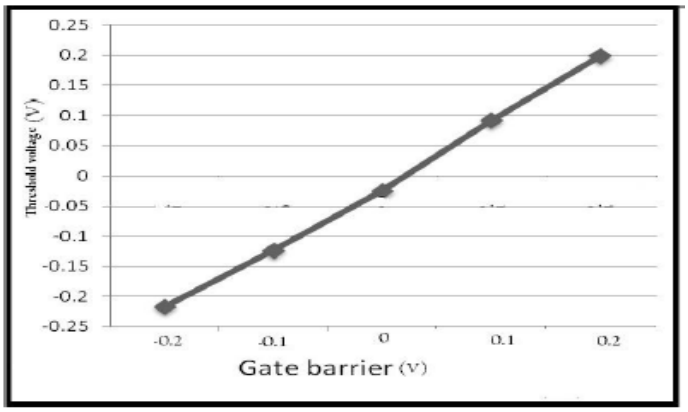


Figure 7 variation of threshold voltage in TG-FinFET with gate barrier

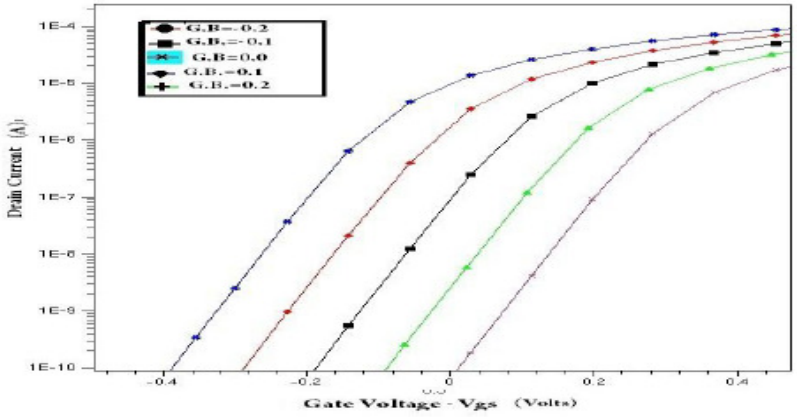


Figure 8 Subthreshold characteristics of TG-FinFET for different gate barriers

3.2. IG-FinFET

IG-FinFET structure is shown in Figure 2. Simulation of IG-FinFET has been done for various back gate voltages. Table 3 shows the value of threshold voltages and subthreshold slopes for different back gate voltages. Figure 9 shows transfer characteristics of IG-FinFET for different back gate voltages and Figure 11 shows transfer characteristics of IG-FinFET.

Table 3

Back gate voltage(V)	Vth (V)	SS(mV/decade)
-0.3	0.304	85.85
-0.2	0.049	115.48
-0.1	0.020	142.22
0	-0.048	211
0.1	-0.319	298
0.2	-0.412	438

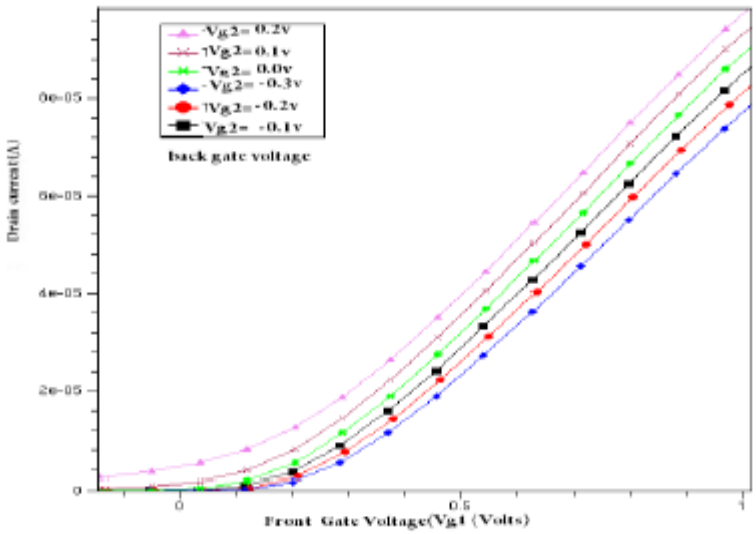


Figure 9 Id-Vg1 curve of IG-FinFET for different back gate voltages

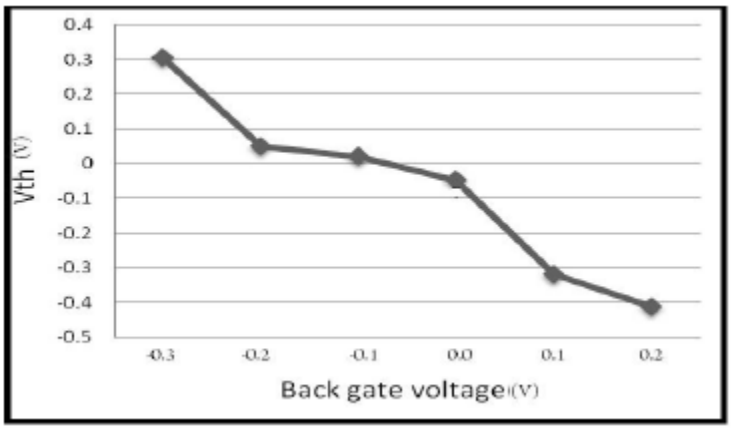


Figure 10 variation in Vt in IG-FinFET w.r.t. Back gate bias (Vg2)

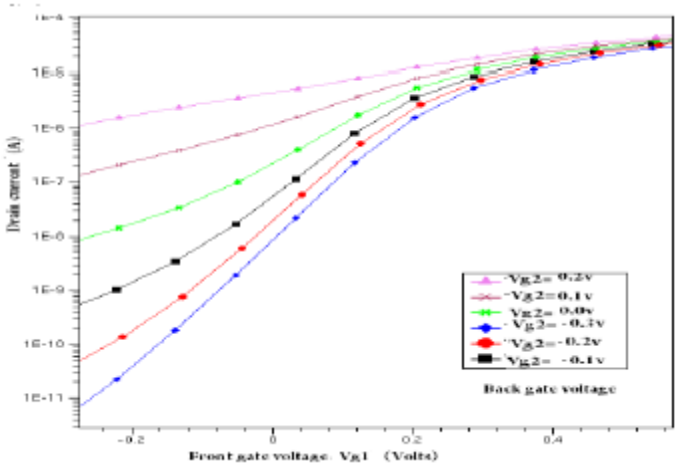


Figure 11 Subthreshold characteristics of IG-FinFET

3.3. IG-FinFET with connected gate (DG-FinFET)

If both gates of IG-FinFET are electrically connected it will work as dual gate FinFET. Table 4 shows the performance of IG-FinFET in connected gate mode of operation. Both gates are considered identical.

Table 4

Gate Barrier (V)	Threshold voltage(volt)	SS(mV/decade)
-0.2	-0.231	64.89
-0.1	-0.139	64.10
0.0	-0.047	64.20
0.1	0.045	63.98
0.2	0.149	64.18

Figure 12 and 13 shows comparison between FinFET‟s IG, DG and TG mode of operations. It is found that performance of TG-FinFET is better than IG and DG mode of operation. This is because TG-mode provides better control of gate over the channel.

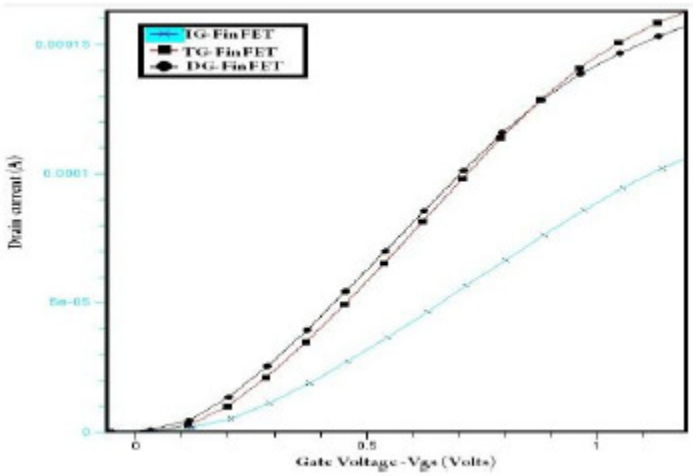


Figure 12 comparisons of transfer characteristic of IG, DG & TG FinFETs

While comparing IG, TG and DG mode, gate barriers is considered to be zero. In IG-FinFET back voltage is zero. It is apparent from Figure 13 that subthreshold performance of TG-FinFET and DG-FinFET is much better than IG-FinFET.

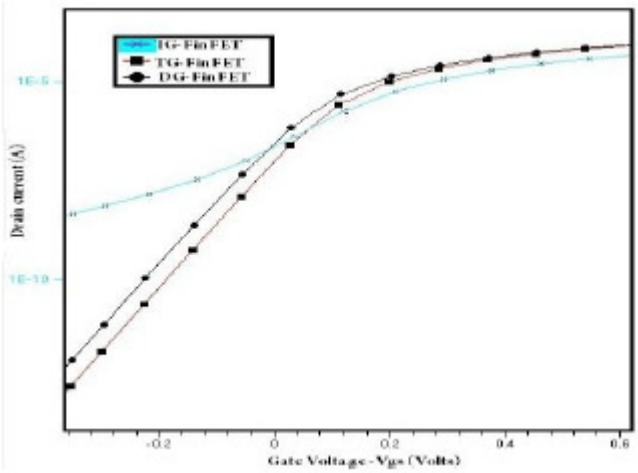


Fig 13 comparisons of subthreshold characteristic of IG, DG & TG FinFETs

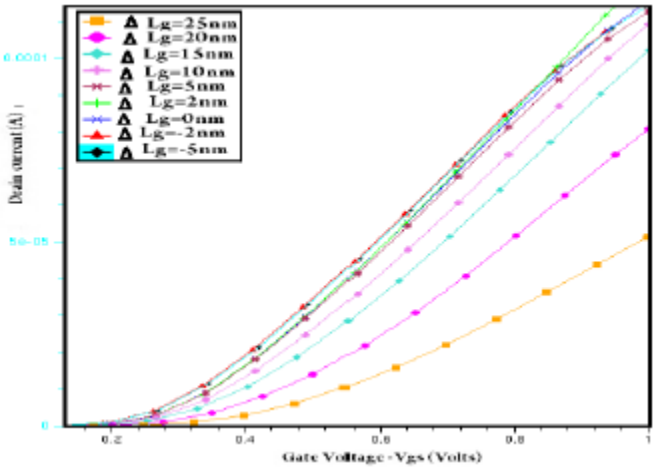


Figure 14 Id-Vg plots for different values of ΔLg

3.4. Extended channel

Channel lapping stands for extension of channel towards drain and source regions. Channel lapping is represented by parameter ΔLg. Here ΔLg shows how much channel is extended towards drain/source. Negative value of ΔLg shows negative channel lapping means extension of drain and source in channel table 5 shows device performance for different value of ΔLg.

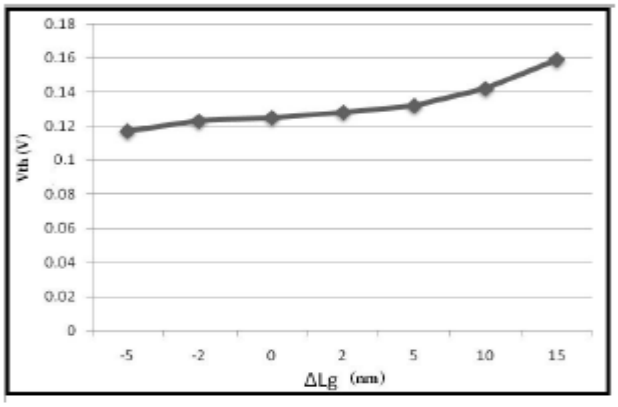


Figure 15- variation in threshold voltage with respect to ΔLg

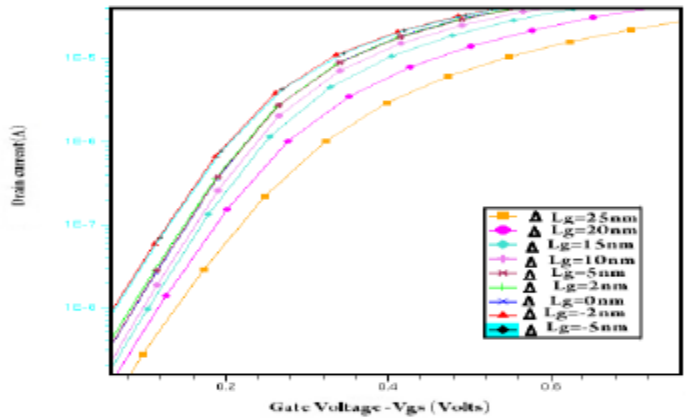


Figure 16 Subthreshold characteristics of FinFET for different value of ΔLg

Table 5

ΔLg (nm)	Vt (V)	SS(mV/dec)	DIBL(mV/V)	Ion (mA)	Ioff(nA)
-5	0.117	62.17	19.05	0.11473	1.1062
-2	0.123	62.99	20.35	0.1145	0.9571
0	0.125	63.47	17.18	0.1194	0.8556
2	0.128	62.90	16.97	0.1227	0.4770
5	0.132	62.53	17.90	0.1129	0.4061
10	0.142	61.75	17.81	0.1093	0.2537
15	0.159	62.05	16.69	0.1024	0.2107
20	0.173	63.07	17.82	0.0807	0.1469
25	0.200	66.61	26.48	0.0516	0.0928

3.4. Dual-Metal gate FinFET

Schematic top view of dual metal gate (DMG) FinFET is shown in fig4. A transfer characteristic of DMG FinFET is shown in Figure 14.

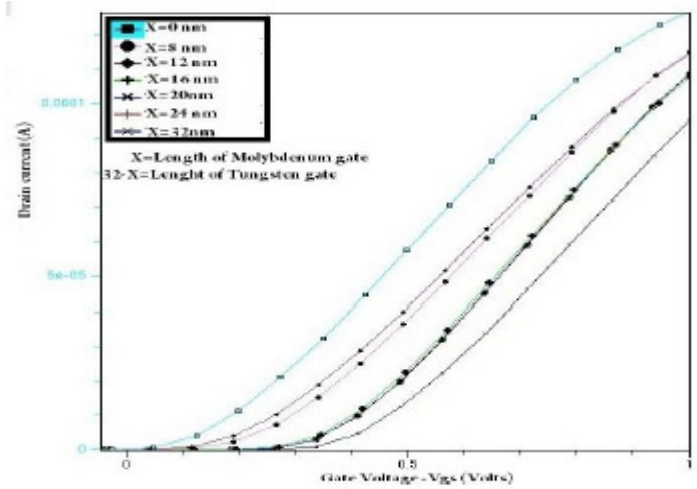


Figure 17 Id-Vg curve of DMG FinFET

Here X is the length of molybdenum gate and 32-X is length of tungsten gate. 32nm is total gate length. Graph clearly indicates that we can vary threshold voltage of FinFET by changing "X".

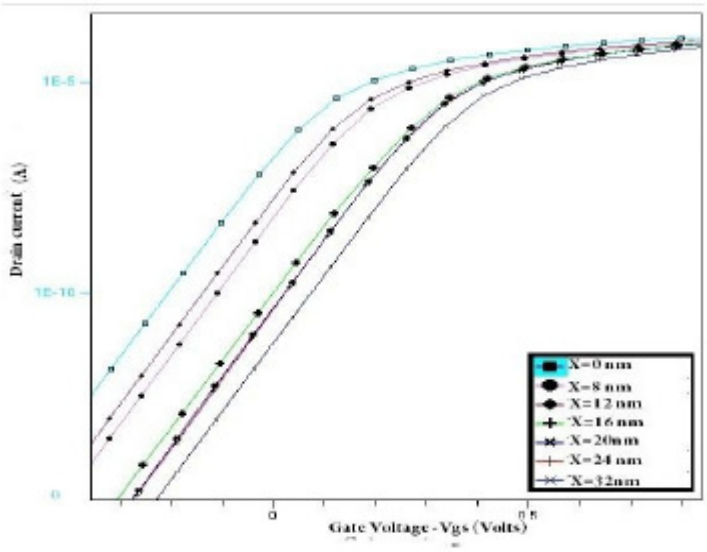


Figure 18 Subthreshold characteristics of DMG FinFET

Table 6

Total gate length (nm)	X molyb denm length (nm)	32-X tungst en length (nm)	Vth(V)	SS (mV/ dec)	DIBL (mv/V)	I_{OFF}	I_{ON}(mA)
32nm	32	0	0.263	62.02	25.01	6.08 pA	0.0954
32nm	24	8	0.1949	61.26	32.97	41.9pA	0.1087
32nm	20	12	0.1958	61.41	33.71	45pA	0.1083
32nm	16	16	0.1955	63.48	67.59	0.103nA	0.1080
32nm	12	20	0.0439	65.50	63.78	16.38nA	0.1146
32nm	8	24	0.0582	61.80	55.03	5931nA	0.1151
32nm	0	32	-0.0226	63.26	24.37	0.1547uA	0.12688

4. CONCLUSION & DISCUSSION

IG-FinFET provides a simple way for variable threshold voltage. It is also possible in IG-FinFET to vary the threshold voltage during the operation, by applying DC bias we got a good range of threshold voltages. Single IG-FinFET can also used as two parallel transistor hence with IG-mode of operation we may have a wide range of threshold voltage as well as significant area efficiency. But there are some drawbacks while using FinFET in IG configurations. While using back gate for threshold voltage control there is only one active gate in IG-FinFET. IG-FinFET shows very low subthreshold performance and very low on current. Figure 12 shows the comparison of IG-FinFET and TG FinFET transfer characteristics, and it clearly indicates that the value of on current of IG-FinFET is lower as compare to TG mode of operation .From Figure 13 we can conclude that IG-FinFET has less control of gate over channel than TG FinFET and DG-FinFET.

Our goal is to vary threshold voltage of FinFET without varying its other characteristics like subthreshold slope, DIBL etc. Channel lapping technique discussed here has provided a wide range of threshold voltage without effecting its SS and DIBL. But effective length of channel is changed and due to high lapping capacitance it is not a good technique.

It is apparent in this work that best way of controlling threshold voltage of FinFET is by changing its gate‟s workfunction. For long channel MOSFETs polysilicon is used as gate materials. It is very easy to change workfunction of polysillicon by changing its doping. But for short channel a metal gate electrode has several advantages compared to the doped polysilicon [14] gate used almost exclusively today. Gate capacitance degradation due to the depletion of the doped polysilicon gate typically accounts for 0.4 – 0.5 nm of the equivalent-oxide thickness of the total gate capacitance at inversion. This is a substantial amount, considering that a gate equivalent oxide of less than 1.5 nm. High k dielectrics are thermally unstable. Fabrication of MOSFET with high k dielectric required low thermal budget process. Polysilicon gate required high temperature processing so it cannot be used when high k dielectrics are used as gate insulator. Moreover the workfunction variation of polysilicon gate technology is limited to values close to the conduction band and the valence band of silicon. The use of a metal gate material opens up the opportunity to

choose the work function of the gate and redesign the device to achieve the best combination of work function and channel doping.

In this work we aligned different metals for formation of gate contact. Results are shown in Figure 17-18. It is found that this alignment of metals not only provides a good range of threshold voltages but gives better performance also. Values of subthreshold slope and DIBL are nearly identical in all combinations. Different threshold voltage schemes are systematically investigated using extensive device simulations with optimized TCAD tools. This paper shows that after careful optimization FinFETs offer a desirable threshold voltage and use of FinFET in multiple threshold voltage circuits will offer future low-power high-performance applications.

REFERENCES

[1] H.-S. P. Wong (2002) “Beyond the conventional transistor” IBM J. RES. & DEV. VOL. 46 NO. 2/3 March/May.

[2] D. Hisamoto, L. Wen-Chin, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, K. Tsu-Jae, J. Bokor, and H. Chenming, (2000) "FinFET – a self-aligned double-gate MOSFET scalable to 20 nm," IEEE Trans. Electron Devices, vol. 47, pp. 2320-2325.

[3] Tsividis “Operation and Modeling of the MOS Transistor” Oxford University Press 2nd edition.

[4] “Sentaurus Structure Editor User˝s Manual”, by Sentaurus TCAD.

[5] “Sentaurus device manual”, Sentaurus TCAD, http:// www.synopsys.com.

[6] Masoud Rostami and Kartik Mohanram (2010) “Novel dual-Vth independent-gate FinFET circuits” Digital Object Identifier: 10.1109/ASPDAC.2010.5419680, Page(s): 867 – 872.

[7] Igor Polishchuk, Pushkar Ranade (2002) “Dual Work Function Metal Gate CMOS Transistors by Ni–Ti Interdiffusion” IEEE ELECTRON DEVICE LETTERS, VOL. 23, NO. 4.

[8] Q. Lu, R. Lin, P. Ranade, T.-J. King, and C. Hu, (2001) “Metal Gate Workfunction Adjustment for Future CMOS Technology,” Symposium on VLSI Technology, Digest of Technical Papers, pp. 45–46.

[9] D. Frank, Y. Taur, M. Ieong, and H.-S. Wong, (1999) “Monte Carlo modeling of threshold variation due to dopant fluctuations,” in Proc. Symp. VLSI Technol., pp. 169–170

[10] A. Muttreja, N. Agarwal, and N. K. Jha, (2007) “CMOS logic design with independent gate FinFETs,” in Proc. Int. Conf. Computer Design, Oct., pp. 560–567.

[11] Ben G. Streetman “Solid State Electronics Devices” sixth edition

[12] Y. Taur and T. H. Ning, (1998) Fundamentals of Modern VLSI Devices.Cambridge, U.K.: Cambridge Univ. Press,.

[13] Masoud Rostami, and Kartik Mohanram (2011) “Dual-Vth Independent-Gate FinFETs for Low Power Logic Circuits” IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, VOL. 30, NO. 3.

[14] Chang-Hoon Choi, P. R. Chidambaram, Rajesh Khamankar (2002) "Gate Length Dependent Polysilicon Depletion Effects" IEEE ELECTRON DEVICE LETTERS, VOL. 23, NO. 4.

[15] J. P. Colinge, (2007) FinFETs and other Multi-Gate Transistors Springer.

Authors

V. Narendar - Received the B.Tech. degree in Electronics and Communication from SVEC-Suryapet-A.P., India, in 2006 and the M.Tech. degree in microelectronics and VLSI design in 2010 from the MNNNIT Allahabad, India, where he is working as an assistant professor in SMDP-II Project and currently working toward Ph.D. degree in Electronics and communication Engg, with "Device Modeling and VLSI Circuits" as the area of specialization.

Ramanuj Mishra- received the B.E. Degree in Electronics and Communication from RGPV in 2009 Bhopal, India. And currently working towards M.Tech in microelectronics and VLSI design from MNNNIT Allahabad, Allahabad, His current research interests include of Short channel devices such as FinFETs

Nayana R- she is working towards M. Tech Degree in microelectronics and VLSI design from MNNIT Allahabad, Allahabad, and Her area of interest is low power CMOS design.

Sanjeev Rai- He is an assistant Professor in MNNIT Allahabad. His areas of interest are Microelectronics & VLSI Design, Modeling of Semiconductor Devices, and VLSI Circuits & Systems

Dr. R. A. Mishra : He is an assistant Prof. in MNNIT Allahabad. His areas of research are VLSI Circuits, Modeling of Semiconductor, Devices RNS based Circuits Design