Design of Near-Threshold CMOS Logic Gates

N. Geetha Rani[1], N. Praveen Kumar[2], Dr. B. Dr. B. Stephen Charles [3]
Dr. P. Chandrasekhar Reddy [4] S.Md.Imran Ali [5]

[1]Assistant Professor, ECE Department, Stanley Stephen College of Engineering & Technology, Kurnool, A.P., India
[2]Assistant Professor, ECE Department, Stanley Stephen College of Engineering & Technology, Kurnool, A.P., India
[3]Professor, ECE Department, Stanley Stephen College of Engineering & Technology, Kurnool, A.P., India [4]Professor, ECE Department, JNTUH College of Engineering, Hyderabad, A.P., India
[5] Assistant Professor, ECE Department, Stanley Stephen College of Engineering & Technology, Kurnool, A.P., India

ABSTRACT

Numerous efforts have made to balance the tradeoff between power consumption, area and speed of a design. While studying the design at the two extreme ends of the design spectrum, namely the ultra-low power with acceptable performance at one end and high performance with power within limit at the other has not made. One solution to achieve the ultra-low power consumption is to operate the design in sub-threshold region. The use of sub-threshold circuit designing in fast and energy efficient circuits is always needed in electronics industry especially in DSP, image processing and arithmetic units in microprocessors, where the low power is the primary concern and the delay can be tolerated. We design a simple CMOS inverter in weak inversion region (sub-threshold) and compare the power consumption with strong inversion region using Cadence 0.18µm Technology.

KEYWORDS:

Ultra low power, Sub-Threshold Region, CMOS

1. INTRODUCTION

Extreme CMOS scaling results in low threshold voltage and very thin oxide thickness for transistors manufactured in nanometer regime. As a result, reducing the sub-threshold leakage current and tunneling gate leakage currents has become one of the most important factor in the design of VLSI circuits. Scaling of CMOS circuits beyond the 65-nm technology node requires not only low threshold voltages to maintain the device switching speeds, but also ultra-thin gate oxides to maintain the current drive and keep threshold voltage variations under control when dealing with short-channel effects [1]. Low threshold voltage for a MOSFET results in an exponential increase in the sub-threshold leakage current, whereas ultra-thin gate oxide results in exponential increase in the tunneling gate leakage current. As leakage power dissipation gets increased, the area of the circuit increases in proportional. Since in many processors, caches

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memory occupies about 50% of the chip area [2]. The leakage power of caches memory is one of the major sources of power consumption in high performance microprocessors. One way of reducing the sub-threshold leakage is to use higher threshold voltage MOSFET's in some parts of a design. While the tunneling gate leakage can be reduced by using high-dielectrics or multiple gate oxides in the design.

2. OVERVIEW OF TOTAL POWER CONSUMPTION

The total power in a CMOS circuit is given by Equation

$$P_{Total}=P_{dynamic}+P_{static}$$

$$P_{Total}=1/2\ C_L V_{dd}^2 \alpha f+I_{sc} v_{dd}+I_{static} V_{dd} \quad (1)$$

Where C_L is the load capacitance, f is the frequency of operation I_{SC} is the short circuit current and α is the activity factor. As can be seen from Equation (1) the total power consists of two major components: dynamic power and leakage power. Both these components reduce in magnitude as the supply voltage reduces.

The dynamic power consumption is mainly due to the charging and dis-charging of the capacitance and short circuit current. A short circuit current flows when the pull up and pull down networks in a CMOS circuit are simultaneously on and a direct path exists between the supply line and ground. Dynamic power is directly proportional to the square of the supply voltage. Therefore, dynamic power reduces in a quadratic manner when the supply voltage is reduced. Leakage power is dependent on the leakage current flowing in the CMOS circuit.

At super-threshold, the charging (or discharging) current is greater than the leakage current. Hence, dynamic power dominates over leakage power in super-threshold. At sub-threshold, the applied supply voltage is lower than the threshold voltage of the MOSFET. Due to its quadratic relation with supply voltage, dynamic power reduces drastically in sub-threshold. Also, leakage current is regarded as the conduction current in sub-threshold. Therefore, leakage power dominates than dynamic power in the sub-threshold region of operation [8].

3. LEAKAGE CURRENT COMPONENTS

The leakage current of a CMOS transistor consists of three major components

1. Junction tunneling current
2. Sub-threshold current and
3. Tunneling gate current

3.1 TUNNELING JUNCTION LEAKAGE CURRENT

In MOSFET, p-n junction gets formed in between regions of drain-body and source to body. Usually when diode is in reverse bias a small amount of reverse leakage current flows due to diffusion of minority carriers near the junction. Since this current is very small we can neglect it.

3.2 SUB-THRESHOLD LEAKAGE CURRENT

Sub threshold leakage is the current that flows in between drain to source of a MOSFET when the gate to source voltage is lower than the threshold voltage. The sub threshold leakage is modeled as

$$I_{sub}=A_{sub}\exp\left(q/\, n_1KT(V_{GS}-v_{to}-\gamma^1 V_{SB}+\eta V_{DS})\right)*(1-\exp(-q/KTV_{DS})) \qquad (2)$$

Where $A_{sub}=\mu_0 C_o W/L_{eff}$ $(KT/q)2\ e^{1.8}$, $\mu 0$ is the zero bias mobility, Co is the gate oxide capacitance per unit area, and W denote the width and L_{eff} effective length of the transistor, K is the Boltzmann constant, T is the absolute temperature, and q is the electrical charge of an electron. In addition, v_{t0} is the zero biased threshold voltage, $\gamma 1$ is the body-effect coefficient, η denotes the drain-induced barrier lowering (DIBL) coefficient, and n_1 is the sub threshold swing coefficient of the MOSFET.

3.3 TUNNELING GATE LEAKAGE CURRENT

Electron tunneling from the conduction band, which is only significant in the accumulation region, results in direct tunneling gate leakage current in NMOS transistors. In PMOS transistors, on the other hand, hole tunneling from the valence band results in the tunneling gate leakage current.

The tunneling gate current is composed of three main components:

1. gate-to-source and gate-to-drain overlap current
2. gate-to-channel current, part of which goes to the source while the remainder goes to the drain
3. gate-to-substrate current.

In CMOS technology, the leakage current flowing from gate to substrate is several orders of magnitude lower than the overlap tunneling and gate-to-channel current, while the overlap tunneling current dominates the gate leakage in the OFF state, gate-to-channel tunneling dominates the gate current in the ON state. Since the gate-to-source and gate-to-drain overlap regions are much smaller than the channel region, the tunneling gate current in the OFF state is much smaller than that in the ON state [6]. If silicon di-oxide is used for the gate oxide, PMOS transistors will have about one order of magnitude smaller gate leakage than NMOS transistors. Therefore, one may conclude that the major source of tunneling gate leakage in CMOS circuits is the gate-to-channel tunneling current of the ON NMOS transistors which can be modeled as [7]

$$J_{tunnel} = 4\pi m^*q/h_3(KT)^2(1+\gamma KT/2\sqrt{EB})^* \exp(E_F/KT-\gamma\sqrt{EB}) \qquad (3)$$

Where m*(=0.19Mo) is the electron transfer mass and Mo is the electron rest mass. More over, h is Planck's constant, E_F is the Fermi level at the Si/SiO2 interface, is the height of barrier, and γ is defined a

$$\gamma = 4\pi T_{ox}\ \sqrt{2m_{ox}} / h \qquad (4)$$

Where m_{ox}(=0.32Mo) is the effective electron mass in the oxide.

4. OVERVIEW OF SUBTHRESHOLD CIRCUIT DESIGN

The MOS (Metal Oxide Semiconductor) transistor conducts current, majority carriers, through an inverted channel between the source and drain caused by a nominal voltage applied to the gate. When a low voltage is applied to the gate, majority carriers in the substrate are repelled from the surface directly below the gate. Then, a depletion charge of immobile atom forms a depletion region beneath the gate. The minority carriers in the depletion layer are made to move by diffusion and induce a drain current by applying a voltage between the drain and source in the MOS device. This weak inversion current was considered to be insignificantly small and ignored in digital circuit design until the recent decade. As is relevant to the electronic wrist watch design [9, 10], the properties of MOS transistors have been investigated at a very low current level. The study uncovered an unusual exponential relationship of the drain current with the gate voltage. Figure 4.1shows the first measurement of drain current of an MOS transistor below the device threshold voltage. This weak inversion current has been named the sub-threshold current.

The conduction region of a transistor depends on the supply voltage at which it operates. As the supply voltage is reduced, the region of operation shifts from strong inversion to moderate inversion and finally to weak inversion. The strong inversion region, also known as the super-threshold regime, is characterized by large current drives and a supply voltage substantially above V_{th}, the threshold voltage of the transistor. The moderate inversion has lower current drives as compared to the super-threshold regime and an operating voltage near to the V_{th}. The weak inversion region, also known as the sub-threshold region, is characterized by small current drives and a supply voltage below V_{th} [16].

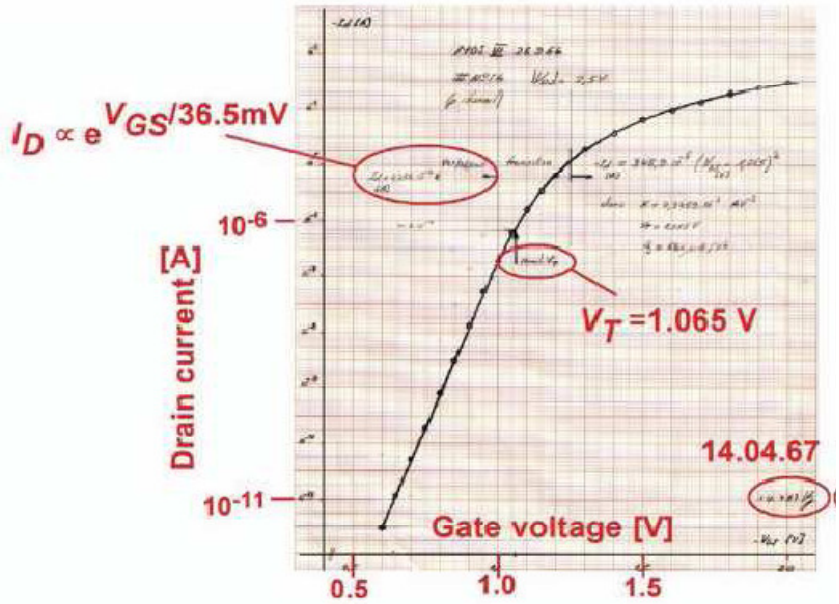

Figure 4.1: First measurement of an MOS transistor at very low current (annotated copy of Vittoz's note book [10]).

4.1 SUBTHRESHOLD LEAKAGE CURRENT MODELS

Sub-threshold conduction current can be expressed by the following basic equation

$$I_{on\text{-}sub} = Io \exp (V_{gs}-V_{th}/\eta V_T) \quad (5)$$

Where I_o is the drain current when $V_{gs}=V_{th}$ given below

$$I_o = \mu_{eff} C_{ox} (W/L_{eff})(\eta-1)V^2_T \quad (6)$$

Where W is the width of the transistor, L_{eff} is the effective length, μ_{eff} is the effective mobility, C_{ox} is the oxide capacitance, η is the sub-threshold slope factor ($\eta=1+[C_d/C_{ox}]$).V_{th} is the transistor threshold voltage and V_T is the thermal voltage $V_T =(kT/q)$. As expected for diffusion current, equation (5) shows that $I_{on\text{-}sub}$ depends exponentially on V_{gs}

As it is clear that the transistor current $I_{on\text{-}sub}$ in the sub-threshold region is exponentially dependent on V_{th} and supply voltage V_{dd} due to which power, delay and current matching between two transistors is also exponentially dependent on V_{th} and V_{dd} . This exponential dependence is a key challenge in designing circuits in sub-threshold. Some of the parameters that are affected by this challenge are process variations, noise margins, soft errors and output voltage swings. Therefore, when designing energy optimal sub-threshold circuits, these parameters play an important role.

The current in the sub-threshold region, also known as leakage current, is considered to be undesirable when operating the transistor in the super-threshold region. However, this current is quintessential as far as sub-threshold operation is concerned. Leakage current is utilized by sub-threshold circuits as their conduction current [24].

4.2 MINIMUM OPERATING VOLTAGE

For the correct functional operation of a sub-threshold logic circuit, the supply voltage V_{dd} should be higher than a certain minimum voltage (V_{min}). For bulk CMOS technology, the theoretical V_{min} is given as [19, 20],

$$V_{min}=2V_T \ln\left(1+\frac{S}{\ln 10.\ VT}\right) \quad (7)$$

Where V_T = kT/q is the thermal voltage, k = 1.381 × 10−23 J/K is Boltzmann's constant, T is absolute temperature in Kelvin, q = 1.602 × 10−19 C is electronic charge and S is the sub-threshold swing. From [21], S is degraded with the down-scaling trend of CMOS technology, which means that the reduced ratio of on-current Ion at $V_{gs}=V_{ds}=V_{dd}$ to off-current I_{off} at $V_{gs}=0$ and $V_{ds}=V_{dd}$ in sub-threshold region ($V_{dd}<V_{th}$) causes smaller noise margins and possible functional logic failures at or below V_{min}.

4.3 DELAY

The delay of a gate in a sub-threshold circuit can be simply formulated from the CMOS gate delay equation [21],

$$t_d = K.C_L V_{dd}/I_{on} \quad (8)$$

Where K is a fitting parameter and C_L is the load capacitance of the gate. If it is assumed that total sub-threshold current is equal to sub-threshold drain current (I_{sub}), we replace I_{on} with I_{sub} [22]

$$I_{sub}=I_0\ 10^{(Vgs-Vth+\eta Vds)/S}.(1-e^{-Vds/VT}) \quad (9)$$

Where η is the drain-induced barrier lowering (DIBL) coefficient and Io is the drain current at $V_{gs} = V_{th}$ in the weak inversion [23].

$$I_0= \mu_0 C_{ox}\frac{W}{L}(m-1)\ V_T^2 \quad (10)$$

Where μ_o is the zero bias electron mobility, C_{ox} is the oxide capacitance, and m is the sub-threshold slope coefficient. When $V_{gs} = V_{ds} = V_{dd} >> V_T$ (≈ 26mV at 300K), we get gate delay as,

$$T_d= (K.C_L V_{dd}) / [I_0\ 10^{[(\eta+1)Vdd-Vth]/S}\ ] \quad (11)$$

Thus, t_d is exponentially dependent on V_{dd}, V_{th},η,and S.

4.4 ENERGY

Energy per cycle of a circuit is a key parameter for energy efficiency in ultra-low power applications. Because computing workload is characterized in terms of clock cycles, this measure directly relates energy consumption to the workload. Before considering the energy consumed by a circuit, we start by examining the total energy per cycle (E_{tot}) of a single gate, which is composed of dynamic energy (E_{dyn}) and leakage energy (E_{leak}):

$$E_{dyn}=\alpha_{0\to1}.C_L.V_{dd}^2 \quad (12)$$

$$E_{leak}=P_{leak}.t_d = I_{off}.V_{dd}.t_d = K.C_L V_{dd}^2\ 10^{-Vdd/S} \quad (13)$$

Where I_{off}(Static leakage power)= $I_0\ 10^{(-Vth+\eta Vds)/S}$, $V_{ds}>>V_t$

$$E_{tot} = E_{dyn} + E_{leak}$$

$$E_{tot} = [\ \alpha_{0\to1} + K10^{-Vdd/S}\ ]\ C_L V_{dd}^2 \quad (14)$$

5. ADVANTAGES AND DRAWBACKS OF SUBTHRESHOLD OPERATION

The advantages of a circuit design approach that utilizes sub-threshold conduction are:

1. Power is significantly lower [17].
2. Device trans-conductance is an exponential function of V_{gs}, resulting in a high ratio of on to off current in a device stack. As a consequence, circuit noise margins are high.

3. Delay gets worse, but the overall PDP (Power-Delay Product) improves [17]. It has been shown [18] that we can obtain an improvement in the Energy-Delay product as well, by operating the circuit in the near-sub-threshold region.

The disadvantages of a sub-threshold design methodology are:

1. I_D exhibits an exponential dependence on temperature, requiring circuitry to compensate for this effect.
2. I_D is highly dependent on process variations. For example, small changes in V_{th} result in large changes in I_D due to the exponential dependence of I_D on V_{th}. We therefore require circuitry to compensate for this effect as well.

6. RESULTS

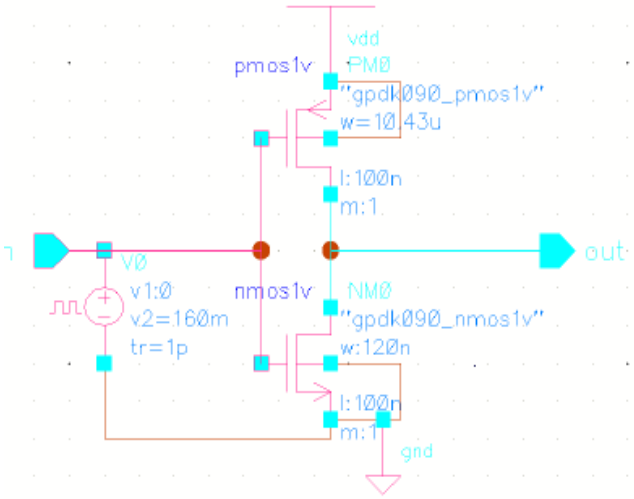

Figure1. Schematic of CMOS-Inverter

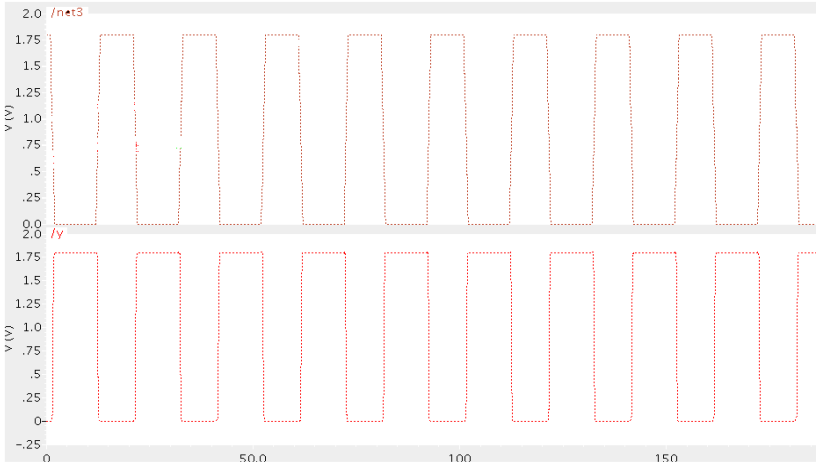

Figure2. Input and output waveforms of Inverter

Table1. Power Consumption and Delay of Inverter in Strong inversion and Sub-threshold Region

	Power Consumption	Delay
Strong Inversion Region	12.05 E-9W	10.1E-13
Sub-threshold Region	0.51 E-9 W	0.362E-12

7. CONCLUSION

In order to achieve ultra low power applications, circuits should be operated in near-threshold region .By this performance of the system will not be degraded. In this paper, we have operated the basic gate both in strong inversion region and in sub-threshold region. It is observed that the power consumption of the basic gate in sub-threshold region is very much less than in strong inversion region. The delay of the gate in sub-threshold is negligible compared to strong inversion operation.

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