CNFET BASED BASIC GATES AND A NOVEL FULL-ADDER CELL

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ABSTRACT

In this paper two novel high performance designs for AND and OR basic gates and a novel Full-Adder Cell are presented. These designs are based on carbon nanotube technology. In order to compare the proposed designs with previous ones both MOSFET based and CNFET based circuits are selected. By the way the proposed designs have better performance in comparison with previous designs in terms of speed, power consumption and power-delay product (PDP).

KEYWORDS

CNFET, MOSFET, Full-Adder cell, Basic gates.

1. INTRODUCTION

Serious Problems and limitations of CMOS technology scaling, have lead the designers to investigate the replacement candidates for future designs. Several materials are introduced and explored in ITRS reports as replacements of silicon channel and source/drain regions such as Ge, III-V compound semiconductors, nanowires, graphene nanoribbons and carbon nanotubes [1]. Carbon nanotube is one of the most promising technologies to replace the traditional CMOS technology [2-7]. This nano scale tube of graphine is used as channel of field effect transistors called CNFETs.

Since CNFETs show better performance in comparison with MOSFETs, most of the designers have designed their circuits based on this technology. One of the most important parts of each circuit is basic gates such as OR and AND gates. Also Full Adder Cell is an important part in microprocessors and digital signal processors. These circuits performance influences the whole arithmetic units. Therefore if we can design these circuits with higher speed and lower power consumption then we can increase the system performance.

In this paper we proposed new designs for basic gates and a Full Adder Cell based on CNFET technology. The rest of paper is organized as following. Section 2 presents a review of different types of CNFETs. Proposed circuits are analyzed in section 3. In section 4 the simulation results of these new circuits and comparisons with previous ones are presented. And finally, section 5 concludes the paper.

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2. CNFETs

Carbon nanotube (CNT) has been considered as one of the most important building blocks in nano devices. CNT is a sheet of graphite rolled into a tube with a diameter of a few nano meters. Since the discovery of CNT in 1991 by S. Iijima[8], significant applications of it have been demonstrated in different fields because of its specific characteristics. These excellent properties of CNT make them the most promising candidate for creating transistors on a scale smaller than can be achieved with silicon[9][10].

The way the graphite sheet is rolled is represented by a pair of indices (n,m) called a chiral vector. CNT with n-m=3 are metals, otherwise they are semiconductors[11]. One of the best applicable properties of CNT is ballistic transportation of electrons along the tube. therfore Semiconducting CNT can be used as channel for transistors[12].

CNFETs operate like traditional silicon transistors. Different types of CNFETs have been presented. One of them is Schottky Barrier CNTEF (SB-CNFET). These transistors are constructed with a semiconducting nanotube and two metallic contacts acting as source and drain; hence they have Schottky Barrier at the metal nanotube junction. In this type of CNFETs By changing the barrier height at the metal- semiconductor interface, gate modulates the injection of carriers in the nanotube[13]. Due to exhibit strong ambipolar characteristics, SB-CNFETs are suitable for using in CMOS logic families. Another type of CNFETs is MOSFET-like CNFET (MOS-CNFET) which exhibit unipolar behavior unlike SB-CNFET. In this MOSFET like device, the ungated portion (source and drain regions) is heavily doped and the CNTFET operates on the principle of barrier-height modulation by application of the gate potential. The conductivity of MOS-CNFETs is modulated by the gate-source bias. Both SB-CNFETs and MOS-CNFETs are used for high speed design because of their high ON current, however the other type of CNFET, band-to-band tunneling CNFET (T-CNFET) is utilized for ultra-low-power design on account of its low ON current and supper cutoff attributes [14].
CNFETs has a useful property that It will ease circuit designing and increase circuit's performance on the other hand, which is that the threshold voltage is proportional to the inverse of the diameter of the nanotube[14], as:

$$V_{TH} = \frac{0.42}{D_{CNT(nm)}} v \qquad (1)$$

$$D_{CNT} = \frac{\alpha \sqrt{N_1^2 + N_2^2 + N_1 N_2}}{\pi} \qquad (2)$$

This feature of CNFETs indicates that by changing the CNFETs diameters one can easily acquire different transistors with different turn on voltages.

3. PROPOSED DESIGNS

3.1. Basic Gates

Basic functions such as *AND*, *OR* and *Buffer* in CMOS technology are implemented by generating related inverted functions (e.g., NAND, NOR and NOT) followed by an inverter. Voltage threshold losing which occurred in passing high and low voltages in nMOSFET and pMOSFET, respectively results in such implementation.

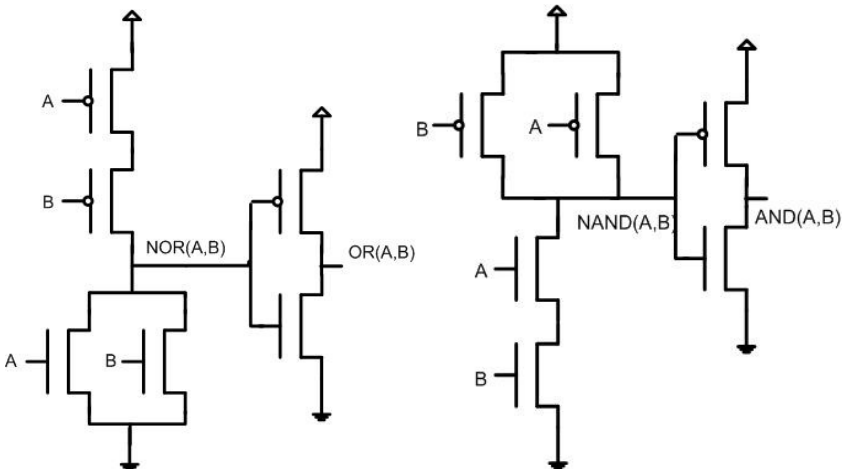

Figure 1 : AND(b) and OR(a) circuits in MOSFET

CNFET technology provides more efficient way to implement these functions in terms of Delay, Power consumption and Area. Such as explained before (see Eqn. 1), voltage threshold is proportional to the $1/D_{CNT}$ and it could be justified by manupulating N_1 and N_2, which (N_1,N_2) is chiral vector. So increasing the diagonal of nanotube (i.e., D_{CNT}) results in decreasing the voltage threshold toward zero. Consequently, pCNFET and nCNFET could be utilized in pull-down and pull-up network, respectively. This mechanism obviates voltage threshold losing in addition to removing inverter from critical path and less delay, area and PDP.

AND/OR circuits in CMOS technology include six transistors, whereas the number of transistors in our proposed CNFET based circuits reduce to four (Fig. 2). As it can be seen in Fig. 2, pCNFETs are used in pull-down network and nCNFETs are used in pull-up network. The threshold voltages of these transistors are almost zero. Hence no voltage dropping occurs in these circuits.

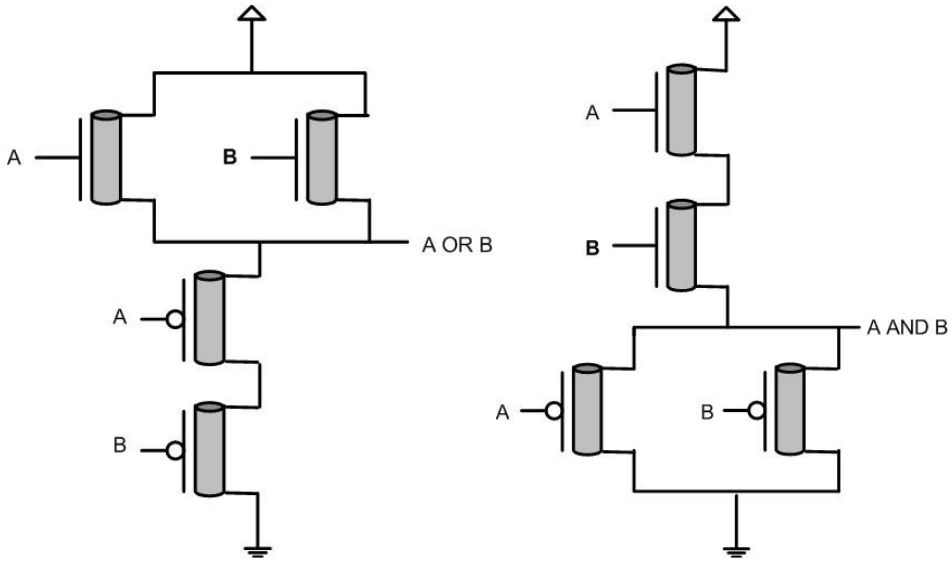

Figure 2 : Proposed Basic Gates(OR(a), AND(b)) Based on CNFET

3.2. Full-Adder Cell

In this section a new FA-cell (i.e., full adder cell) aka modified TGA are presented. The TGA Full Adder Cell is based on *XOR*/*XNOR* and transmission gates. Eqn. 3 and 4 describe how *sum* and *cout* signals are generated in TGA, respectively.

$$sum = (A \otimes B)C \vee (A \oplus B)\bar{C} \quad (3)$$

$$cout = (A \otimes B)A \vee (A \oplus B)C \quad (4)$$

Transmission gates are used in TGA to avoid the threshold voltage losing in output in cost of using more transistors (i.e., six transistors). Such as mentioned before, CNFETs adjust voltage threshold toward zero by increasing the diagonal of CNT. Consequently, transmission gates can be replaced by pass transistors.

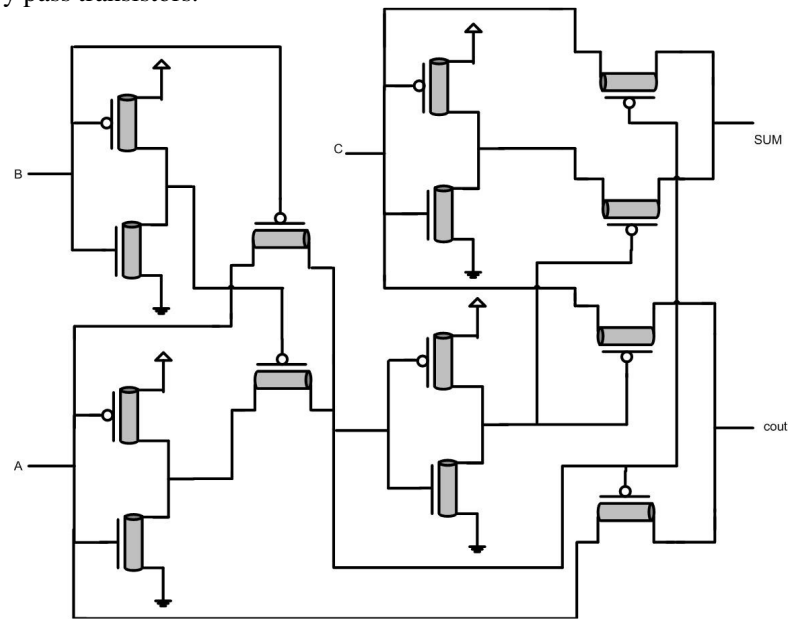

Figure 3 : First Step of Modified TGA

Such as seen in Fig. 3, the number of transistors in the modified TGA is 14 in comparison with the standard TGA that includes 20 transistors (i.e., six transistors reduction in modified TGA). In the next step by Substituting two pCNFETs by two nCNFETs obviates required inverter from the circuit for transforming *XOR* to *XNOR*. Details depict in Fig. 4.

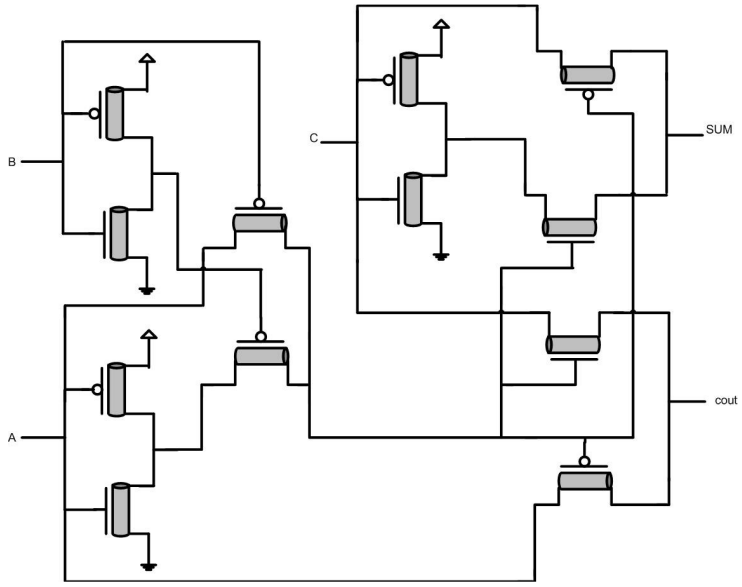

Figure 4 : Final Modified TGA

Consequently, final modified TGA includes 12 transistors. Therefore, the area consumption of proposed FA-cell (i.e., modified TGA full adder cell) is less than standard TGA full adder cell.

4. SIMULATION RESULTS

The HSPICE circuit simulator has been used to simulate both CMOS and CNFET based circuits. The MOSFET circuits are simulated using a 32n technology. A compact model of CNFETs presented in [14], [15] and [16] has been used for CNFET based circuits' simulation. In this model a MOS-CNFET device is implemented in three levels. In first level (CNFET_L1) the intrinsic behavior of MOS-CNFET has been modeled. In level 2 (CNFET_L2) the device non-idealities have been included and in the top level of this hierarchical modeling (CNFET_L3), multiple CNTs for each MOS_CNFET device are allowable.

The current sources and the trans-capacitance network are two main parts of the CNFET_L1. Semiconducting sub-bands current (I_{semi}), metallic sub-bands current (I_{metal}) and leakage current (I_{btbt}) are three current sources considered for CNFET model in [14] and [15]. These current sources are given by the following equations:

$$I_{semi}(V_{ch,DS}, V_{ch,GS}) \approx \frac{4e^2}{h}\sum_{m=1}^{M} {}_{k_m} T_m . \left[V_{ch,DS} + \frac{KT}{e} ln\left(\frac{1+e^{(E_{m,0}-\Delta\Phi_B)/KT}}{1+e^{(E_{m,0}-\Delta\Phi_B+eV_{ch,DS})/KT}}\right)\right] \quad (5)$$

$$I_{metal} = (1-m0)\frac{4e^2}{h} T_{metal} V_{ch,DS} \qquad \mu\iota\lambda \qquad (6)$$

$$I_{btbt} = \frac{4e^2}{h} KT . \sum_{m=1}^{M} {}_{k_m} \left[T_{btbt} ln\left(\frac{1+e^{(E_{m,0}-\Delta\Phi_B)/KT}}{1+e^{(E_{m,0}-\Delta\Phi_B+eV_{ch,DS})/KT}}\right) . \frac{\max(eV_{ch,DS}-2E_{m,0},0)}{eV_{ch,DS}-2E_{m,0}}\right] \quad (7)$$

In these equations K is the Boltzmann constant and T is the temperature in Kelvin. $V_{ch,DS}$ and $V_{ch,GS}$ symbolize the Fermi potential differences near source side within the channel. $\Delta\Phi_B$ is the channel surface potential change with gate/drain bias. $E_{m,l}$ denotes the carrier energy at the (m,l)sub-state above the intrinsic levelE_i, and $E_{m,0}$ is the half band gap of the m^{th}sub-band. T_m, T_{metal} and T_{btbt} are the transmission probability in each case.

Elastic scattering in the channel region, the quantum / series resistance and the parasitic capacitance of the doped source/drain region and the Schottky barrier resistance at the interface between the doped CNT and the source/drain metal contacts are the device non-idealities which CNFET_L2 models[14], [16]. In this paper CNFET_L3, the top level of this device model, is used for simulating the CNFET based circuits.

The comparison of DELAY, POWER and POWER-DELAY PRODUCT (PDP) of circuits is discussed below. The time from fifty percent of the input voltage swing to fifty percent of the output voltage swing is measured as delay.

4.1. Basic Gates Simulation Results

In this section, we report our analysis and compare proposed circuits with MOSFET and CNFET AND and OR gates. We remark that the design of CNFET gates (i.e., AND and OR) are similar to the MOSFET gates and obtained by replacing MOSFETs by CNFETs. The design of MOSFET based gates are described in details in section III.

The circuits are simulated at room temperature and the supply voltage is 0.9V for all of the circuits. For all circuits a *2.1 femto Farad* load capacitor has been used. Table.1 shows the delay, power and PDP of classical MOSFET and CNFET based and two novel CNFET based Basic Function circuits.

Table 1. Basic gates simulation results

Function	**Delay (e-11)**	**Power (e-8)**	**PDP (e-19)**
MOSFET-OR	5.141	20.26	104.16
CNFET-OR	1.736	7.78	13.51
Proposed-OR	1.757	3.30	5.804
MOSFET-AND	4.637	18.631	86.398
CNFET-AND	2.402	7.803	18.74
Proposed-AND	1.872	4.77	8.93

As it can be seen in the table.1 proposed OR is 322 and 1.11 times faster than OR MOSFET and OR CNFET respectively. And it consumes less power than two other designs, which it consumes146% and 42.4% power less than MOSFET and CNFET kinds, respectively. Therefore its PDP is better than two others.

The obtained speed up for AND circuit is 289% and 155% in comparison with AND MOSFET and CNFET, respectively. According to the power consumption factor, proposed AND circuit consumes 22.7% and 87% power less than MOSFET and CNFET AND, respectively. Consequently, the proposed AND circuit PDP is again better than the others.

In order to compare more precisely these designs are also simulated in 0.8V, 0.65V and 0.5V supply voltages. Results show that the proposed basic gates have better performance in all situations.

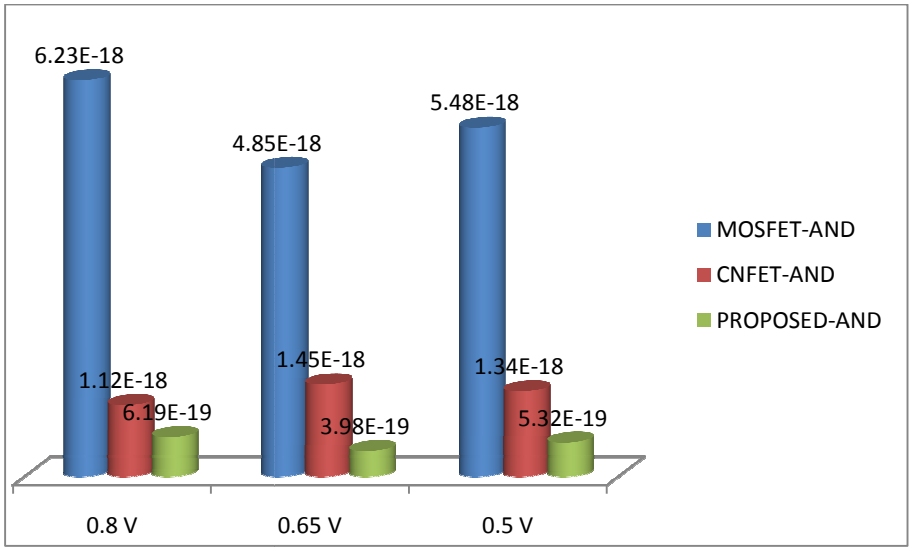

Figure 5 : PDP of AND gate in different supply voltages

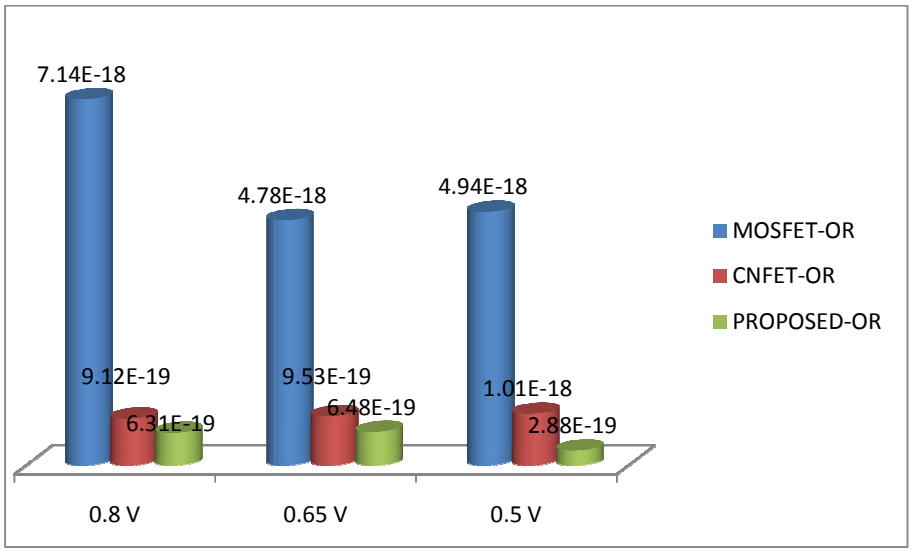

Figure 6 : PDP of OR gate in different supply voltages

4.2. Full-Adder Cell Simulation Results

We compare our proposed Full Adder Cell with 5 traditional Full Adder Cells(C-CMOS[17], TGA[18], CPL[19], CNTFA1[20] and CNTFA2[21]). For all circuits supply voltage is *0.8V* and *load capacitor* is 4.9 *femto Farad*. Table.2 shows the delay, power and PDP of traditional MOSFET based and CNFET based circuits and the novel CNFET based Full Adder circuit. As it shown in this table, the smallest delay belongs to the proposed design. It is 17.5 times faster than TGA which has the best delay among other full adders. Although proposed Full Adder design is best in term of speed and its average power dissipation is less than others. It consumes 33.7% less power than the CNTFA2. Its power dissipation is 22.5% and 20.5% less than CNTFA1 and TGA. As it considered from the table.2 the proposed design has the best PDP in comparison with the other full adders. Simulation results in different supply voltages are shown figure 7. as it shown in this figure the proposed Full-Adder cell has the best performance in different situations.

Table 1. Full-Adder Cells simulation results

Design	Delay (e-12)	Power (e-7)	PDP (-18)
C-CMOS	123.05	20.90	257.24
TGA	87.92	19.31	169.81
CPL	146.34	23.22	339.80
CNTFA1	109.37	17.62	192.78
CNTFA2	114.25	11.76	134.36
Proposed FA	5.00	3.96	1.98

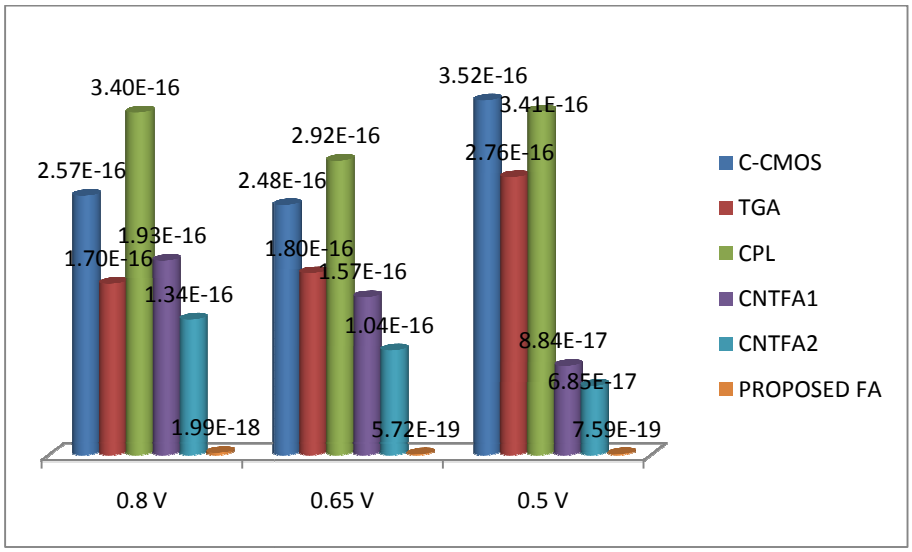

Figure 7 : PDP of Full Adder Cells in different supply voltages

5. CONCLUSIONS

Using emerging technologies such as CNFET technology have lead to design circuits with better performance in comparison with traditional MOSFET based circuits in on hand, and have eased the designing process on the other hand. The proposed designs in this paper are faster, smaller and simpler than the old designs. Hence they have better performance.

REFERENCES

[1] The International Technology Roadmap for Semiconductors (ITRS), 2009.

[2] F. Prégaldiny, C. Lallement, JBKammerer, (2006) "Design-oriented compact models for CNTFETs", International Conference on Design and Test of Integrated Systems in Nanoscale Technology, pp 34-39.

[3] M. Sulieman, V. Beiu, (2003) "Review of recent full adders implemented in single electron technology," IEEE 46th Midwest Symposium on Circuits and Systems, Vol. 2, pp 872-875.

[4] J. Appenzeller, J. Knoch, R. Martel, V. Derycke, S. Wind, and P. Avouris, (2002) "Carbon nanotube electronics," IEEE Transactions on Nanotechnology, Vol. 1, No. 4. pp 184-189.

[5] A. Raychowdhury and K. Roy, (2004) "A novel multiple-valued logic design using ballistic carbon nanotube FETs," in Proceedings of International Symposium on Multiple-Valued Logic, pp 14–19.

[6] A. Raychowdhury, K. Roy, (2005) "Carbon-Nanotube-Based Voltage-Mode Multiple-Valued Logic Design," IEEE Transactions on Nanotechnology, Vol. 4, No. 2, pp 168-179.

[7] A. Raychowdhury K. Roy, (2007) "Carbon Nanotube Electronics: Design of High-performance and low power Digital Circuits," IEEE Transactions on Circuits and Systems-I: Regular papers, Vol. 54, No. 11.

[8] S. Iijima, (1991) "Helical microtubules of graphitic carbon," Nature 354, 56–58.

[9] J. Appenzeller, (2008) "Carbon nanotubes for high performance electronics— Progress and prospect," Proceedings of the IEEE, Vol. 96, No. 2.

[10] P. Avouris, Z. Chen, & V. Perebeinos, (2007) "Carbon-based electronics," Nature Nanotechnology. 2, pp 605–615.

[11] R. Saito, T. Takeya, T. Kimura, G. Dresselhaus, and MS Dresselhaus, (1998) "Raman intensity of single-wall carbon nanotubes," Phys. Rev. B 57, 4145.

[12] R. Martel, T. Schmidt, HR Shea, T. Hertel, and Ph. Avouris, (1998) "Single- and multi-wall carbon nanotube field-effect transistors," Appl. Phys. Lett. 73, 2447.

[13] S.Heinze, J.Tersoff, R.Martel, V.Derycke, J.Appenzeller and P.Avouris, (2002) "Carbon Nanotubes as Schottky Barrier Transistors," Phys. Rev. Lett. 89, 106801.

[14] J. Deng, (2007) "Device modeling and circuit performance evaluation for nanoscale devices: silicon technology beyond 45 nm node and carbon nanotube field effect transistors," Doctoral Dissertation, Stanfor University.

[15] J. Deng and H.-SP Wong, (2007) "A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application—Part I: Model of the intrinsic channel region," IEEE Trans. Electron Devices, Vol. 54, No. 12, pp 3186-3194.

[16] J. Deng and H.-SP Wong, (2007) "A Compact SPICE Model for Carbon- Nanotube Field-Effect Transistors Including Nonidealities and Its Application: Part II: Full Device Model and Circuit Performance Benchmarking." IEEE Trans. Electron Devices. Vol. 54, No. 12, pp 3195- 3205.

[17] R. Zimmermann and W. Fichtner, (1997) "Low-power logic styles: CMOS versus pass-transistor logic," IEEE J. Solid-State Circuits, Vol. 32, pp 1079–1090.

[18] N. Weste and K. Eshraghian, (1993) "Principles of CMOS VLSI Design, A Systems Perspective," 2nd edition, Reading, Mass.: Addison-Wesley, pp 236.

[19] S. Issam, A. Khater, A. Bellaouar, Ml Elmasry, (1996) "Circuit techniques for CMOS lowpower high performance multipliers," IEEE J. Solid-State Circuit 31, pp 1535-1544.

[20] K.Navi, A. Momeni, F. Sharifi, P. Keshavarzian,(2009)"Two novel ultra high speed carbon nanotube Full-Adder cells ", IEICE Electronics Express, Vol. 6, No. 19 , pp 1395-1401.

[21] K. Navi, F. Sharifi, A. Momeni, P. Keshavarzian,(2010) "Ultra High Speed CNFET Full –Adder Cell Based on Majority Gates," IEICE Trans. Electronics, Vol. E93-c, No.6, pp 932-934.