A NOVEL FULL ADDER CELL BASED ON CARBON NANOTUBE FIELD EFFECT TRANSISTORS

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ABSTRACT

Presenting a novel full adder cell will be increases all the arithmetic logic unit performance. In this paper, We present two new full adder cell designs using carbon nanotube field effect transistors (CNTFETs). In the first design we have 42 transistors and 5 pull-up resistance so that we have achieved an improvement in the output parameters. Simulations were carried out using HSPICE based on the CNTFET model with 0.9V V_{DD}. The denouments results in that we have a considerable improvement in power, Delay and power delay product than the previous works.

KEYWORDS

Full Adder, Carbon Nano-tube, Carbon Nano-tube field effect transistor, Low power full adder, CNTFET

1. INTRODUCTION

Many problems have been introduced because of the MOSFET technology limitations. By the miniaturization of silicon based circuits we have achieved its physical limitations, molecular devices are becoming hopeful alternatives to the existing silicon technology. Special characteristics of CNT such as high mobility of electrons, high Ion/Ioff ratio and their unique one dimensional band structure that suppresses back scattering and near ballistic or ballistic operation has made it as a potential successor to silicon MOSFETs [1].

Since the I-V characteristics of CNTFETs are quality similar to silicon MOSFET, most of MOS circuits can be transforming to a CNTFET based design.

Carbon Nano Tubes Field Effect Transistors (CNTFETs) in comparison with MOSFET transistors have less size and more scalability and this feature make them suitable for displacing of this technology. These transistors use carbon nano tubes as their channel.

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Less power and high velocity of this transistor, have Encouraged the digital circuit designers to use of these transistors for their designs [2].

Recently, the designers handle CNTEFTs in their designs such as multiple valued reasonable circuits, accounted circuits, invertors and other logic circuits.

For decades the binary logic is used in computational circuits. In recent decades MVL is considered as an alternative to the common binary logics. With using MVL we can transfer information via multiple career , therefore it will be reduced the complexity of interconnections, circuitry and chip area. The most important obstruction to the reception of MVL technology is encoding more than two levels , so that the available room temperature for voltage swing is decreased [3]. In this paper, we present two new full adder cell designs.

2. CNTFET

As one of the hopeful new devices, CNTFET avoids many of conventional silicon devices limitation [4]. All the carbon atoms in CNT are bonded to each other and there is no hanging bond which enables the combination with high-k dielectric materials. A carbon atom in graphene assembles in a single-sheet hexagonal lattice. In this paper we use single-walled carbon nano-tube (SWCNT) which can Be observed as a graphite sheet is rolled up and attach together along a wrapping vector $C_h = n_1 \cdot \bar{a}1 + n_2 \cdot \bar{a}2$,Where $[\bar{a}_1, \bar{a}_2]$ are lattice unit vectors , and the index (n1, n2) are positive integers that identify the chirality's of the tube[5]. Length of C_h is thus the circumference of the CNT, which is given by equation1.

$$C_{\mathrm{h}} = a\sqrt{n_1^2 + n_1^2 + n_1 n_2} \qquad eq3$$

Single-walled CNTs are classified into one of their groups, depends on the chiral number

(n1, n2): (1) armchair (n1 = n2), (2) zigzag (n1 = 0 or n2 = 0), and (3) Chiral (all other indices) and here we use CNT with the chiral number (19, 0). The electrons in CNT are restricted within the atomic plane of graphene. Due to the quasi-1D structure of CNT, the motion of the electrons in the Nano-tubes is extremely limited.

Single electrons may move freely along the tube axis direction. As a result, all wide angle scatterings are prohibited. Only forward scattering and back scattering due to electron phonon interactions are possible for the carriers in Nano-tubes.

The operation principle of Carbon Nano-tube Field Effect Transistor (CNTFET) is similar to the conventional silicon devices.

This three (or four) terminal device consists of a Semi-conducting Nano-tube, acting as conducting channel, bridging the source and drain contacts.

The device is turned on or off electrostatically through the gate. The quasi-1D device structure provides better control of electrostatic gate above the channel distriction than 3D and 2D device structures. In terms of the device operation mechanism, CNTFET can be grouping as either Schottky Barrier (SB) controlled FET (SB-CNTFET) or MOSFET-like FET [4].

The conductivity of SB-CNTFET is controlled by the majority carriers tunnelling via the SBs at the end contacts. The On-current and consequently device performance of SB-CNTFET is

determined by the contact resistance due to the existence of tunnelling barriers at both or one of the source and drain contacts, instead of the channel conductance.

SB-CNTFET exhibits ambipolar transport behaviour [6]. The work function induced obstacles at the end contacts can be made to increase either electron or hole transport. As a result both polar device (N-type FET or P-type FET) and the device bias point can be adjusted by choosing the appropriate work function of source/drain contacts.

On the other hand, MOSFET like CNTFET exhibits unipolar behaviour by blocking either electron (pFET) or hole (nFET) transport with deeply doped source/drain [6].

The non-tunnelling potential barrier in the channel region, and thus the conductivity, is modulated by the gate-source bias. Although better dc current can be obtained by SB-CNTFET with the self-aligned structure, its efficiency is going to be poor due to the nearness of the gate electrode to the source/drain metal.

The ambipolar behaviour of SBCNTFET also makes it undesirable for complementary logic design. Taking into account both the manufacture achievability and superior performance of MOSFET-like CNTFET as compared to SB-CNTFET, the CNTFET that used in HSPICE model is MOSFET-like CNTFET.

3. Previous works

Many full adder cells have been presented. One of these designs is Hybrid-CMOS full adder cell that implemented by 24 transistors [7]. The outputs of this design are full swing [7]. Another Full adders are based on multiplexers [8,9], Full Adder presented in [9] implements with 10 transistors, but the outputs are not full swing. Some adders are designed with majority function [10–14]. The researchers have presented many full adder cell designs which state of the art design used majority functions. In this paper we will compare the result of our new proposed designs with 3 recent carried out models. One of these designs has 7 capacitors which have been implemented by equation 2.(Fig.1)[11].

This design has implemented in two stages. The first stage implements $\overline{C_{out}}$ by using majority-not function. And the second stage utilities a five input majority-not function to create $\overline{SUM}$.

$$\text{Majority}(A,B,C) = AB + AC + BC = C_{out} \qquad \text{eq4}$$

$$SUM = Maj(A, B, \overline{C_{out}}, \overline{C_{out}})$$

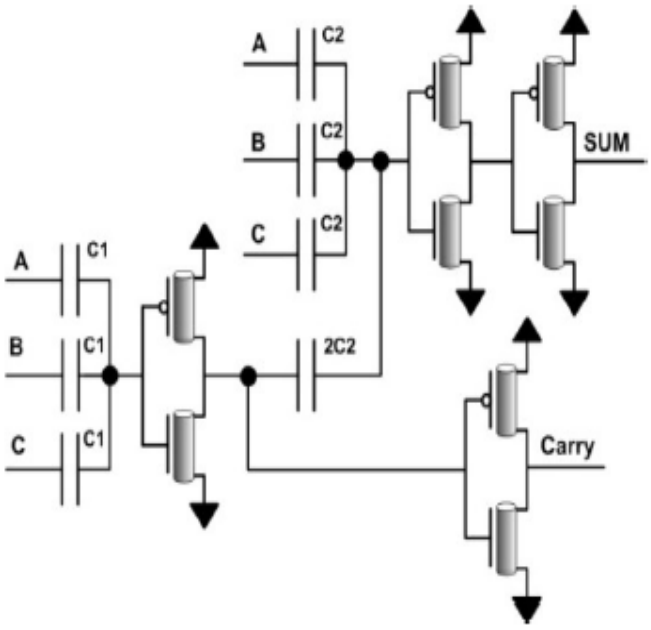


Figure 1. Full adder1 [11]

Next design improved the circuit parameters by reducing the number of the capacitors with 2 stages.(Fig.2)[13]. The state of the art full adder cell presented with using 8 capacitors and 10 transistors (Fig.3)[15]. This design was implemented by minority,NAND and NOR function.

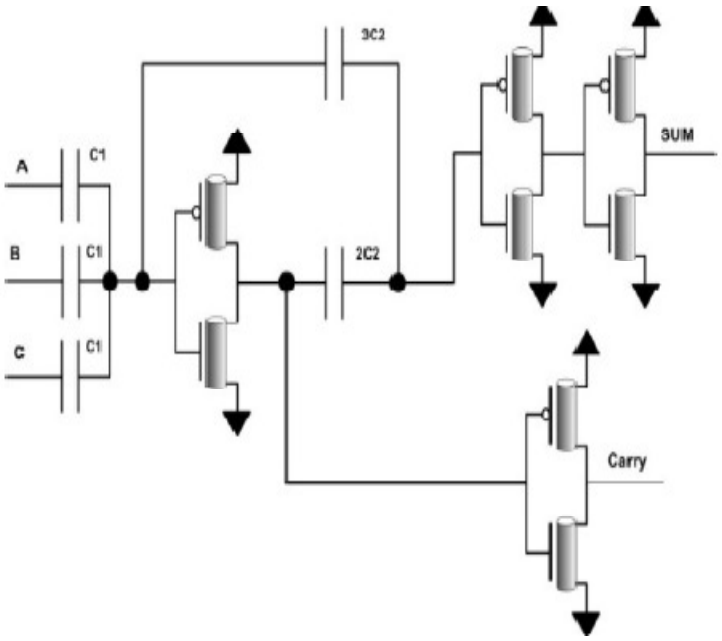


Figure 2. Full Adder 2

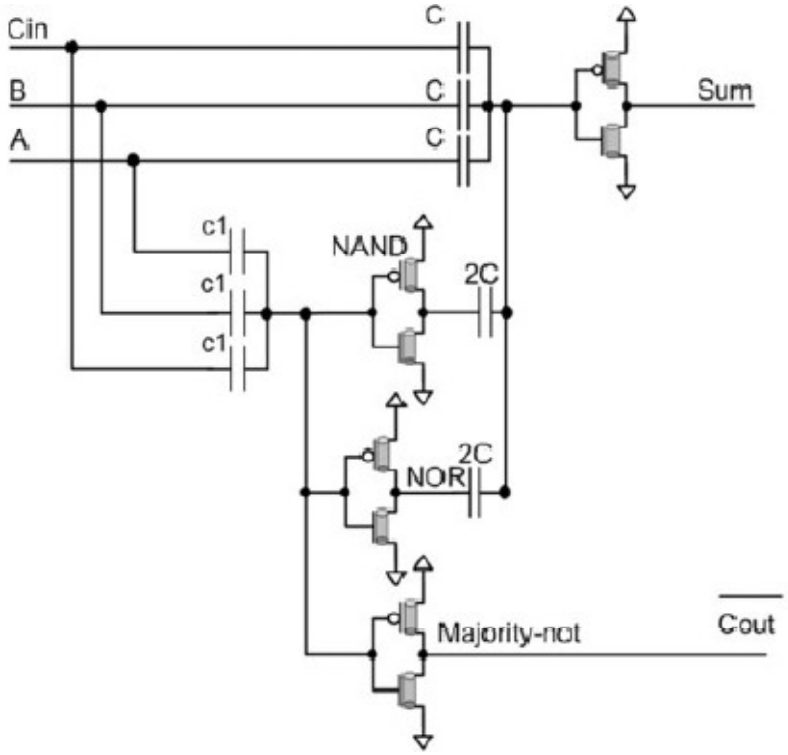
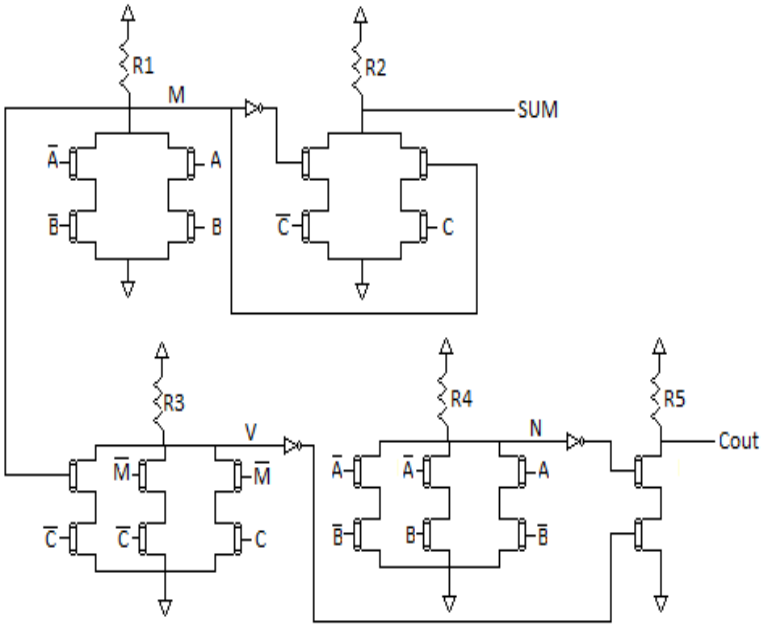


Figure 3. Full Adder3

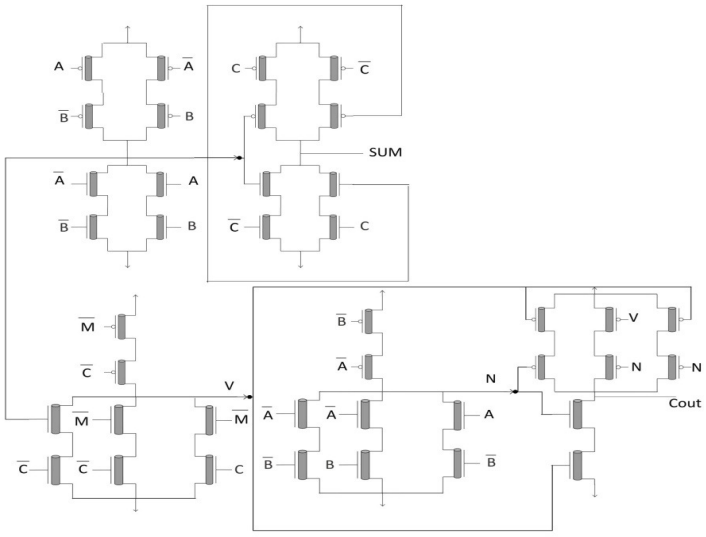
In the last full adder cell designs $\overline{SUM}$ and $\overline{C_{out}}$ was implemented and they should used a NOT function to achieve the full adder outputs, But in our novel circuit design we implement Carry and Sum without using any not function.

4. Proposed Design

In this paper, we presented a new efficient full adder cell. In our first design (figure4-A) we used 42 transistor and 5 pull up resistance And in the second design (figure4-B) by replacing the pull up transistors instead of resistances, we have achieved a significant improvement in our output parameters. Fig 5 show the HSPICE simulation results.



(A)



(B)

Figure 4. proposed design

The outputs of this circuit are completely full swing (As shown in Figure 5).

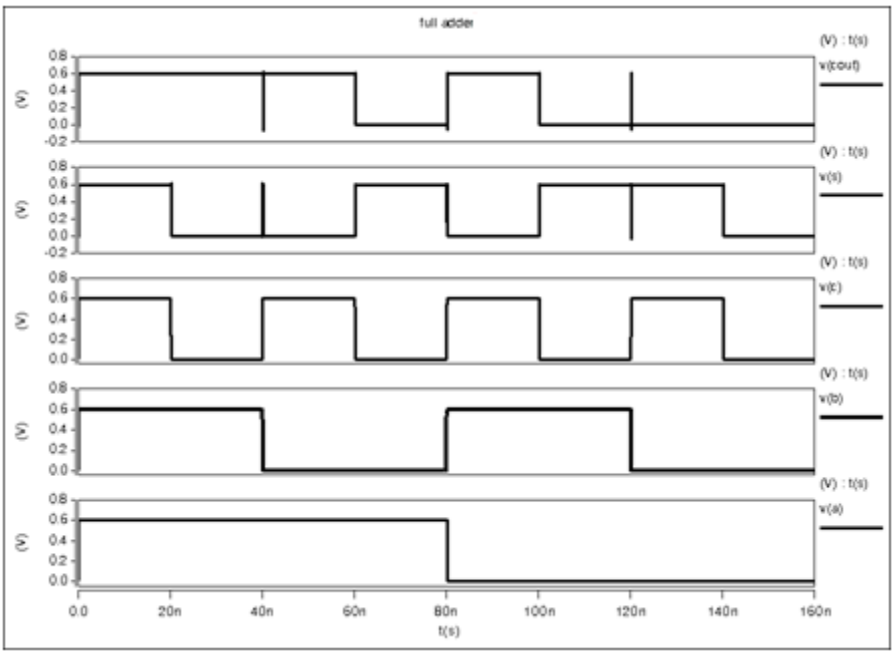


Figure 5. Simulation results (A, B, Cin, Sum, Cout)

Finally, the calculated result of PDP, delay and power parameters is proposed in table 1.

	Power	**Delay**	**PDP**
Full adder-1[7]	5.23E-07	7.97E-11	4.17E-17
Full adder-2[8]	4.71E-07	8.82E-11	4.15E-17
Full adder-3[9]	7.12E-07	7.51E-11	5.35E-17
Design A	2.25E-05	3.00E-08	9.01E-16
Design B	1.35E-08	3.45E-11	4.663E-19

Table 1**.** Simulation results (A, B, Cin, Sum, Cout)
Our proposed circuit power and delay are less than previous circuits

In figures 6 to 8 can be seen that the output parameters are significantly improved compared to the previous design. Cause of this improvement is the use of resistors and capacitors in this design.

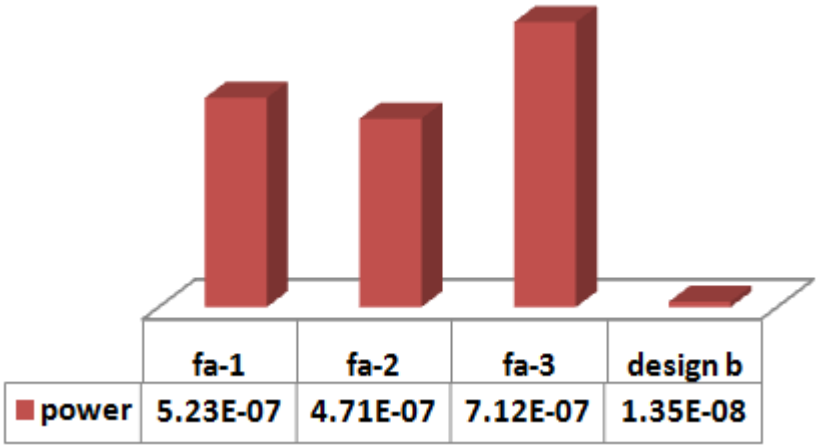


Figure 6. Power results

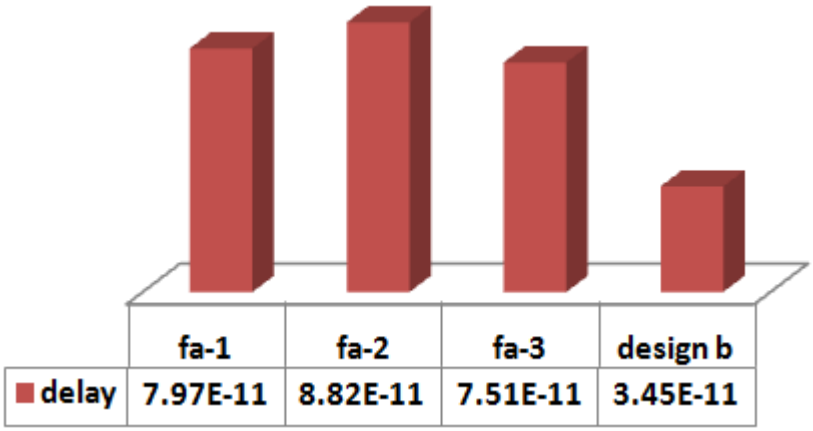


Figure 7. Delay results

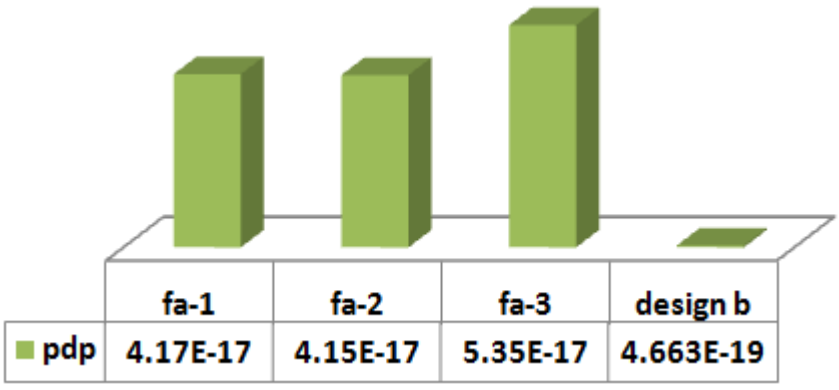


Figure 8. PDP results

5. CONCLUSIONS

In this paper we have presented an improved CNFET Full Adder circuit design using carbon Nano-tube field effect transistors. We have achieved a significant improvement in delay, power and power delay product. This design controls all the three stable output voltage values by controlling the appropriate carbon Nano-tube field effect transistors. To achieve an improved CNFET Full Adder circuit designs, all the CNTFETs have been used to activate the adequate guidance path and to disable all the other paths to the output, The considerable progresses in terms of speed and energy savings achieve in various test conditions using the proposed design and finally we showed that we can improve simulation result by using transistors instead of resistance.

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