A HIGH EFFICIENCY CHARGE PUMP FOR LOW VOLTAGE DEVICES

Aamna Anil[1] and Ravi Kumar Sharma[2]

[1]Department of Electronics and Communication Engineering
Lovely Professional University, Jalandhar, Punjab, India
jaswalaamna@gmail.com
[2]Department of Electronics and Communication Engineering
Lovely Professional University, Jalandhar, Punjab, India
ravi.85jpr@gmail.com

ABSTRACT

A charge pump is a kind of DC to DC converter that uses capacitor as energy storage elements to create a higher or lower voltage power source. Charge pumps make use of switching devices for controlling the connection of voltage to the capacitor. Charge pumps have been used in the nonvolatile memories, such as EEPROM and Flash memories, for the programming of the floating-gate devices. They can also be used in the low-supply-voltage switched-capacitor systems that require high voltage to drive the analog switched. This paper includes voltage analysis of different charge pumps. On the basis of voltage analysis a new charge pump is proposed.

1. INTRODUCTION

A charge pump circuit provides a voltage that is higher than the voltage of the power supply or a voltage of reverse polarity. In many applications such as Power IC, continuous time filters, and EEPROM, voltages higher than the power supplies are frequently required. Increased voltage levels are obtained in a charge pump as a result of transferring charges to a capacitive load and do not involve amplifiers or transformers. For that reason a charge pump is a device of choice in semiconductor technology where normal range of operating voltages is limited. Charge pumps usually operate at high frequency level in order to increase their output power within a reasonable size of total capacitance used for charge transfer. This operating frequency may be adjusted by compensating for changes in the power requirements and saving the energy delivered to the charge pump.

Among many approaches to the charge pump design, the switched-capacitor circuits such as Dickson charge pump are very popular, because they can be implemented on the same chip together with other components of an integrated system. The voltage gain of Dickson charge pump is proportional to the number of stages in the pump. It may cost quite many devices and silicon area, when a charge pump with the voltage gain larger than 10 or 20 is needed. Such high voltage gains are required for low voltage EEPROMs, and typically more than three stages of Dickson charge pump are used. Improved Dickson charge pumps for low voltage EEPROMs and flash memories are developed.

Charge pump operates by switching ON and OFF a large number of MOS switches which charge and discharge a large number of capacitances, transferring energy to the output load. Large

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amount of energy is lost whenever the load current is reduced. Savings of switching energy were primary reason for the design efforts, where a special circuit organization was proposed to regulate switching frequency whenever a requirement for the load current changes. There is a need for better understanding of the design tradeoffs related to charge pump design.

2. LITERATURE REVIEW

The first widely used voltage boosting circuit was the Cockcroft-Walton voltage multiplier [1]. This circuit, shown in Figure 1.1, uses diodes and serially connected capacitors and can boost to several times the supply voltage. The Cockcroft-Walton charge pump provides efficient multiplication only if the coupling capacitors are much larger than the stray capacitance in the circuit, making it undesirable for use in integrated circuits.

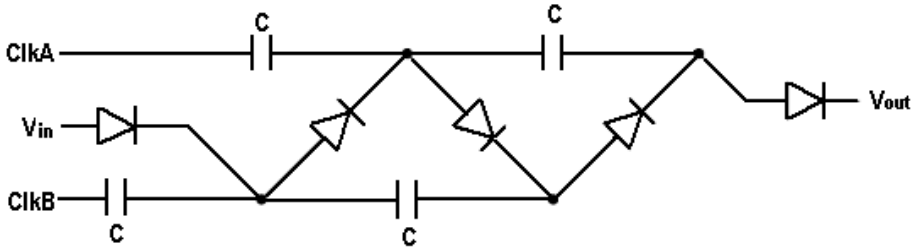

Figure 1: Cockcroft-Walton charge pump

The Dickson charge pump [2] circuit is presented as an improvement of Cockcroft-Walton circuit. In the Cockcroft-Walton charge pump circuit, the coupling capacitors are connected in series. This results in higher output impedance as the number of stages increases.

In[2] the Dickson charge pump circuit, the coupling capacitors are connected in parallel and must be able to withstand the full output voltage. This results in lower output impedance as the number of stages increases. Both circuits require the same number of diodes and capacitors and can be shown to be equivalent. The drawback of the Dickson charge pump circuit is that the boosting ratio is 3 degraded by the threshold drops across the diodes. The body effect makes this problem even worse at higher voltages.

In [3], A novel mixed-structure charge pump based upon the combination of the modified CTS charge pump and cross-coupled output stage to reduce the output threshold-drop by the output MOS-diode transistor in the smart voltage controller based CTS charge pump. An enhanced modified-CTS charge pump structure which combines the modified-CTS charge pump with a simplified cross-coupled output stage.

A feedback charge pump circuit that uses cross-coupled NMOS switches are used to achieve a high boost ratio for a low-voltage DRAM word-line driver. This circit uses two capacitors that are switched in such a way that during every clock cycle, one capacitor is charged to the supply voltage and the other capacitor is boosted to twice the supply voltage by the clock. The two capacitors reverse roles every clock cycle, causing the voltage at the output to be a square wave that switches between V_{DD} and $2V_{DD}$. Two of these cross-coupled NMOS pairs are used along with another type of charge pump and an inverter to make up the complete boosted voltage generator.

An earlier circuit that switches between 4 two networks of capacitors is described in [4] as an “inductance-less dc-dc converter.” A lot of work has been done in recent years involving charge pumps for use in DRAM circuits. In, a high-efficiency word-line driver for a DRAM is presented. In [5], a charge pump circuit that provides a negative substrate bias for a DRAM is presented.

In, the cross-coupled NMOS charge pump introduced in [6] is used to improve the speed of a pipeline A/D converter by boosting the clock drive in order to reduce the on-resistance of transmission gates in the pipeline. This work also utilizes a bias voltage generator to bias the n-well to twice the supply voltage, preventing latch up from occurring during the initial startup transient.

Charge pumps are also widely used in the program circuits and word line drivers in an EEPROM. A charge pump for use in low-voltage EEPROM's is presented. This circuit is similar to the Dickson charge pump, but it uses a bootstrapped clock generator to eliminate the threshold drops across the pass transistors. A different method for eliminating the threshold drops in the Dickson charge pump is presented in .

3. DICKSON CHARGE PUMP

John F Dickson proposed a voltage multiplier circuit. The MOST's in Dickson charge pump function as diodes, so that the charges can be pushed only in one direction. However the nodes of the diode chain are coupled to the inputs via capacitors in parallel, instead of series so that the capacitors have to withstand the full voltage developed along the chain. Two pumping clocks are used. The two pumping clocks Clk1 and Clk2 are out of phase and have a voltage amplitude V. The value of V_0 is equal to V_{DD}. Through the coupling capacitors C1-C4, two clocks push the charge voltage upward through the transistors. Cs is the parasitic capacitance assosiated with each pumping node, f is the frequency of the pumping clocks and I_0 is the output current loading.

The Dickson charge pump circuit shown in Figure 2 has been widely deployed for generating higher voltages. This circuit consists of capacitor stages connected by diodes and coupled in parallel by two non-overlapping clocks. The diode-connected NMOS transistors are used instead of p-n junction diodes for implementing the circuit in standard CMOS process. The diode-connected NMOS allow the charge flow only in the direction of the output stage in ideal conditions. The charges are pushed from one stage to the next, resulting in higher DC voltage at the output.

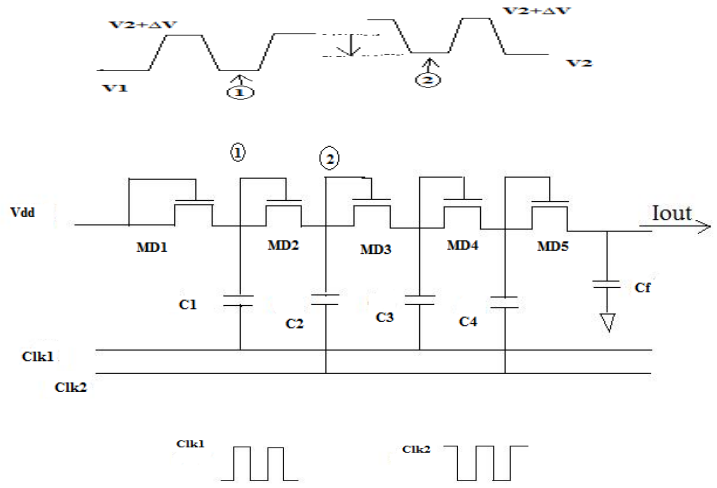

Figure 2: A Four Stage Dickson Charge Pump

When Clk1 goes from low to high and Clk2 goes from high to low, the voltage at node 1 is settled to $V_1 + \Delta V$ and the voltage at node 2 is settled to V_2, where V_1 and V_2 are defined as steady-state lower volatge at node 1 and node 2. Both MD1 and MD2 are reverse biased and the

charges are being pushed from node 1 to node 2 through MD2. The final voltage difference between node 1 and node 2 is the threshold voltage MD2. The necessary condition for the charge pump to function is that ΔV must be larger than the MOST's threshold voltage V_{tn}, i.e $\Delta V > V_{tn}$. The voltage pumping gain for the second pumping stage $G_{V2}$is defined as the voltage difference between V_2 and V_1.

The drawback of Dickson charge pump is that the boosting ratio is 3 degraded by the threshold drop across the diodes. The body effect makes this problem even worst at high voltages.

4. CHARGE PUMP USING STATIC CTS'S

Static CTS charge pumps are new charge pumps employing dynamic switches to increase the voltage pumping gain The basic idea behind these multipliers is to use MOS switches with precise on/off characteristics to direct charge flow during pumping rather than using diodes, or diode connected transistors which inevitably introduce a forward voltage drop at each node. One of the first low voltage CTS based charge pumps with static backward control was presented by Wu.

MOST switches with proper on/off cycles are reffered to as CTS's. They have been used in place of diodes and show better voltage pumping gain than the diodes. MD1-MD4 are diodes for setting up the initial voltage at each pumping node. They are not involved in the pumping operation. MS1=MS4 are the CTS's. If the switches can be on/off at the designated clock pulses, they can allow the charge to be pushed only in one direction. Then for each pumping stage upper voltage of each input is equal to the lower voltage of the output. In Figure 2 when Clk1 is high and Clk2 is low , the voltage at node1 is pushed to V_2 from V_1 and voltage at node 3 is pushed to $V_3 + \Delta V$. MS2 switch must be turned on by the voltage at node 3. Therefore voltage at node 3 must be higher than the threshold voltage of MS2. The gate to source volatge of MS2 is $2\Delta V$, i.e. $2\Delta V > V_{tn}(V_2)$.

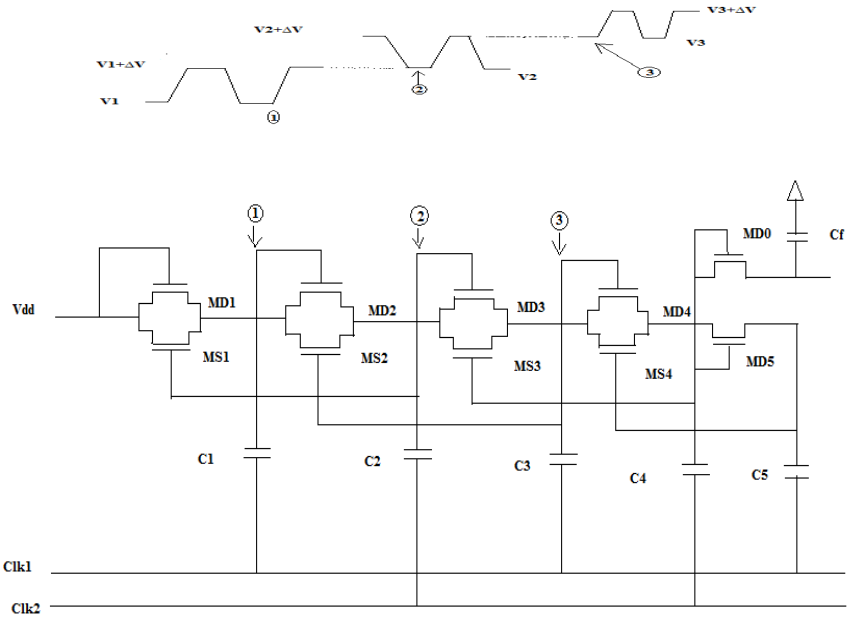

Figure 3: A Four Stage Charge Pump Using Static CTS's

On the other hand when the opposite condition arises the voltage at node 1 is V_1 and voltage at node 3 is V_3. For ideal operation MS2 has to be turned off. Therefore gate to source voltage of

MS2 must be smaller than the threshold voltage i.e. $2\Delta V < V_{tn}, V_1$ These two conditons have to be satisfied. Therefore MS2 can never be turned off completely and reverse charge sharing between node 1 and node 2 occurs. Thereby reducing the output of the charge pump.

The drawback of this circuit is that charge transfer switches can not be completely turned off, leading to reverse charge sharing which leads to reducing in voltage gain.

5. CHARGE PUMP USING DYNAMIC CTS'S

To overcome the drawback of static charge pump dynamic charge pump is designed. In dynamic charge pump each CTS's is accompanied with p-mos and n-mos pair, so that CTS's can be turned on and off completely.

When Clk1 is high node 1 and node 2 have volatge V_2 and voltage at node 3 is $V_3+\Delta V$. If the voltage is $2\Delta V$ above V_{tn} , then MP2 is turned on, causing MN2 being turned on by the voltage at node 3.

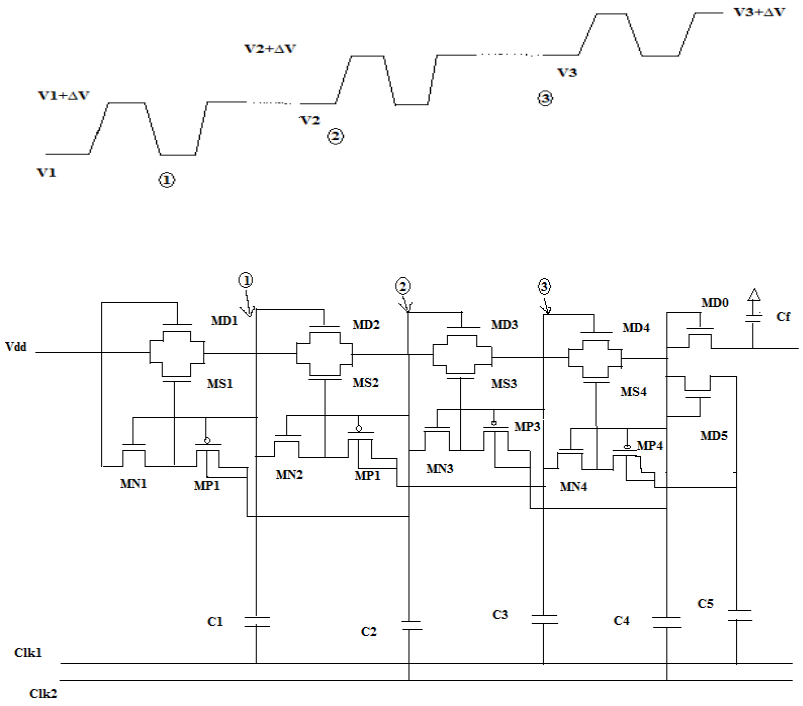

Figure 4: A Four Stage Charge Pump Using Dynamic CTS's

On the other hand , when Clk1 is low and Clk2 is high, the voltage at node 1 is V_1 and both the voltages at node 2 and node 3 is $2\Delta V$. If $2\Delta V > V_{tp}$ and $2\Delta V > V_{tn}(V_2)$, where $V_{tn}$is the threshold voltage of PMOST's, then MP2 is turned on , causing MS2 being turned OFF.

To overcome these problems associated with the Dickson charge pump, Wu and Chang [2] proposed the Dynamic charge pump. Figure 3 shows a 4-stage Dynamic charge pump. This circuit employs dynamic charge transfer switches (CTS). Each of the CTS (MS's transistors) is controlled by the pass transistors MN's and MP's. The dynamic CTS are used to transfer charges from one stage to the next without suffering the problem of voltage drop. The CTS's can be turned off completely when required and can also be turned on effectively by the higher voltage generated in the next stage. Thus, reverse charge flow is avoided, leading to increased efficiency.

During time interval T1, clock signal Clk1 is low and Clk2 is high. The voltage at node 1 is V_{DD} and the voltage at node 2 is 3 x V_{DD}. The pass transistor MN1 is turned off as V_{GS} =0, while MP1 is turned on. As a result, charge transfer switch MS1 is turned on.

This leads to charge transfer from power supply V_{DD} to node 1. During time interval T2, Clk1 is low and Clk2 is high. The MP1 is turned off and MN1 is turned on due to voltage 2 V_{DD} at node 2. Hence, CTS MS1 is turned off completely. The working of the rest of the stages is based on similar concept. The output stage of the Dynamic charge pump is a diode connected NMOS transistor and this leads to reduction of output voltage due to body effect.

6. MIXED-STRUCTURE CHARGE PUMP

An enhanced modified-CTS charge pump structure which combines the modified-CTS charge pump with a simplified cross-coupled output stage.

At the time, when Clk1 is low (0V) and Clk2 is high. The node voltage V_4 will be pumped up to $5\times V_{DD}$ which is high enough to turn off MO2. The node V_5 will back down to $4\times V_{DD}$ which is low enough to turn on PMOS MO1 completely without any threshold-drop effect. These results in the optimum high voltage transferring, V_{out} shall be charged up to 5×VDD as V4.

In another time, when Clk1 is high and Clk2 is low (0V), V_3 and V_5 are pumped up to $4V_{DD}$ and $5V_{DD}$, respectively. The voltage level of V_5 is high enough to turn off MO1. On the other hands, V_4 goes back to $4\times V_{DD}$ which is low enough to turn on PMOS MO2, and then V_{out} shall be charged up to $5\times V_{DD}$ as V5.

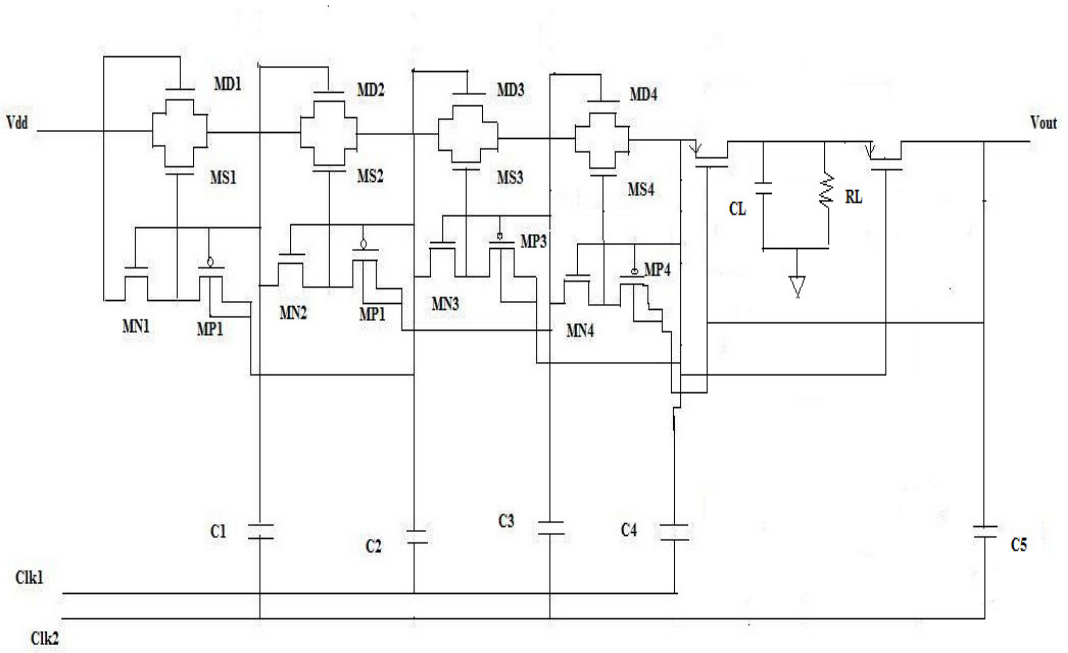

Figure 5:Mixed structure charge pump

7. RESULTS

In this paper volatge analysis for different charge pumps has been performed. Results have been simulated in Cadence Virtuoso and the results are shown in the form of input vs output voltage plot. On the basis of voltage analysis a new charge pump is proposed for improving the output voltage obtained.

7.1 DICKSON CHARGE PUMP

Voltage analysis of the Dickson charge pump. On varying the input voltage change is observed in output voltage. Output voltage increases with increase in input voltage.Input voltage is varied from 1V to 5V. Period of the input pulse is kept constant at 10n.

Input voltage	Frequency	Stop time	Dickson charge pump
1V	100MHz	3000ns	15.97V
2V	100MHz	3000ns	16.77V
3V	100MHz	3000ns	17.63V
4V	100MHz	3000ns	18.52V
5V	100MHz	3000ns	19.46V

Table 1: Voltage analysis on Dickson Charge pump

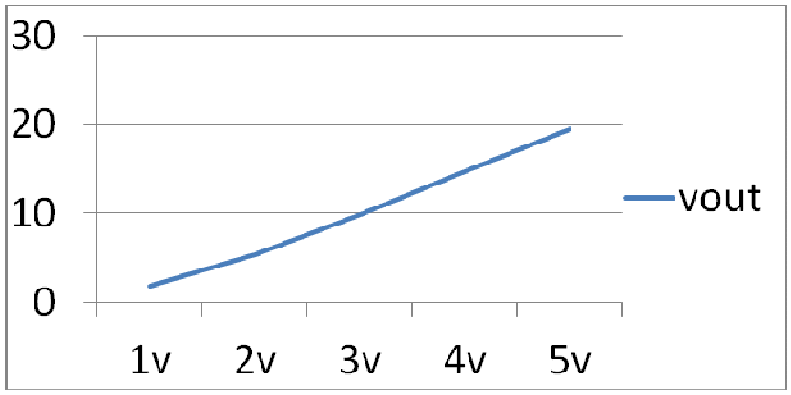

Figure 6: Output of Dickson charge pump for variable V input

7.2 CHARGE PUMP USING STATIC CTS'S

Voltage analysis of the Static charge pump. On varying the input voltage change is observed in output voltage. Output voltage increases with increase in input voltage. But the increase in output voltage is less in comparison to Dickson charge pump. The output voltage is less because of reverse charge sharing effect. To overcome this problem Dynamic charge pump was designed. Input voltage is varied from 1V to 5V. Period of the input pulse is kept constant at 10ns. Voltage of input pulse is also varied fromm 1V to 5V.

Input voltage	Frequency	Stop time	Static charge pump
1V	100MHz	3000ns	8.716V
2V	100MHz	3000ns	9.53V
3V	100MHz	3000ns	10.57V
4V	100MHz	3000ns	11.58V
5V	100MHz	3000ns	12.56V

Table 2: Voltage analysis of Static charge pump

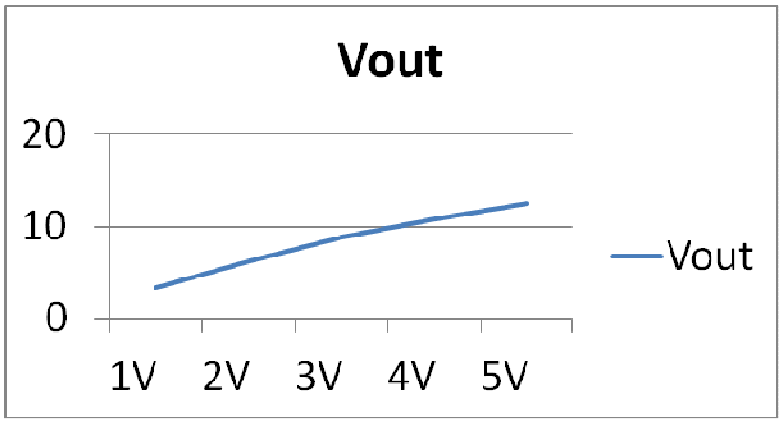

Figure 7: Output variation with respect to change in the input voltage

7.3 CHARGE PUMP USING DYNAMIC CTS'S

To overcome these problems associated with the Dickson charge pump, Wu and Chang [2] proposed the Dynamic charge pump[2]. This circuit employs dynamic charge transfer switches (CTS). Each of the CTS (MS's transistors) is controlled by the pass transistors MN's and MP's. The dynamic CTS are used to transfer charges from one stage to the next without suffering the problem of Vth voltage drop. The CTS's can be turned off completely when required and can also be turned on effectively by the higher voltage generated in the next stage. Thus, reverse charge flow is avoided, leading to increased efficiency.

Input voltage	Frequency	Stop time	Dynamic charge pump
1V	100MHz	100MHz	18.39V
2V	100MHz	100MHz	19.39V
3V	100MHz	100MHz	20.39V
4V	100MHz	100MHz	21.39V
5V	100MHz	100MHz	22.39V

TABLE 3:Voltage analysis of dynamic charge pump

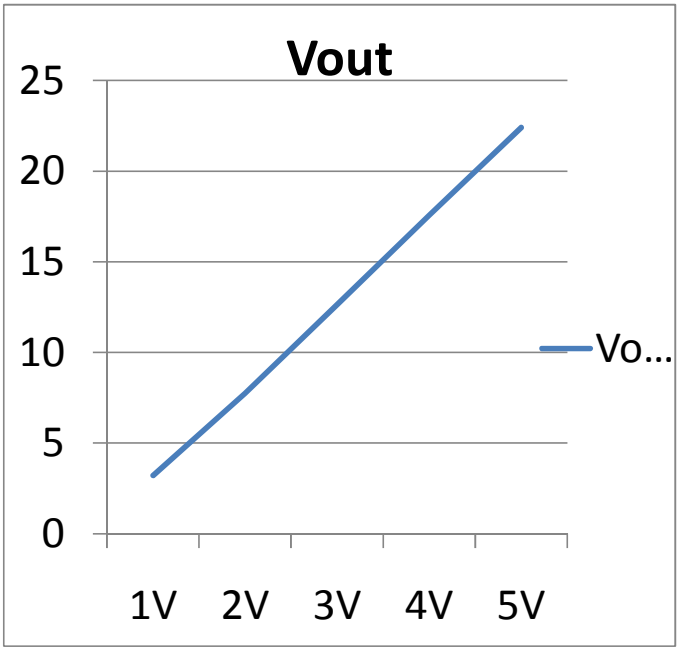

Figure 7:Output for variable V input

7.4 MIXED STRUCTURE CHARGE PUMP

A novel mixed-structure charge pump based upon the combination of the modified CTS charge pump and cross-coupled output stage is implemented in this section to reduce the output threshold-drop by the output MOS-diode transistor in the smart voltage controller based CTS charge pump [3]. The mixed structure charge pump showed leakage in the output voltage obtained. To overcome this drawback a new charge pump is proposed which reduces leakage and amplifies the output.

Implementation of mixed structure charge pump in Cadence Virtuoso is shown below. Output voltage obtained is around 22V with leakage present in it.

8. PROPOSED CHARGE PUMP

A MOS switch when is completely on can pass charge from its drain to its source similar to a forward biased diode. It has the advantage that almost no voltage drop occurs between its drain and source terminal. Replace the diode connected NMOS transistors of a classical Dickson charge pump with PMOS switches. If these switches are turned ON and OFF at proper clock phases, they can allow the charge to be pushed in only one direction. In order to control the ON/OFF operation of each switch, a dynamic inverter is inserted in each stage.

The inverter works dynamically because its low and high voltages change during different clock phases and are different from the low and high voltages of the inverters of the other stages. The control voltage of each inverter is derived from the pumping node of the preceding stage; i.e. a forward control scheme is used where the voltage at each pumping node controls the ON/OFF operation of the next stage.

The basic operation of the charge pump, in steady-state mode with no load and ideal conditions (no parasitic). Where we show the voltage waveform of each pumping node and non overlapping clocks, Clk1 and Clk2.

At first, Clk1 is low and Clk2 is high, M0 and M2 are turned on and able to pass charge to their following stages and M1 and M3 should be turned off to impede reverse current. Therefore, during this phase $V_1=V_{DD}$, $V_2=V_3=3V_{DD}$ and $V_{out}=4V_{DD}$. As a result, the V_{GS} of transistor MP2 is equal to zero and the output of the inverter MN2- MP2 is low; i.e., V_{DD}.

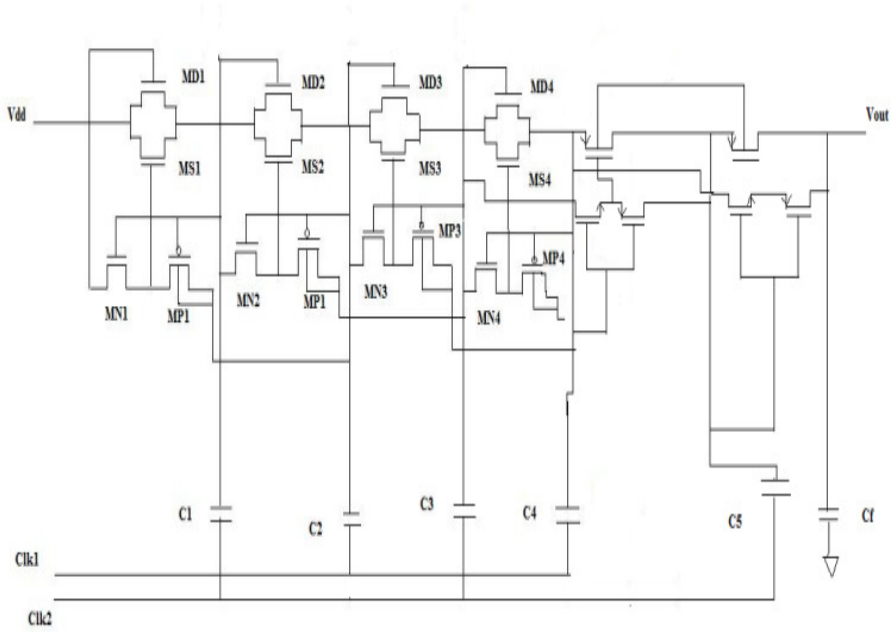

Figure 8: Proposed Charge Pump

Hence, the V_{GS} of PMOS transistor M2 is equal to $2V_{DD}$, which confirms the supposition that M2 is on. When Clk1 is high and Clk2 is low, M1 and M3 should be turned on to be able to pass the charge to their following stages and M0 and M2should be off to impede the reverse current. Hence during this phase $V_1=V_2=2V_{DD}$, $V_3=V_{out}=4V_{DD}$.

As a result, the V_{GS} of transistor MN2 is equal to zero and the output of the inverter MN2-MP2 is high; i.e., $4V_{DD}$, which means the V_{GS} of PMOS transistor M2 is equal to zero, verifying that transistor M2 is OFF

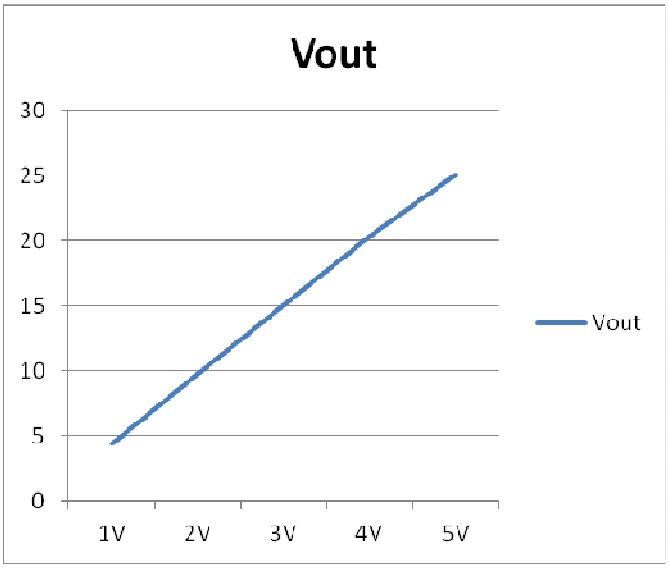

Figure 9: Output for variable voltage input

Input voltage	Frequency	Stop time	Proposed charge pump
1V	100MHz	3000ns	4.452V
2V	100MHz	3000ns	9.78V
3V	100MHz	3000ns	15.06V
4V	100MHz	3000ns	20.32V
5V	100MHz	3000ns	25.07V

Table 4: Voltage analysis of proposed charge pump

9. COMPARATIVE ANALYSIS

Input voltage	Frequency	Stop time	Dickson charge pump	Static charge pump	Dynamic charge pump	Mixed structure charge pump	Proposed charge pump
1V	100MHz	3000ns	15.97V	8.716V	18.39V		4.452V
2V	100MHz	3000ns	16.77V	9.53V	19.39V		9.78V
3V	100MHz	3000ns	17.63V	10.57V	20.39V		15.06V
4V	100MHz	3000ns	18.52V	11.58V	21.39V		20.32V
5V	100MHz	3000ns	19.46V	12.56V	22.39V	22V (with leakage)	25.07V

Table 5: Comparative analysis on the basis of variation in input voltage

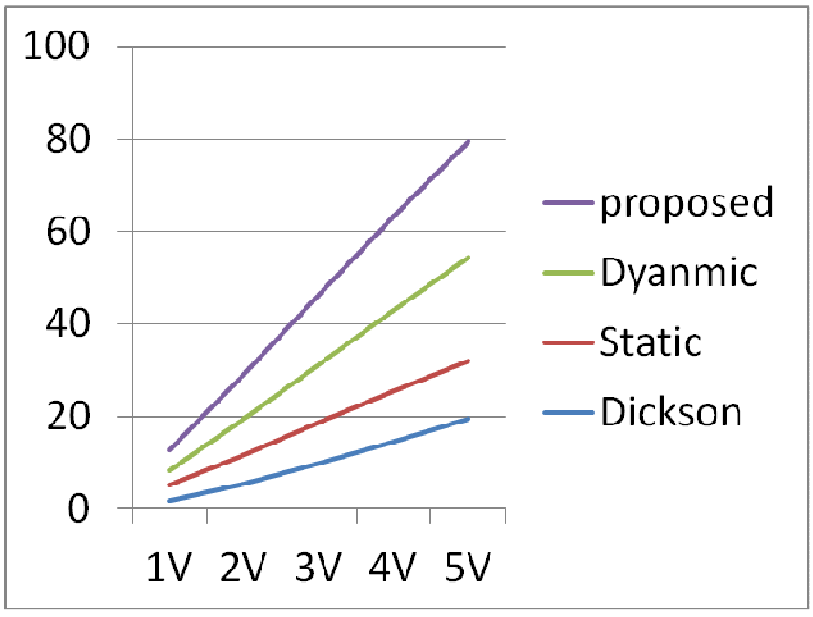

Figure 10: Comparison on the basis of voltage variation

10. CONCLUSION

A Proposed CMOS charge pump circuit, which uses both the NMOS switches and the PMOS switches to eliminate the body effect, has been designed. A novel CTS control scheme which combines the backward control scheme and the forward control scheme is proposed to obtain high voltage gain. In 180nm CMOS process, the simulation results have shown that much higher pumping efficiency can be achieved by the proposed charge pump compared with other.

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AUTHORS

Aamna Anil[1] was born in Shimla(Himachal Pradesh). She has done her B.tech degree in Electronics and Communication Engineering from Lovely Professional University, Jalandhar. She is currently pursuing her M.tech degree from Lovely Professional University, Jalandhar. Her research interest includes Low power VLSI design.

Ravi kumar sharma[2] was born in Jaipur(Rajasthan). he has done his B.Tech degree in Electronics and Communication Engineering from University of Rajasthan,Jaipur and M.Tech degree from Guru Gobind Singh Indraprastha University, Delhi. He is currently working as Asst. Professor in Lovely Professional University, Jalandhar. His research interest includes Low power VLSI design.