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NOVEL SLEEP TRANSISTOR TECHNIQUES FOR LOW LEAKAGE POWER PERIPHERAL CIRCUITS

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ABSTRACT

Static power consumption is a major concern in nanometre technologies. Along with technology scaling down and higher operating speeds of CMOS VLSI circuits, the leakage power is getting enhanced. As process geometries are becoming smaller, device density increases and threshold voltage as well as oxide thickness decrease to keep pace with performance. Two novel circuit techniques for leakage current reduction in inverters with and without state retention property are presented in this work. The power dissipation during inactive (standby) mode of operation can be significantly reduced compared to traditional power gating methods by these circuit techniques. The proposed circuit techniques are applied to inverters and the results are compared with earlier inverter leakage minimization techniques. Inverter buffer chains are designed using new state retention low leakage technique and found to be dissipating lower power with state retention. All low leakage inverters are designed and simulated in cadence design environment using 90 nm technology files. The leakage power during sleep mode is found to be better by X 63 times for novel method. The total power dissipation has also reduced by a factor of X 3.5, compared to earlier sleepy keeper technique. The state retention feature is also good compared to earlier leakage power reduction methodologies.

KEYWORDS

Leakage power, sleep transistor, power gating, average power, state retention

1. INTRODUCTION

With reducing channel length for successive technology generations, threshold voltage and gate oxide thickness are also being scaled down. Leakage current consequently increases exponentially with reduction in threshold voltage. As per the ITRS [1], leakage current is going to be a limiting factor for successive scaling down of transistors. Due to the smaller feature sizes in nanometre technologies, shorter channel lengths cause subthreshold current to increase when the transistor is in the off state. The lower subthreshold voltage gives rise to increased subthreshold current as well, because transistors cannot be switched off completely. Since with every successive technology the number of transistors per given area is on a rise, the leakage power in an integrated circuit for successive generations is increasing , because transistors leak even when they are not activated and significant power dissipation takes place even during inactive state of circuits.

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Thus it is essential to reduce static power during the idle or standby mode of operation of the circuits. SRAMS are integral and vital components of almost all processors, SOCs and Embedded Systems and are occupying a larger area on chips. Various leakage power reduction methods are invariably applied to SRAMs to save valuable battery resources in hand held mobile applications. Since SRAM peripheral circuits such as input drivers, word line drivers, and output drivers occupy major portion of on chip caches in processors, savings in leakage power of peripheral circuits is also advantageous for better performance. Since the on chip memory utilisation might involve long inactivity states during cache misses or might be spending larger time in idle or sleep modes in some applications, static power reduction is going to be a greater concern for such cases.

For a CMOS circuit, the total power dissipation includes dynamic and static components during the active mode of operation. In the standby mode, the power dissipation is due to the standby leakage current [2] [3].

The dynamic (switching) power (P_D) and leakage power (P_{LEAK}) are expressed as

$$P_D = \alpha f C V^2_{DD} \quad \text{................} \quad (1)$$

$$P_{LEAK} = I_{LEAK} V_{DD} \quad \text{...........} \quad (2)$$

where α is the switching activity; f is the operation frequency, C is the load capacitance, VDD is the supply voltage and I_{LEAK} is the cumulative leakage current due to all the components of the leakage current.

In a CMOS Inverter ideally current flows from Source to Drain when $V_{GS} > V_T$. In real transistors current does not abruptly cut-off below threshold, but drops off exponentially as given by equation (3).This conduction is known as leakage conduction and results in undesired conduction when transistor is nominally off. The leakage current is the subthreshold or weak inversion current that flows from drain of a transistor to its source when the transistor is off (gate voltage is below the threshold voltage).

The leakage current in MOSFETs depends on various process parameters, the transistor size and the quiescent state of the circuit [3]. This sub-threshold leakage current for $V_{GS} < V_T$ is given by

$$I_{DS} = I_{DSO}\, e^{(V_{GS}-V_T)/(nv_T)} [1-e^{(-V_{DS}/v_T)}] \quad \text{......} \quad (3)$$

Where

$$V_T = V_{TO} - \eta V_{DS} + \gamma [(\phi_s + V_{SB})^{0.5} - (\phi_s)^{0.5}] \quad \text{......} \quad (4)$$

In these equations I_{DSO} is current at threshold (dependent on process and device geometry), V_{TO} is the zero bias threshold voltage, γ - is the linearised body effect coefficient, η represents the effect of V_{DS} on threshold voltage, n is the sub-threshold swing coefficient, V_T is thermal voltage respectively. η term describes Drain Induced Barrier Lowering effect. Subthreshold conduction is enhanced by Drain Induced Barrier Lowering (DIBL) in which positive V_{DS} effectively reduces V_T . Leakage current doubles for every 8^0 to 10^0K rise in temperature.

The subthreshold leakage current can be reduced by increasing threshold voltage V_{TO}, increasing V_{SB} and reduction of V_{GS}, V_{DS} and lowering the temperature. In deep submicron CMOS circuits, the reduction in leakage current has to be achieved using both process- and circuit-level techniques. At the process level, leakage reduction can be achieved by controlling the dimensions (length, oxide thickness, junction depth, etc.) and doping profile in transistors. At the circuit level, threshold voltage and leakage current of transistors can be effectively controlled by controlling the voltages of different device terminals [drain, source, gate, and body (substrate)].

This work addresses novel static power reduction techniques in inverters and SRAM memory peripheral circuits such as word line drivers. This idea can be extended to other peripherals like write data drivers, decoders etc. A novel low leak inverter is proposed in this work. This novel low leak inverter uses new power gating technique in which PMOS transistor is used in the pull down path and NMOS transistor in the pull up path as sleep transistors. During the active mode of operation both the sleep transistors are on. The PMOS pull down transistor holds the virtual ground (VG) node at a higher potential than ground and the NMOS pull-up transistor maintains the virtual power (VP) node at a lower potential. This causes the current flowing through the circuit to reduce and hence lower power dissipation during active mode. During the idle mode the sleep transistors are off. This causes a large impedance path to be established across the nodes VP and VG than the traditional power gating method. This method provides maximum reduction in static power during periods of inactivity or sleep state. However the output states during active mode of operation will not be at good logic1 and logic 0 values. To obtain good logic output levels during active mode of operation and to achieve the retention of previous output state, state retention transistors are introduced across the sleep control transistors. This state retention technique has resulted in state retention at lower total power dissipation as compared to previous best known techniques. This work also addresses leakage power reduction in buffer chains. Word line drivers have been designed with novel low leak inverters.

Earlier power gating techniques for inverters are compared in terms of static power dissipation and total average power consumption with respect to the novel techniques proposed in this work. Section 2 deals with related work. Earlier power reduction techniques and new proposed techniques for inverters are discussed in section 3. These power minimisation techniques are applied to inverter buffer chains and the relative performance is discussed in section 4. The simulation procedure and results are provided in section 5. The concluding remarks are provided in section 6.

2. RELATED WORK

There are several VLSI techniques to reduce leakage power. Each technique provides an efficient way to reduce leakage power; but disadvantages of each technique limit the application of each technique. Two new approaches are proposed in this work which also reduce total power consumption, thus providing a new choice to low-leakage power VLSI designers. Previous techniques are also studied and compared with the new methods presented in this report.

The well known method to achieve reduced leakage power in inverters makes use of transistor stacking [4].

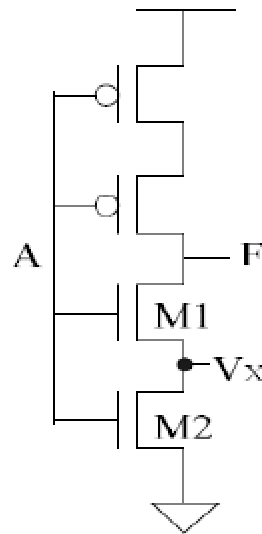


Figure 1. Forced stack Inverter

Subthreshold leakage current flowing through a stack of series connected transistors reduces when more than one transistor in the stack is turned off. This effect is known as stacking effect. Unlike the traditional CMOS inverter this forced stack inverter consists of two pull-up transistors and two pull-down transistors. All inputs share the same input 'A.' If A = 0, then both transistors M1 and M2 are turned off. Due to the internal resistance of M2, the intermediate node voltage Vx is at higher potential than Ground due to the small drain current. The positive potential at the intermediate node, Vx has following effects.

1. The positive source potential Vx causes the gate to source voltage of transistor M1 (VGS1) to be negative and hence the subthreshold current reduces.

2. Since Vx >0, the body to source potential (VSB1) of the transistor M1 becomes positive and results in an increase in threshold voltage of M1 due to larger body effect and hence lower subthreshold leakage.

3. The drain to source potential (VDS1) of transistor M1 decreases due to positive Vx which results in higher threshold voltage because of the Drain Induced Barrier Lowering (DIBL) effect and the subthreshold leakage current gets reduced. All these effects together reduce the leakage current.

[5] proposes the use of sleep transistors for leakage reduction, which are also called gated-V_{DD} and gated-GND techniques. This technique is used to cut off pull-up or pull-down or both networks from supply voltage or ground using sleep transistors. In this technique either i) an additional NMOS sleep transistor is used between pull-down network and ground or/and an additional PMOS sleep transistor is used between pull-up network and VDD. The sleep transistor is turned on during active mode of operation and turned off during idle or standby mode of operation. When the sleep transistor is off the virtual ground terminal VG will be at a nonzero potential. The gate to source voltage of off transistor M2 becomes negative and its threshold voltage increases. This has an effect of reducing subthreshold current flowing between drain and

source of the transistor. The substrate to source voltage and drain to source voltage also reduce and give rise to higher threshold voltage. All these effects cumulatively add up to lowered subthreshold current that flows in the off transistors. [6], implements sleepy stack structure, a combination of forced stack technique and the sleep transistor technique. By combining two prior techniques, the sleepy stack technique can achieve ultra-low leakage power consumption by the use of high-V_{TH} transistors in key places while saving state. Sleepy keeper technique for inverters is discussed in [7].

Using multiple-threshold CMOS technologies, the high-threshold transistors can suppress the subthreshold leakage current, while the low-VTH transistors are used to achieve high performance. Different multi VTH techniques discussed in literature are Multi-threshold voltage CMOS [8], Dual threshold CMOS,Variable threshold CMOS (VTMOS) and Dynamic threshold CMOS. Transistor stacking and self adjustable voltage level circuit for reducing leakage power in sequential circuits is proposed in [9].

The techniques discussed above result in either destruction of state or floating output voltage, large number of extra transistors etc. The new leakage reduction techniques proposed in this work achieve higher leakage power reduction as well as lower average power dissipation.

3. LOWLEAKAGE CIRCIT TECHNIQUES FOR INVERTERS

Section 3.1 discusses the earlier leakage reduction techniques in inverters and the relative merits and demerits of them. Section 3.2 deals with novel leakage minimisation techniques and their applications.

3.1 Sleepy Inverters

Traditionally subthreshold leakage current is reduced by introducing NMOS sleep transistor in the pull down path and PMOS sleep transistor in the pull up path of a CMOS circuit. The CMOS inverter is shown in figure 2. In sleep transistor technique, an NMOS sleep transistor is connected in the pull down path and PMOS transistor is connected in the pull-up path. This sleepy inverter is shown in figure 3. Sleep technique applied to only pull down NMOS transistor is shown in figure 4. Consider sleepy inverter operation. During normal operation the sleep signal slp is held at logic 1 voltage level and complementary sleep signal slpb is held at logic 0 voltage level. The circuit comprising of transistors M1 and M2 functions as a traditional inverter. During normal operation the transistors M3 and M4 are also on and hence the node VG is at ground potential and node VP is at VDD. Thus the inverter produces inverted output. When inverter has to function in stand-by or sleep mode the signal slp is held at logic 0 and signal slpb is held at logic 1. This makes the two transistors M3 and M4 to enter into cut-off state. Thus the node VG is at a virtual ground potential and node VP is at a virtual power potential. Thus the inverter enters in to sleep mode. Due to the cut off transistors M3 and M4 the potential VG increases; the potential VP drops. The source to body potential of transistor M1 increases and causes threshold voltage of transistor M1 to rise. Thus sub threshold current of transistor M1 reduces. The size (W/L) of the stacked sleep transistors determines the value of potential levels at VG and VP.

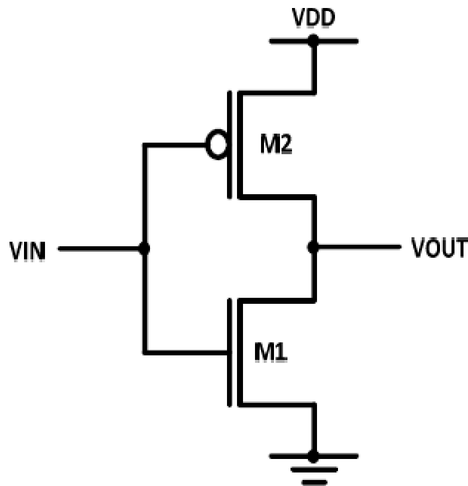


Figure 2. Inverter

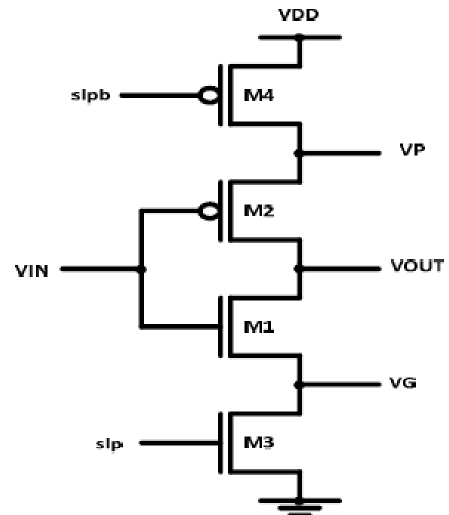


Figure 3. Sleepy Inverter

The sleepy inverter provides good leakage power reduction. However when it enters in to sleep mode it loses the state information. Sleep transistor technique can be applied to only pull down circuit of the inverter. This methodology is shown in figure 4. Though this circuit utilises one less sleep transistor at obvious area advantage, it suffers from higher average total power dissipation. A different power gating technique is suggested in [10]. This method is shown in figure 5. This technique provides low leakage and state retention at large total power consumption. Though this results in good output during active mode, produces higher average power during pulsed operation. The sleepy keeper approach of [7] is shown in figure 6.This technique results in state retention but at reduced voltage levels. As has been concluded by the author of [7], this circuit operation has resulted in to large total power dissipation and thus needs to be cautiously used.

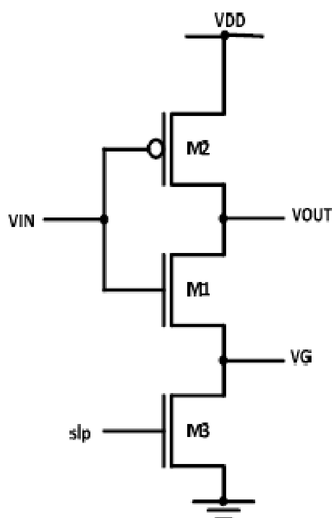


Figure 4. Pull Down Sleepy Inverter

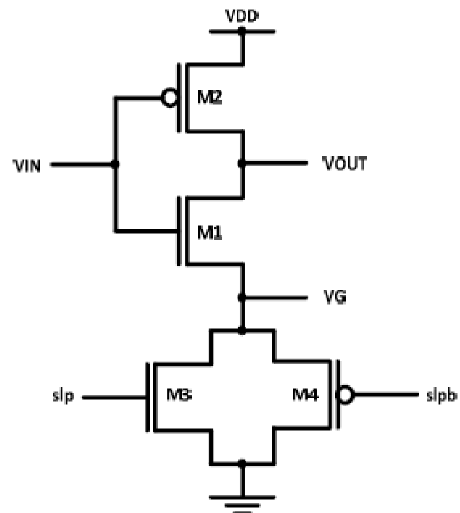


Figure 5. Power Gated Inverter

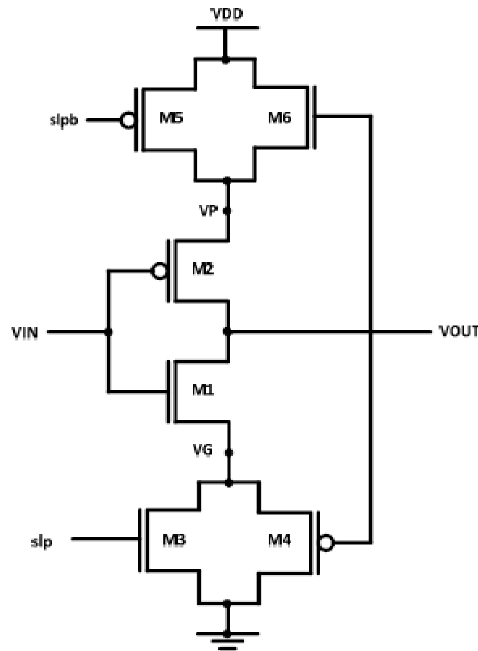


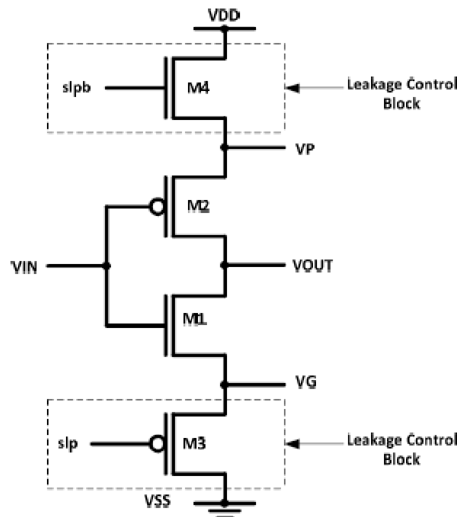
Figure 6. Sleepy Keeper

3.2. Proposed Low Leakage Sleepy Inverters

3.2.1 Novel Sleepy Inverter:

The novel technique for low leakage operation of an inverter is depicted in figure 7. This new sleepy inverter though provides good leakage power reduction; the voltage levels at the output are not at good logic1 and logic 0 values. However this larger reduction in leakage power can be utilised in inverter chains which are used in peripheral circuits of SRAM memory systems, such as data input/output driver, address input/output driver, row pre decoder, word line driver, row decoder etc. if reduced voltage levels are not a limiting factor.

The new sleepy inverter makes use of PMOS transistor as the pull down sleep transistor and NMOS transistor as the pull up sleep transistor. During active operation the sleep signal slp is held at logic 0 value and sleep bar signal slpb is held at logic 1 value. During the active period the two sleep transistors M3 and M4 are on. The node VG is at a higher potential than ground and the node VP is at a lower potential than VDD. The inverter circuit thus sees lower potential difference across nodes VP and VG. Thus the current though the circuit reduces and power dissipation comes down. For the standby mode of operation the signal slp is made logic 1 and signal slpb is made logic 0. Transistor M3 and M4 are off and provide a very high impedance path between VDD and ground and leakage current is lowered. The power dissipation during this standby mode of operation is the lowest.



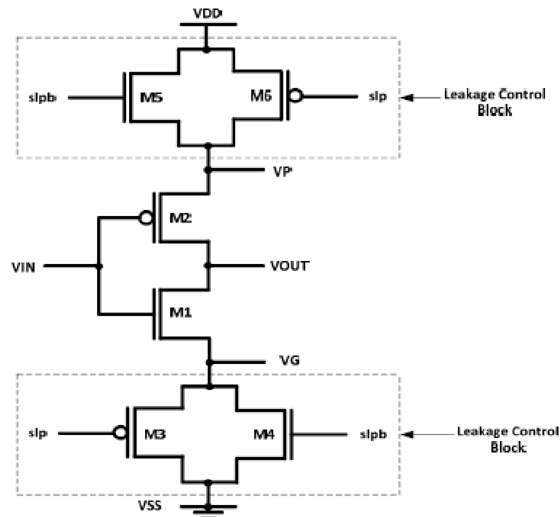


Figure 7. Novel Sleepy Inverter

Figure 8. State Retention Inverter

3.2.2 State Retention Low Leak Inverter

The novel low leak sleepy inverter though provides excellent low leakage power operation, has degraded output voltage levels during active mode of operation. The inverter output is not at good logic levels. During sleep (standby) mode of operation, the last output state is also not retained. To address these issues, a state retention transistor is connected in parallel to the sleepy transistors in the circuit of low leak sleepy inverter. The proposed state retention low leak inverter is shown in figure 8. An NMOS transistor is connected in parallel to PMOS pull down to achieve state retention; a PMOS transistor is used to maintain the last state during sleep in the pull up path in parallel to NMOS sleep transistor. During Active mode operation the sleep signal slp is maintained at logic 0 value and slpb is held at logic 1 value. These sleep signals cause both pairs of P and N transistors in the pull up and pull down path to be on. The output is at good logic levels. During sleep (standby) mode of operation sleep signals slp and slpb are held at logic 1 and 0 values respectively. Both the pairs of sleep transistors are off and hence reduced leakage current and lower power dissipation.

The state retention Inverter has four modes of operation.

i) Active mode : both sleep signals are used to switch on the sleep transistors M3,M4,M5 and M6 by making slp=0 and slpb = 1.The circuit sees good ground and VDD potentials and provides satisfactory output voltage levels.
ii) Deep Sleep mode: both sleep signals are used to switch off the sleep transistors M3,M4,M5 and M6 by making slp=1 and slpb = 0.The connection to ground and VDD is broken and a very high resistance path is established between VDD and ground. The leakage current is thus lowered significantly.
iii) State Retention with good 1: The sleep signals are maintained at slp=0 and slpb = 0.The connection to ground is at VG and full VDD is provided. The state retention
takes place with low leakage current.

iv) State Retention with good 0: The sleep signals are maintained at slp = 1 and slpb = 1.The connection to ground is complete and virtual VDD is provided. The state retention takes place and leakage current is lowered due to one off transistor.

4. LOW LEAKAGE DRIVER CIRCUITS

Recent surveys indicate that leakage power in SRAM peripheral circuits such as input, output drivers, word-line drivers, address decoders are now the main sources of leakage [11]. Since the peripherals usually drive a large number of memory cells, they experience a high capacitive load. To drive such high capacitive load, a chain of inverter buffers of increasing sizes by a factor of e is used with 4-6 levels. Leakage power of a standard memory cell is significantly lower than the leakage power of inverter buffers and inverter leakage power grows exponentially with its size. The combined leakage power of these drivers will be larger than the leakage of memory cells. Low leak inverter chains are designed in this work.

The conventional inverter driver chain as a word line driver is shown in figure 9. The leakage power is reduced by using sleep transistors as shown in figure 10.The SRAM peripherals like word line driver, data driver etc. make use of such inverter buffer chains to provide the large current required for these drivers. The word line driver used to drive the word select signal in typical SRAM memory systems can be converted in to a low power circuit by use of sleepy inverters. The circuit is enabled in the active state by keeping slp and slpb signals in logic 1 and logic 0 values respectively. The sleepy word driver enters in to sleep (standby) state by de asserting the signals slp and slpb in to logic 0 and logic 1 values respectively. This driver circuit functions as a normal inverter during active mode of operation. During sleep (standby) mode of operation, all the NMOS transistors in the pull down sleep path and all the PMOS transistors in the pull up sleep path enter in to off state. Due to the well known stack property already explained for sleepy inverter, the leakage power gets reduced.

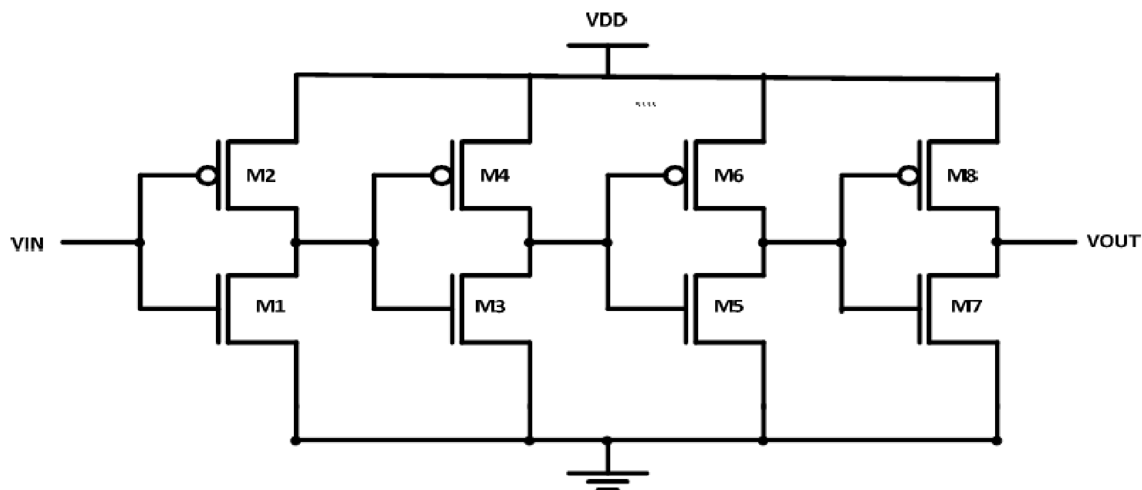


Figure 9. Inverter chain

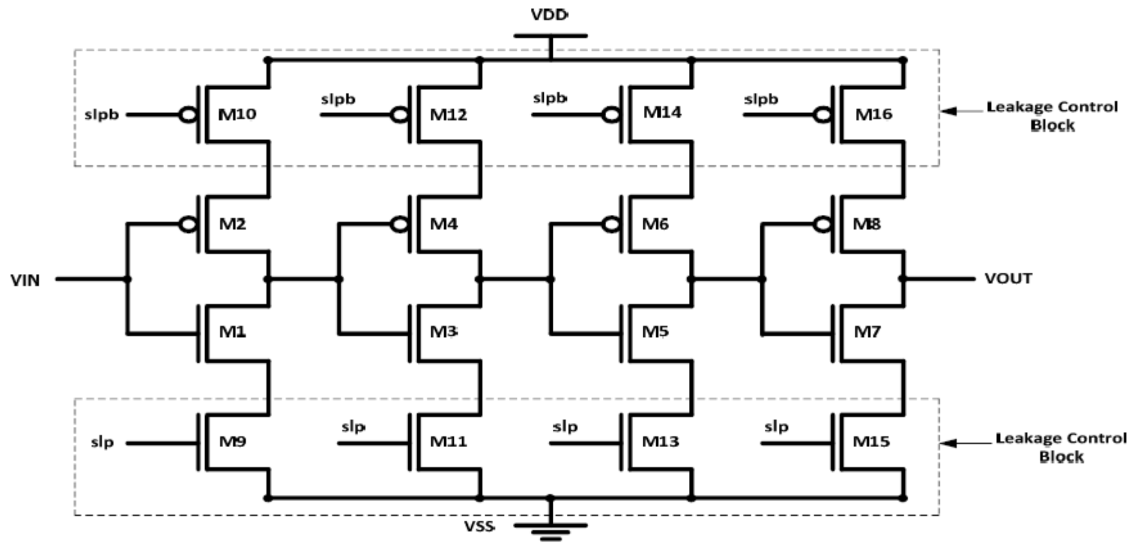


Figure 10. Sleepy Inverter chain

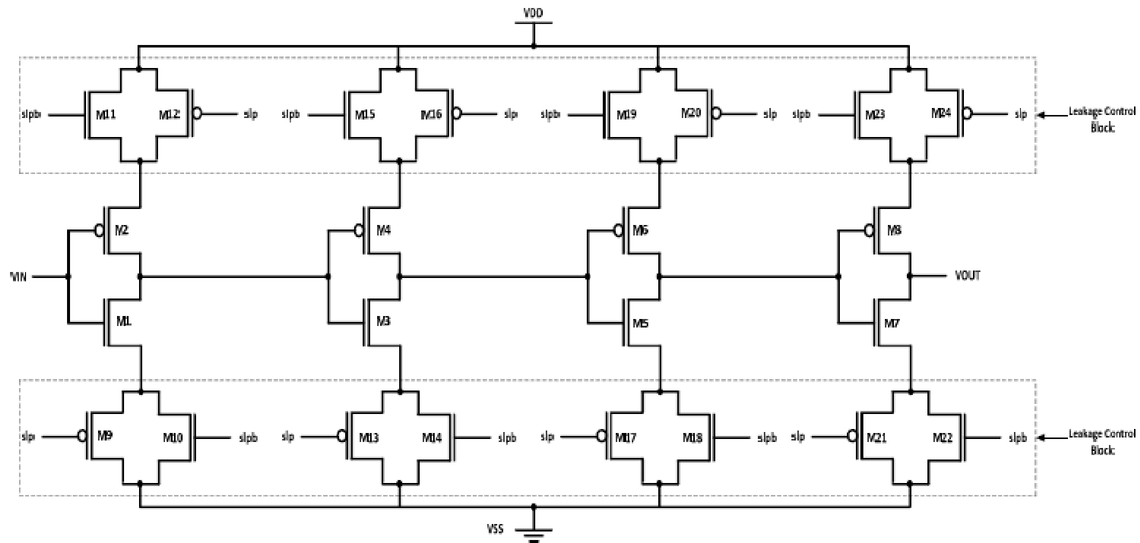


Figure 11. Sleepy Inverter chain with state retention

The low leak word driver circuit can be designed by making use of low leak sleepy inverter of figure 7. However in this case the output peak to peak voltage during active period is at a lower value due to the lower potential difference seen by the circuit. When such an inverter chain is used to drive other circuits which provide logic restoring, the reduced output may not be a critical issue. However while developing inverter buffer chains; this lowered output voltage in the active mode of operation may hinder the required drive. To overcome this problem an inverter chain is realised using novel state retention inverters of figure 8. The novel sleepy word driver circuit using sleepy state retention inverters is shown in figure 11.

Active mode of operation:

The sleep signal slp drives the PMOS sleep transistors and sleep signal slpb drives NMOS sleep transistors. The sleep signals are applied to the inverter buffer stages in order to operate them in active mode. The slp signal is made active 0 and slpb is made active 1. So the appropriate PMOS and NMOS transistors in the power gating circuit are switched on to provide low power operation. Thus the inverters in the word driver function as inverters with good output voltage and reduced power due to stack effect.

Standby mode of operation:

During standby mode of operation the sleep signals slp is made high and slpb is made low. This causes the PMOS and NMOS transistors in the power gating circuit to be switched off and provide lower leakage current flow through the off transistors.

State Retention

The state retention can be achieved by making both of the sleep control signals 0 or 1.

5. SIMULATION AND RESULTS

The circuit design is carried out using 90 nm CMOS technology files. All the designs are done and simulation is performed in cadence design environment. The static power dissipation and total (average) power dissipation are measured using cadence tools. The power dissipation is measured both during active mode and standby mode of operations, for all the inverters and drivers.

The simulation of inverters and driver circuits is performed by applying slp and slpb signals with 1microsecond period and variable pulse widths. Active mode operation is observed by keeping these signals in the logic states as explained in section 3. Long sleep (standby) period is also introduced to observe the performance during inactive period. The sleep inverter using novel technique has exhibited lower leakage current and lower power. However during active mode lower output voltage is observed at correct functionality. The state retention inverter has resulted in good voltage levels during active mode excellent power reduction during sleep mode and state retention property.

The static and average power dissipation during all operating modes is measured by using cadence result browser and calculator. Table 1 compares the static power dissipation of all the inverters during active mode i.e. when sleep control signals slp and slpb hold the respective sleep transistors in the on state and the logic inverter behaves as a normal inverter. Table 2 provides the static power dissipation during sleep mode of operation for all the inverters discussed in section 3. Average power dissipation for all the inverters is provided in the Table 3. The input signal is taken as a clock of 2 nanoseconds period and transition period is taken as 2
microseconds duration for all the circuits. The sleep control signals of same pulse width and period are applied to all the inverters for the sake of comparison. The sleep signal slp is in the pull down path and sleep signal slpb is used in the pull up path. Depending upon whether PMOS or NMOS sleep transistor is driven, slp and slpb assume logic states to make them on or off. The

logic values of these sleep signals for different modes of operation in case of different inverters are provided in the tables of observation.

Table 1. Inverter Static Power Dissipation (ACTIVE MODE)

S.NO.	Inverter	Power(watts) Vin=0	Power(watts) Vin=1
1	Inverter	3.8135 E-08	4.1564E -10
2	Sleepy Inverter (both P.U.& P.D.) slp=1,slpb=0	3.8423 E-08	8.3954 E-10
3	Sleepy Inverter (only P.D.) slp=1	3.8012 E-08	4.1564 E-10
4	Power gate Inverter slp=0,slpb=1	3.8012E-08	4.1564 E-10
5	Sleepy keeper slp=1,slpb=0	3.8618 E-08	9.8151E-10
6	Novel sleepy inerter slp=0,slpb=1	**6.0301 E-10**	**9.0523 E-11**
7	State retention inverter slp=0,slpb=1	**3.8238 E-08**	**5.8514 E-10**

Table 2. Inverter Static Power Dissipation (SLEEP MODE)

S.NO.	Inverter	Power(watts) Vin=0	Power(watts) Vin=1
1	Inverter	N.A.	N.A.
2	Sleepy Inverter (both P.U.& P.D.) slp=0,slpb=1	2.4009 E-10	1.0622 E-11
3	Sleepy Inverter (only P.D.) slp=0	1.7831 E-09	3.7323 E-10
4	Power gate Inverter slp=0,slpb=1	1.7827 E-09	3.7319 E-10
5	Sleepy keeper slp=0,slpb=1	1.2095E-09	1.3714E-11
6	Novel sleepy inerter slp=1,slpb=0	**4.449 E-12**	**4.8328E-13**
7	State retention inverter slp=1,slpb=0	**4.4614E-10**	**6.8113E-12**

Table 3. Inverter Total (Average) Power Dissipation

S.NO.	Inverter	Power during clocked opration (watts)
1	Inverter	405.601 E-09
2	Sleepy Inverter (both P.U.& P.D.)	3.721 E-09
3	Sleepy Inverter (only P.D.)	57.630 E-09
4	Power gate Inverter	59.781 E-09
5	Sleepy keeper	13.852 E-09
6	Novel sleepy inerter	**3.150 E-09**
7	State retention inverter	**3.664 E-09**

Table 4. Static Power Dissipation of Inverter Buffer Chains (ACTIVE MODE)

S.NO.	Driver	Power (watts) Vin=0	Power (watts) Vin=1
1	Inverter Driver	1.1372 E-07	1.6621 E-07
2	Sleepy Inverter Driver slp=1,slpb=0	1.1864E-07	1.7082 E-07
3	State retention inverter driver (slp=0,slpb=1)	**1.1418 E-07**	**1.6617 E-07**

Table 5. Static Power Dissipation of Inverter Buffer Chains (Sleep Mode)

S.NO.	Driver	Power(watts) Vin=0	Power(watts) Vin=1
1	Inverter Driver	N.A.	N.A.
2	Sleepy Inverter Driver slp=0,slpb=1	2.4558 E-09	1.9185 E-09
3	State retention inverter driver (slp=1,slpb=0)	**2.04172 E-09**	**1.6848 E-09**

Table 6. Total (Average) Power Dissipation of Inverter Buffer Chains

S.NO.	Driver	Power(watts) Clocked Operation
1	Inverter Driver	14.44 E-06
2	Sleepy Inverter Driver	151.03 E-09
3	State retention inverter driver	**150.12 E-09**

6. CONCLUSION

All the inverters and inverter buffer chains are simulated in 90nm CMOS technology in cadence design environment. The novel sleepy inverter provides very good leakage power reduction of X 60. However it has low output levels. This Technique can be utilised in situations which do not demand good voltage levels. The state retention inverter has resulted in good leakage power reduction as well as the previous output state can be retained. The dynamic power reduction is also lower compared to sleepy keeper inverter by X3.5. The low leakage power and lower total power dissipation for the novel circuit techniques is obtained by using single VTH transistors unlike many earlier techniques which use dual VTH transistors to achieve low power operation.

The buffer chain can also be realised using novel state retention inverter to provide lower leakage and state retention.

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