EFFECT OF EQUAL AND MISMATCHED SIGNAL TRANSITION TIME ON POWER DISSIPATION IN GLOBAL VLSI INTERCONNECTS

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ABSTRACT

High density chips have introduced problems like crosstalk noise and power dissipation. The mismatching in transition time of the inputs occurs because different lengths of interconnects lead to different parasitic values. This paper presents the analysis of the effect of equal and unequal (mismatched) transition time of inputs on power dissipation in coupled interconnects. Further, the effect of signal skew on transition time is analysed. To demonstrate the effects, a model of two distributed RLC lines coupled capacitively and inductively is taken into consideration. Each interconnect line is 4mm long and terminated by capacitive load of 30fF. The analysis is carried out for simultaneously switching lines. The results are obtained through SPICE simulations and waveforms are generated.

KEYWORDS

Equal / Unequal rise time, Power dissipation, simultaneous switching, Signal Skew

1. INTRODUCTION

The growth of VLSI circuits is largely dependent on technology scaling. The integration of more and more functionalities on chip causes die size to increase which results in complex geometry of interconnect wires on chip. With technology advancement, on chip interconnects have turned out to be more and more important than transistor resource [1], [2]. As per international technology roadmap for semiconductors (ITRS) [3], the gap between interconnection delay and gate delay will increase to 9:1 and on-chip wire length is expected to increase to 2.22 km/cm^2 for future nanometer scale integrated circuits. So, for high speed high density chips, the chip performance is mostly affected by the interconnections rather than device performance.

The decrease in interconnect width and thickness leads to increase in resistance while short spacing between them progressively increases the parasitic capacitance. With high clock speed, faster signal rise time and longer wire lengths, the inductance of interconnect significantly plays a major role in on-chip circuit performance [4]. Due to the presence of these line parasitics effect, the *RLC* distributed model or transmission line model [2], [5] is more effective in current technology. The short spacing between interconnect wires, longer wire lengths and high operational frequency causes significant value of coupling parasitics i.e. mutual inductance (M) and coupling capacitance (C_C) in the circuit. The resulting effect of these parasitics is crosstalk noise, propagation delay and power dissipation. These performance parameters affect the signal integrity.

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The denser designs of integrated circuits introduce problems of power dissipation. So, the power analysis of integrated circuits becomes an important issue of study. Small power consumption makes the circuit/device more reliable. The CMOS circuits are best known for its low power consumption. Below submicron technology, the power consumption per unit area of CMOS chip has risen tremendously. Some of the factors affecting the power consumption are input voltage level, input transition time, output loading and power dissipation capacitances. The power dissipation in CMOS circuit consists of two components i.e. static and dynamic dissipation. The static power component is the result of leakage currents and sub-threshold currents and is quite low. The dynamic power dissipation, which is due to charging and discharging of parasitic capacitive load of interconnects and devices, contributes dominantly. The dynamic power dissipation may be written as

$$P = KC_T{V_{dd}}^2 f \tag{1}$$

In Eq.(1), C_T comprises of various capacitances i.e. interconnect parasitic capacitance, load capacitance (C_L) and drain and source capacitances. The V_{dd} is power supply voltage, f is operating frequency and K is switching activity factor. There are two factors affecting the dynamic power dissipation viz. clock speed and transistor density. If the transistors are switching more rapidly, the power dissipation will be more. The dynamic power dissipation is due to switching current and through current. The through current is due to short circuit path between supply and ground rails during switching and is dependent on the input rise/fall time, the load capacitance and gate design [6]. The power dissipation due to through current is always substantially smaller than switching power. To obtained the total power dissipation (Eq.(2)), the three dissipation components may be added [6],

$$P_{Total} = P_{Static} + P_{Dynamic} + P_{Short\ circuit} \tag{2}$$

A great deal of research has been done on the analysis of crosstalk noise and delay [7], [8], [9], [10], [11], [12]. However, researchers have reported the power dissipation in interconnects considering different aspects. Power related issues of CMOS in nanometer regime are reported in [13]. The analysis of power consumption in optimally buffered single line RC model is reported in [14]. The power dissipation is analyzed against variations in interconnect width for uncoupled line [15]. Power dissipation is analyzed against variations in load for capacitively coupled interconnects [16]. A method for analyzing power distribution using reduced order model is reported in [17]. This paper is an extended version of [18]. Firstly, this paper re-addresses the power dissipation dependencies on equal and unequal transition time of inputs in capacitively and inductively coupled interconnects. The analysis is equally important because of the fact that the two inputs may have different transition time due to different length of interconnects. Secondly, this paper addresses the effect of skew on signal transition time. Skew is the difference between actual and expected arrival time of the pair of signals. Some of the factors affecting signal skew are process variation, wire and coupling parasitics, clock loading. The signal skew is dependent on wire delay which in turn depends on many factors. The impact of signal skew on delay and overshoot noise is presented in [9]. The effects of coupling parasitics on skew are analyzed in [19].

This paper is organized in four sections. Section 2 describes the simulation setup of interconnect model under consideration. The effects of equal and unequal (mismatched) transition time of inputs to two interconnect lines on power dissipation are observed and discussed in section 3. The analysis of the effects of skew on signal transition time is presented in section 4. Finally, section 5 concludes this paper.

2. SIMULATION SETUP

For analysis, two uniformly distributed *RLC* lines coupled capacitively and inductively as shown in Fig. 1. are simulated. . The length of each interconnect is taken as 4mm and each line of coupled structure is 2 µm wide, 0.68 µm thick and separated by 0.24 µm [12]. The global interconnect is taken into consideration and it is assumed that there are several metal layers available for the interconnects

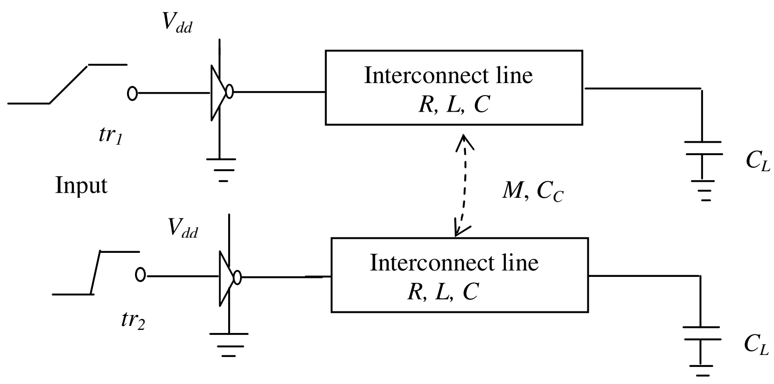

Figure 1. Coupled lines

$$R = \begin{bmatrix} 12{,}500 & 0 \\ 0 & 12{,}500 \end{bmatrix} \qquad C = \begin{bmatrix} 190p & -64p \\ -64p & 190p \end{bmatrix} \qquad L = \begin{bmatrix} 1.722\mu & 1.4\mu \\ 1.4\mu & 1.722\mu \end{bmatrix}$$

Figure 2. Line parasitic matrices

It is well accepted that the simulations of a distributed RLC interconnect line matches more accurately the actual behavior as compared to lumped model [2]. So, fifty distributed lumps of gamma type are taken for the length of interconnect under consideration. The parasitics values are obtained from expressions reported in [20], [21]. The far end of interconnect lines are terminated by a capacitive load of 30 fF. The interconnect parasitics matrices for one meter length are shown in Fig. 2. The simulations use an IBM 0.13 µm technology node with copper interconnect process (MOSIS) with a power supply voltage of 1.5 V. The width of driver PMOS and NMOS are taken as 70 µm and 35 µm respectively. To carry the analysis, results are obtained through SPICE simulations and waveforms are generated.

3. IMPACT OF EQUAL AND UNEQUAL TRANSITION TIME OF INPUTS

The transition time is defined as the time for a signal to go from 10 % to 90 % of its final value. The power dissipation is dependent on the supply current which in turn is sensitive to input transition time. In this section, the impact of equal rise time ($tr_1 = tr_2$) and unequal rise time ($tr_1 \neq tr_2$) of inputs to the two interconnect lines (Figure 1) are observed. The unequal rise time is because of different lengths of wire which maps into different parasitic values.

For analysis, the rise time of both the inputs is varied equally from 10 to 760 ps. In case of unequal rise time of inputs, the difference i.e. $\Delta tr = tr_1 \sim tr_2$ is varied from 0 to 750 ps. The interconnect model under consideration is SPICE simulated for equal and unequal transition time of inputs. The two cases of simultaneously switching inputs are taken into consideration i.e.

Case I: Both inputs are switching in same phase i.e. from high to low or from low to high.

Case II: Both inputs are switching in opposite phase i.e. aggressor input in switching from high to low and victim input is switching from low to high.

3.1 Results and Observations

To show the impact of equal and unequal rise time of inputs on power dissipation, the waveforms are generated as shown in Figure 3-6.
From these figures, following observations are drawn.

(i) For in-phase switching of inputs, it is observed from Figure 3 that there is wide variation of power dissipation for high to low switching. However, the power dissipation is quite low for low to high switching. This is from the fact that for high to low switching of driver inputs, the parasitics are charging. After the parasitics get charged, the power dissipation is minimum. Also, for low value of rise time, the inductive effect becomes prominent. For low to high switching of driver inputs, the parasitics are discharging. So, power consumption is low. Furthermore, it is observed that the peak value of power dissipation for in-phase switching of inputs is 14.1mW for the specified range of rise time under consideration.

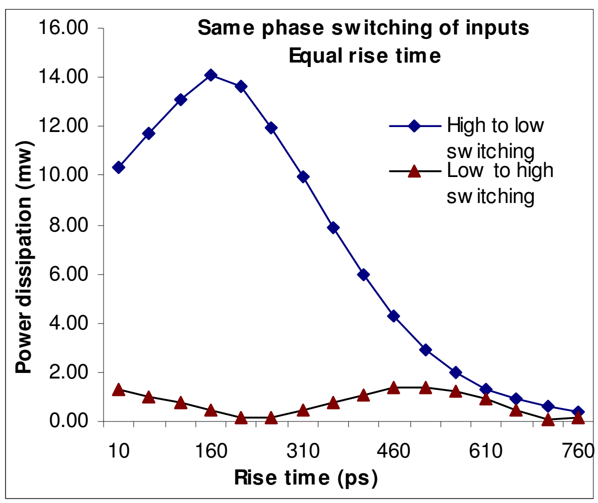

Figure 3. Power dissipation as function of rise time for in-phase switching

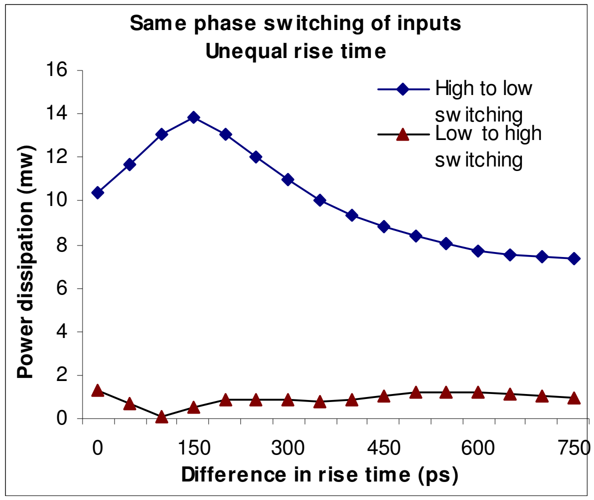

Figure 4. Power dissipation as function of Δtr for in-phase switching

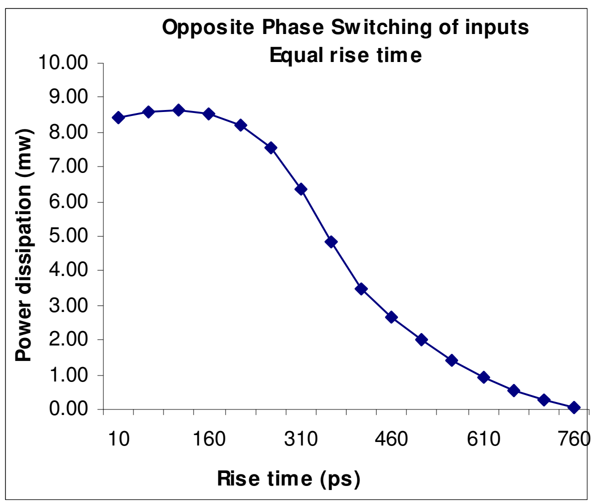

Figure 5. Power dissipation as function of rise time for out-of-phase switching

(ii) Figure 4 shows the simulation results for in-phase switching wherein difference in rise time (Δtr) is varied by taking into consideration both the transitions from high to low and low to high. It is observed that, for inputs switching from high to low, the power dissipation first increases and then starts decreasing monotonically. However, the power dissipation when inputs are switching from low to high is quite low as compared to high to low for the specified range of Δtr under consideration. The reason can be explained in the similar way as explained earlier. Furthermore, it is observed from Figure 4 that the maximum power dissipation for this case is 13.8 mW.

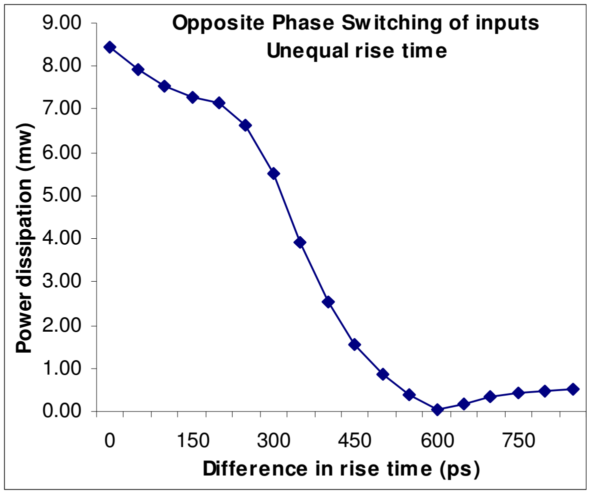

Figure 6. Power dissipation as function of Δtr for out-of-phase switching

(iii) For opposite phase switching and equal rise time of inputs (Figure 5), it is observed that the power dissipation decreases with increasing rise time. In this case, it is observed that the maximum power dissipation is 8.66 mW which is reasonably smaller than the value of maximum power dissipation observed in case of same phase switching of inputs. However, at large values of rise time in the specified range, the power dissipation for the two cases of simultaneous switching (Case I and Case II) is quite low.

(iv) From Figure 6, it is observed that, with increasing Δtr, the power dissipation decreases dramatically and a minima of value 0.0423 mW occurs at 600ps difference in rise time.

4. EFFECT OF SIGNAL SKEW ON TRANSITION TIME

Skew is the time difference (Δ) between the actual and expected arrival times of a pair of signals as illustrated in Figure 7. Signal skew is dependent on wire delay. Since, wire delay is dependent on many factors, one of those is signal transition time, so, signal skew will have some effect on signal transition time. In this section, the analysis of the effect of skew on signal rise time is carried out for the two cases of simultaneously switching lines. To observe the effects, skew is varied from 5ps to 95ps in steps of 10ps. The coupled model is simulated and the rise time (10% to 90% of signal final value) is observed at far end of lines.

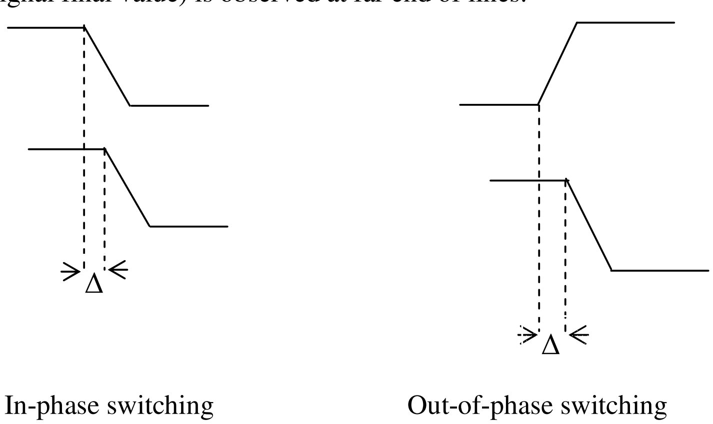

Figure 7. Signal Skew

4.1 Results and Observations

The rise time observed for in-phase and out-of-phase switching of lines with growing signal skew is shown in Figure 8. From this figure, it is observed that the rise time increases with increasing signal skew for the two cases of simultaneous switching of lines under consideration. This is from the fact that with increasing skew, the overlapping in the transition region of the two signals decreases, so, inductive coupling reduces. It is further observed from the figure that, for opposite phase switching of inputs, the rise time is large as compared to in-phase switching at all values of signal skew for the specified range.

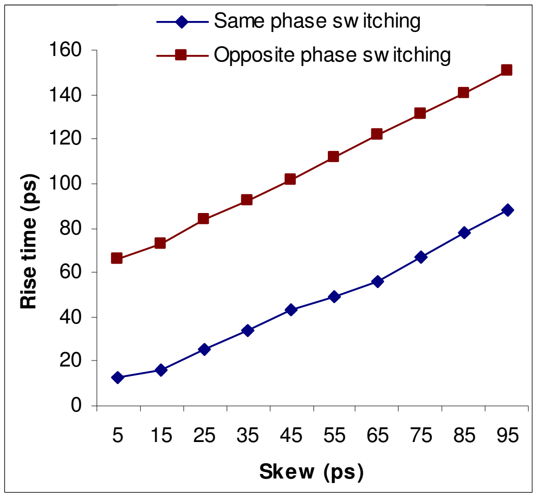

Figure 8. Rise time as function of signal skew

5. CONCLUSION

This paper addressed the power dissipation issues in inductively and capacitively coupled VLSI interconnects for simultaneously switching inputs. The results have been analyzed for equal and unequal (mismatched) rise time variations. For in-phase switching of inputs, it is observed that the maximum value of power dissipation is 14.1 mW for the specified range of rise time. However, the power dissipation is quite low for low to high switching mode. Furthermore, for opposite phase switching of inputs, the power dissipation decreases monotonically with increase in rise time of inputs equally. It has also been shown that the signal transition time is dependent on skew. It is observed that the signal rise time increases with increasing skew for simultaneously switching lines.

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