LOW POWER DYNAMIC BUFFER CIRCUITS

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ABSTRACT

In this paper we propose two buffer circuits for footed domino logic circuit. It minimizes redundant switching at the output node. These circuits prevent propagation of precharge pulse to the output node during precharge phase which saves power consumption. Simulation is done using 0.18µm CMOS technology. We have calculated the power consumption, delay and power delay product of proposed circuits and compared the results with existing standard domino circuit for different logic function, loading condition, clock frequency, temperature and power supply. Our proposed circuits reduce power consumption and power delay product as compared to standard domino circuit.

KEYWORDS

Buffer, Dynamic circuit, Power consumption, Delay, Precharge pulse.

1. INTRODUCTION

Domino logic circuits are used in wide applications such as microprocessor [1], memory [2], digital logic [3], etc. It has superior advantage over static logic circuit, it require less number of transistor count and reduces output load capacitance hence enhance the speed. Realization of wide fan-in OR gate using static logic circuit requires long stack of PMOS which is not practical, it increase the delay and area. But domino logic use dual phase namely precharge and evaluation to implement complex circuit with single evaluation network [4].Domino circuit has drawback of high power consumption due to clock loading and reduce noise margin due to charge sharing and charge leakage. Charge sharing is compensated by adding keeper transistor.

Buffer is required to drive the output of the domino logic circuit into the next stage [5]. It is seen that static logic circuit consume power due to redundant switching at the output node. But domino logic circuit consumes power due to redundant switching at dynamic and output node [6]. This redundant switching increase the power consumption. Different techniques are proposed in the literature to deal this issue. True single phase clock (TSPC) based domino logic [7] and limited switch dynamic logic (LSDL) [8] reduces the output node redundant switching. TSPC based domino logic require extra clock transistor, overhead the clock loading. Similarly, latch is added in LSDL at dynamic node, it increases the area. Power dissipation of the domino circuit is divided into three components [9]:

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$$P_{Total} = P_{Dynamic} + P_{Leakage} + P_{Short\ Circuit} \quad (1)$$

$P_{Dynamic}$ is the power consumed during capacitance charging and discharging, $P_{Leakage}$ is the total leakage power of the circuit and this power increases as the technology is scaled down, and $P_{Short\ Circuit}$ is the power dissipated when direct current flows from power supply to ground.

$$P_{Dynamic} = \propto \times C \times VDD^2 \times Fclk \quad (2)$$

Where $\propto$ is the switching activity at the output and dynamic node, it depends on the gate topology and inputs, C is the capacitive load at the evaluation node, F_{clk} is the clock frequency.

$$P_{Leakage} = I_{Leakage} \times VDD \quad (3)$$

where $I_{Leakage}$ is the combination of subthreshold and gate oxide leakage current.

$$P_{Short\ Circuit} = \propto \times I_{SC} \times VDD \quad (4)$$

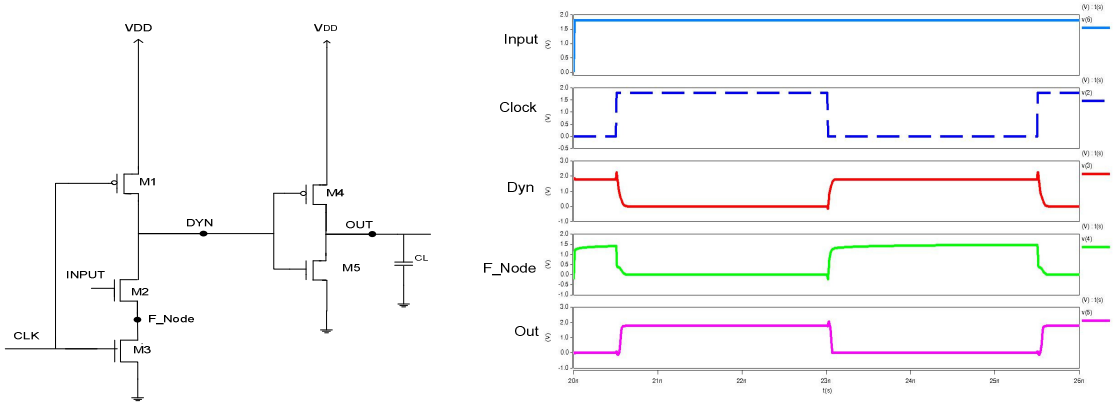
I_{SC} for domino logic gate is the contention current that flows between the evaluation network and pMOS keeper during evaluation mode. This power dissipation must be kept low for better operation of the domino circuit.

In this paper, we propose two switching-aware techniques which minimize redundant switching at the output node. The remainder of the paper is organized as follows. Previous proposed techniques are described in section 2. Proposed circuits are proposed in section 3. Simulation results are presented in section 4, and conclusion is presented in section 5.

2. PREVIOUS WORK

Standard domino logic is shown in Fig. 1(a). Operation of the circuit is divided into two phase. When clock is low, precharge phase, pull up transistor M1 is ON and footer transistor is OFF. Dynamic node is charged to VDD and output node discharge to zero voltage. Parasitic capacitance at node F_Node is charged to high. During evaluation phase, M3 is ON, dynamic node is discharge it depends on the input of the circuit. When input is kept low, dynamic node maintain high in both operating phase. When input is kept high and operation of the circuit in two operating phase is characterized in Fig. 1(b).During prechrage phase dynamic node and F_Node is charge to high voltage and output is discharge to low voltage. During evaluation phase dynamic and F_Node is discharge to low voltage and output is charge to high voltage [10]. Here propagation of precharge pulse to the output of the circuit and output logic is unstable. This redundant switching increase the power consumption.

Circuit techniques have been proposed in the literature such as TSPC based domino logic and limited switch dynamic logic (LSDL).Main idea regarding these circuit design is to reduce redundant switching at the output node.

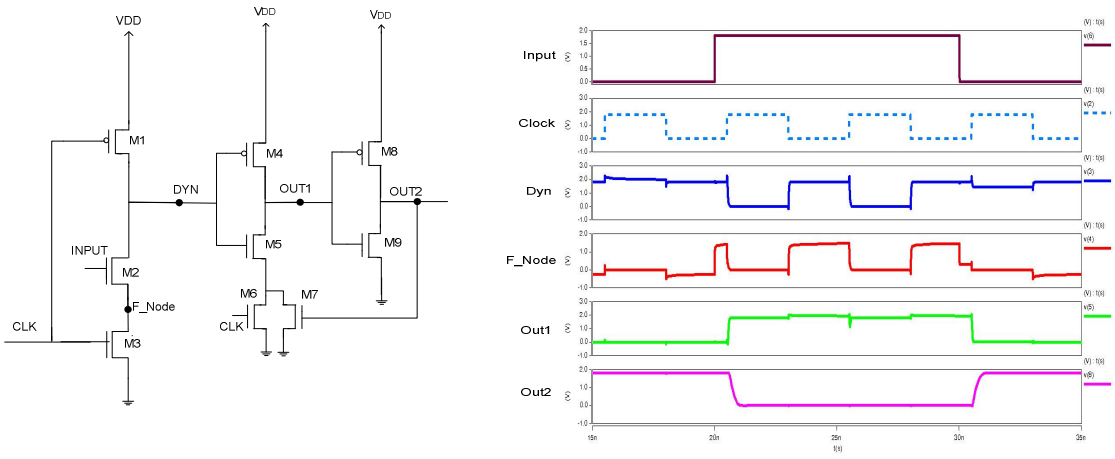


(a) (b)

Figure 1. (a) Standard domino circuit, (b) Its selected node characteristics.

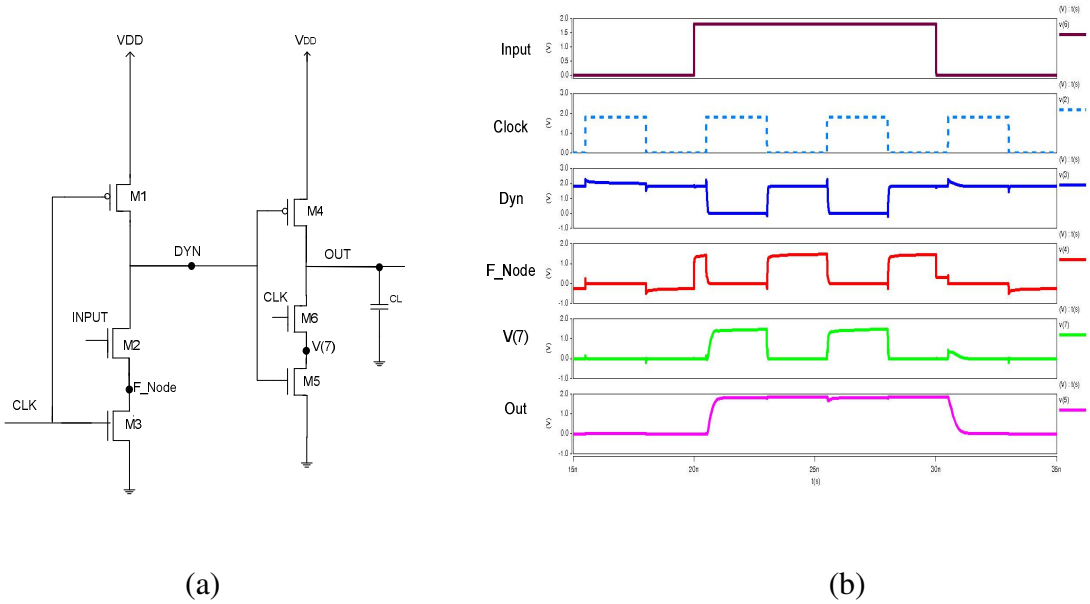
2.1. Limited switch dynamic logic (LSDL)

Limited switch dynamic logic (LSDL) [8] is shown in Fig 2(a) and its voltage characteristics in Fig. 2(b). This circuit is similar to the standard domino logic circuit except latch structure is added at the dynamic node. This latch structure consists of M4, M5, M6, and M7.Transistot M4 and M5 prevents back propagation of the latch signal to the dynamic node. This increases the parasitic capacitance at the dynamic node and eliminates the redundant switching at the output node but fails at dynamic node. LSDL provides dual output at OUT1 and OUT2 without the need of dual rail signalling. There are two drawback of LSDL, first it requires latch circuit to every dynamic node which increases the power consumption and the area, second it need three clock transistor which increases the load capacitance of the clock signal.



(a) (b)

Figure 2. Limited switch dynamic logic circuit, (b) Its selected node characteristics [8].



(a) (b)

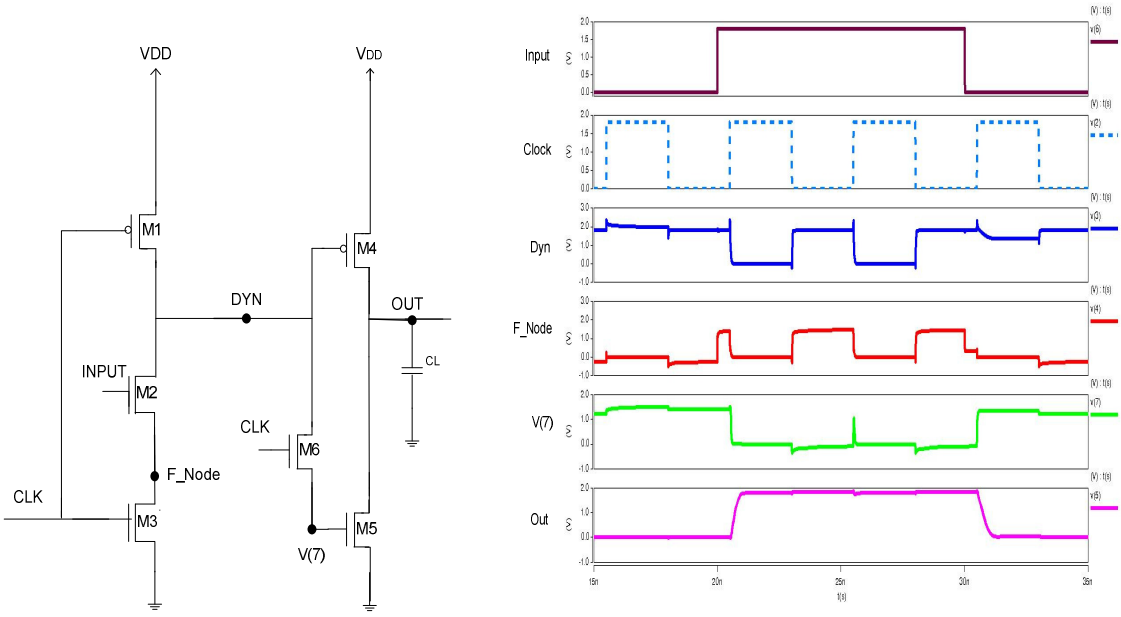
Figure 3. (a) TSPC dynamic logic circuit, (b) Its selected node characteristics [7].

2.2. True Single Phase Clock (TSPC) Dynamic Logic

TSPC dynamic logic [7] is shown in Fig. 3(a) and its characteristics at different node is shown in Fig. 3(b). This circuit is similar to standard footed domino logic except extra nMOS transistor is connected in the output inverter. This circuit requires 3 clock transistor and it increase the load capacitance of the clock signal and the power consumption. In this circuit, during precharge phase transistor M6 is OFF which helps the output to hold its previous value.

3. PROPOSED CIRCUITS

Propagation of precharge pulse during precharge phase in standard domino logic circuit increases the switching activity at the dynamic node and output node. This increases the power consumption and output node is unstable. This problem is overcomes by proposed circuit1 and proposed circuit2. Proposed circuits minimize redundant switching at output node.



(a) (b)

Figure 4. (a) Proposed circuit 1, (b) Its selected node characteristics.

3.1. Proposed Circuit 1

Circuit diagram of proposed circuit 1 is shown in Fig. 4(a) and its voltage characteristic at different node is shown in Fig. 4(b) .Implementation of this buffer, consist of extra transistor in the output inverter as compared to standard domino circuit. This circuit consists of three clock transistor M1, M3 and M6.The drain of M6 is connected to the dynamic node and its source is connected to the gate of transistor M5.Using this technique, it avoid precharge pulse not to propagates to the output node. Operation of this circuit is explained by considering the input logic. When input logic is low, dynamic node remains high regardless of operating phase and output node is kept low. When input is high, there are two different cases depending on the operating phase.

(a) During evaluation phase, dynamic node is discharge to ground. Transistor M4 turns ON and charges the output node to VDD. On the other hand, high clock turns ON the M6 which turns OFF the M5.M6 avoid short circuit current in the output inverter.

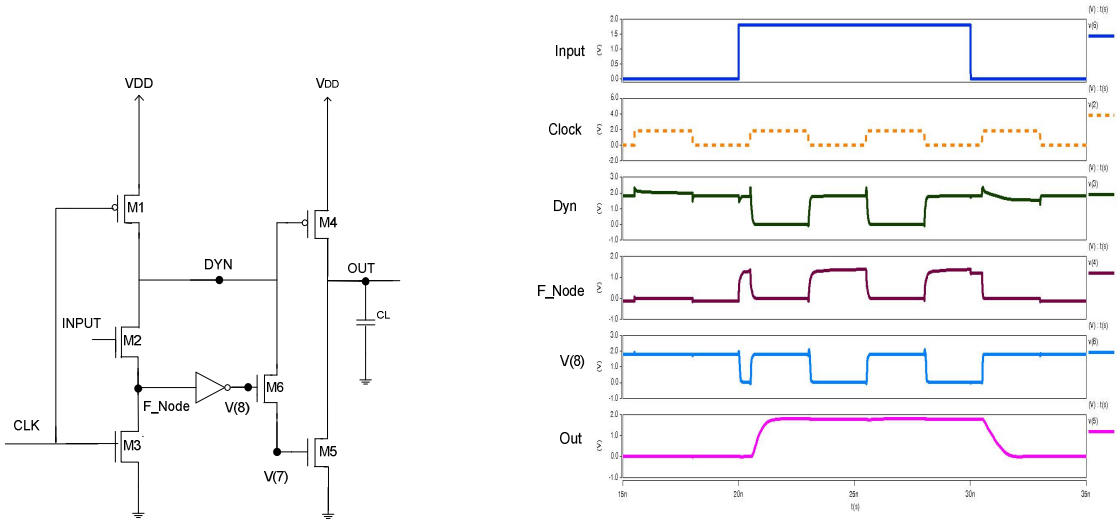
(b) During precharge phase, pull up transistor M1 turns ON and M3 turns OFF, dynamic node charged to VDD. Transistor M6 is OFF, which turns OFF the M5 and it helps the output node to hold the previous value. In this circuit topology, output node is isolated from ground during precharge phase means it helps to avoid propagation of precharge pulse to the output node.

3.2. Proposed Circuit 2

Circuit diagram of proposed circuit 2 is shown in Fig. 5(a) and their voltage characteristic at different node is shown in Fig.5 (b). This buffer is similar to previous circuit except gate of M6 is connected to F_Node through inverter. Advantage of this circuit is avoiding propagation of precharge pulse during precharge phase to the output node. Operation of the circuit is explained by considering the input logic. When input is low, F_node voltage is low, dynamic node remains high regardless of operating phase and output node is kept low. When input is high, F_Node voltage is similar to dynamic node voltage, there are two different cases depending on the operating phase.

(a) During evaluation phase, dynamic node and F_Node is discharge to ground. Output node is charged to VDD by M4.M6 turns ON due to low voltage at F_Node.M6 pass low dynamic voltage to the gate of M5, this turns OFF the M5.

(b) During precharge phase, transistor M3 is OFF, pull up transistor M1 precharge the dynamic node and F_Node is charge to high voltage due to parasitic capacitance at this node. High voltage at F_Node turns OFF the transistor M6, which turns OFF the M5 and it helps the output node to hold its previous value.



(a) (b)

Figure 5. (a) Proposed circuit 2, (b) Its selected node characteristics.

4. SIMULATION RESULTS

The proposed circuits are simulated using HSPICE in the high performance 180nm predictive technology [11].The supply voltage in the simulations is 1.8V and clock rate is 200MHz and with 50% duty cycle (clock period is 5ns) .Rise and fall time of the clock rate is set equal to 10ps. Transistor size is set by W_{PMOS} =27Lmin, W_p/W_n=2 for whole circuit. Worst case delay is

determined from input to the output node V_{out}. Power consumption is determined when input is high voltage. Standby power is measured when input of the circuit is low.

Comparison of power saving for various logic function of proposed domino circuits with standard domino circuit is tabulated in Table 1.In this comparison, clock frequency, input frequency and load capacitance were set to 200MHz,50MHz and 100Ff.From the table, increase of fan-in, increases the power consumption and OR gate logic consumes more power as compare to AND gate logic.

Table 1. Comparison of Power Saving with Different Logic Function in 0.18µm (VDD=1.8V, Clock Frequency=200MHz, Input Frequency=50MHz and load capacitance=100Ff)

Logic function	Standard Circuit	Proposed circuit 1	Proposed circuit2	Power saving by proposed circuit1	Power saving by proposed circuit 2
A	46.04	31.86	45.95	30.79%	0.19%
A.B	46.57	33.09	46.00	28.94%	1.22%
A+B	47.17	31.29	42.87	33.66%	9.11%
A.B.C	47.24	34.64	46.50	26.67%	1.56%
A+B+C	48.20	30.97	42.96	35.74%	10.87%
A.B.C.D	47.82	36.30	47.00	24.09%	1.73%
A+B+C+D	49.00	30.93	41.06	36.87%	16.24%

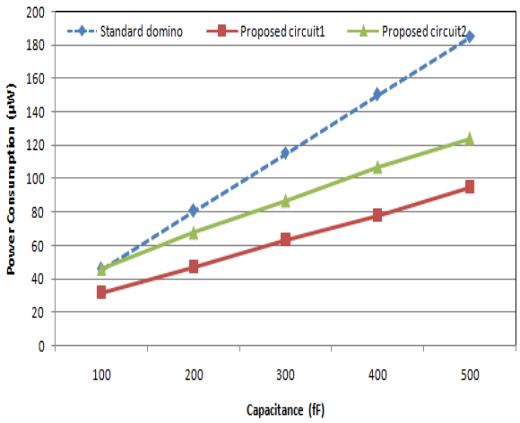


Figure 6. Power versus capacitance.

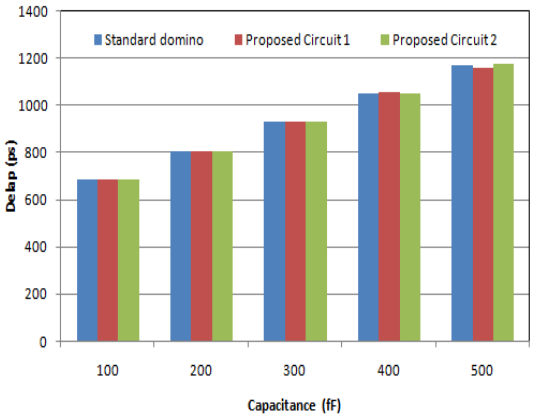


Figure 7. Delay versus capacitance.

Comparison of power consumption of proposed circuits and standard domino circuit with clock frequency 200 MHz for different loading condition is shown in Fig. 6. As a result, at higher load capacitance, our proposed circuits save higher power consumption as compared to standard domino circuit with little delay penalty is shown in Fig. 7 . Our proposed circuits have better power delay product and at higher load capacitance its saving is large as compared to standard domino circuit is shown in Fig.8. Proposed circuits also minimize the standby power as compared to standard domino circuit is shown in Fig.9.

Comparison of power consumption of proposed circuits with standard domino circuit, load capacitance is set 100fF for different clock frequency is shown in Fig.10. It shows power

consumption increase as clock frequency increases, maximum power saving is achieved at higher operating frequency, reduction in power consumption from 37% to 66% at 500MHz clock frequency compared to standard domino circuit.

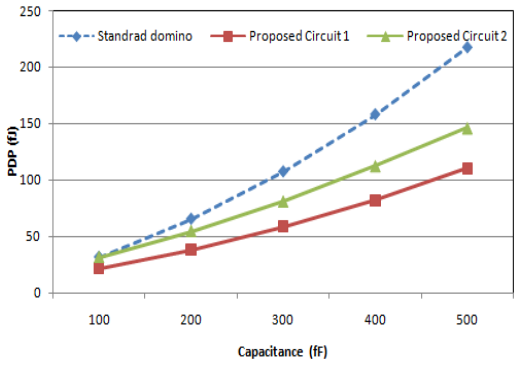


Figure 8. Power versus capacitance.

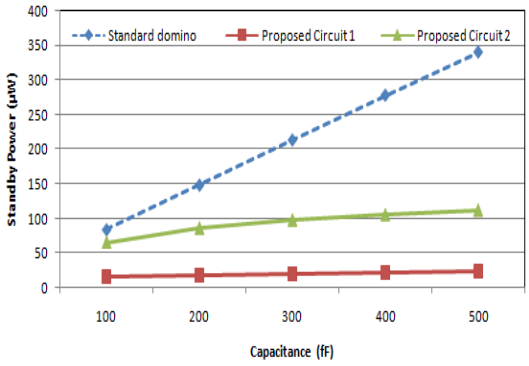


Figure 9.Stanby power versus capacitance.

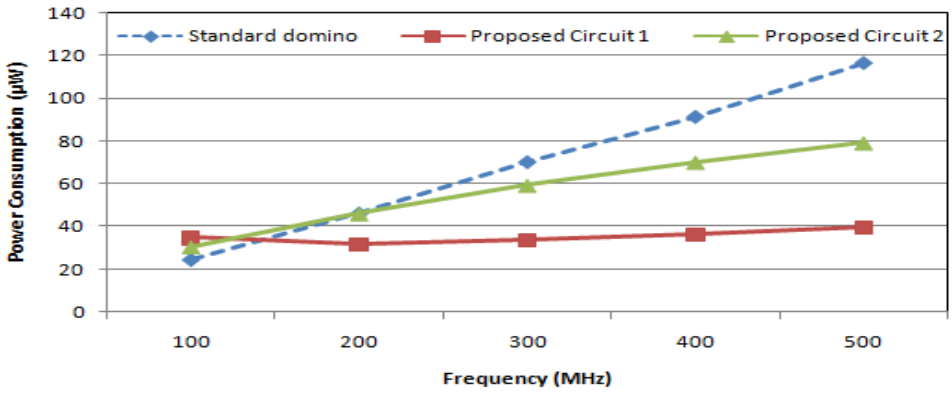


Figure 10. Power consumption versus frequency.

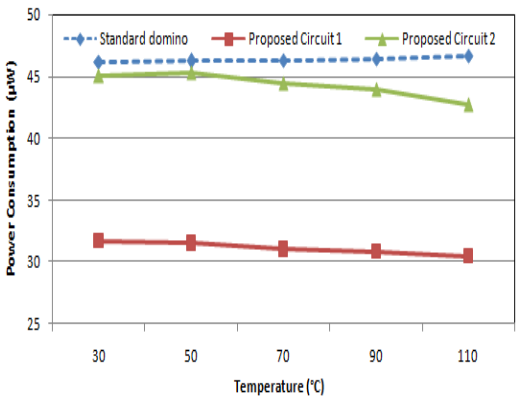


Figure 11. Power versus temperature.

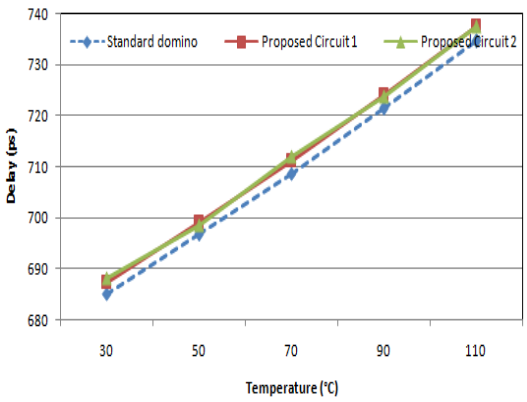


Figure 12. Delay versus temperature.

In Fig.11 illustrates the relationship between the power consumption and temperature for proposed circuits and standard domino circuit, clock frequency and load capacitance were set 200MHz and 100fF.It shows proposed circuits has much lower power consumption and its value decrease as temperature increase. For higher temperature our proposed circuits perform better than standard domino circuit. Similarly, in Fig.12 delay versus temperature is represented. Delay is linear function of temperature. Our proposed circuits suffer little delay penalty as compared to standard domino circuit. Fig.13 shows PDP versus temperature, our proposed circuits have minimum PDP.

Fig.14 illustrated the power consumption for proposed circuits and standard domino circuits for different supply voltages. The clock frequency is set 200MHz and load capacitance is set 100Ff.Our proposed circuits shows better power saving at higher power supply.

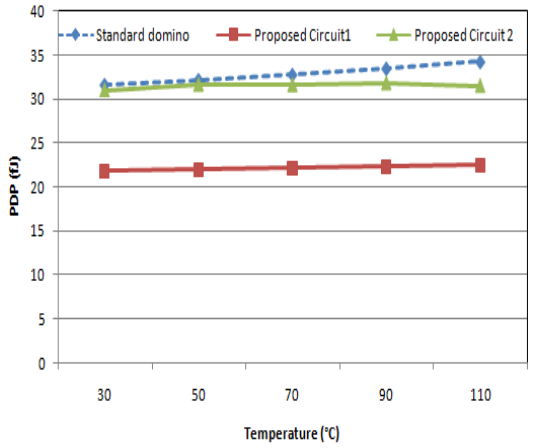


Figure 13. PDP versus temperature.

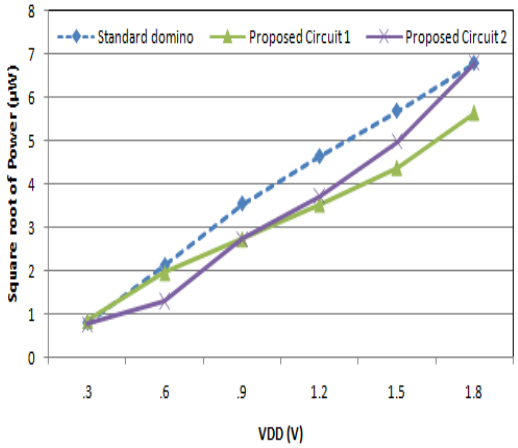


Figure 14. Power versus power supply.

A ripple carry adder is also simulated by using proposed circuit1 and proposed circuit2 is shown in Fig. 15 and Fig.16. Comparison of power consumption of proposed circuits adder and standard domino circuit adder for different loading condition, clock frequency is set 200 MHz is summarized in Table 2.Indicating about 8% to 40% power saving at higher load capacitance.

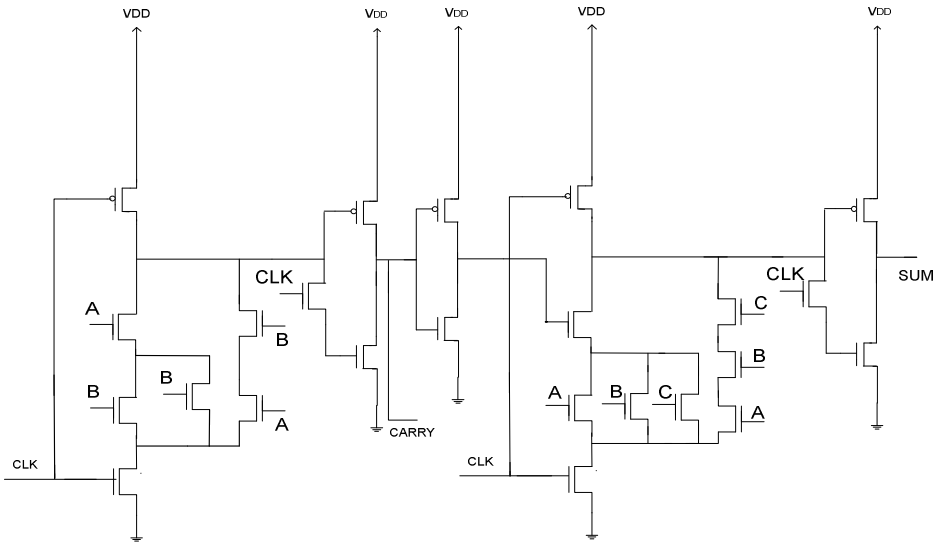


Figure 15. 1 bit ripple carry adder using proposed circuit1.

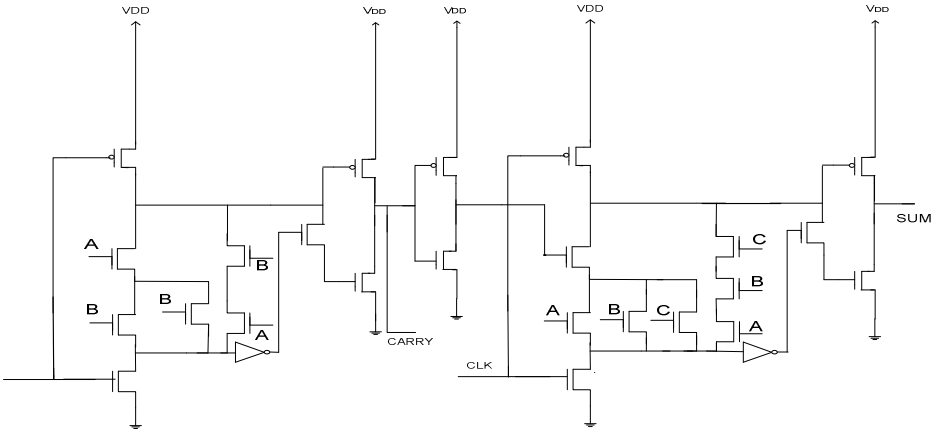


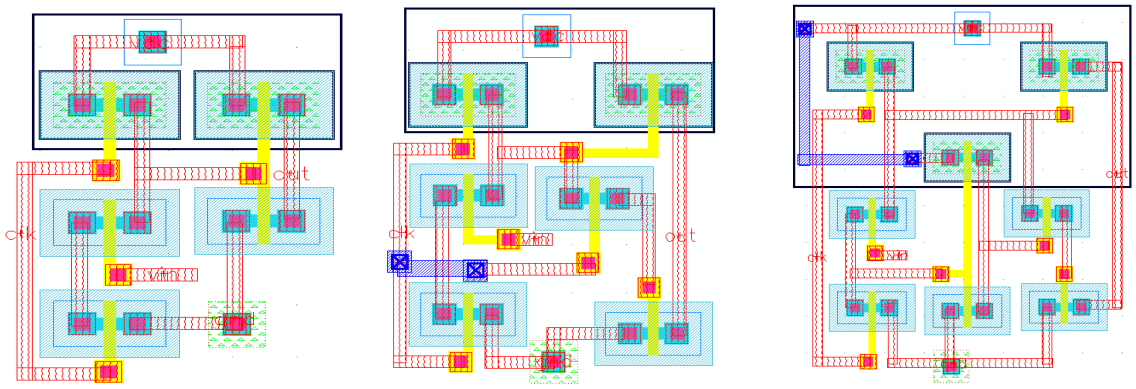
Figure 16. 1 bit ripple carry adder using proposed circuit 2.

Table 2. Comparison of Power Consumption of Proposed Adder Circuits and Standard Domino Adder Circuit (Clock Frequency=200 MHz and Load Capacitance=100Ff)

Load capacitance(fF)	Standard adder	Proposed circuit 1 adder	Proposed circuit 2 adder
100	69.73	60.664	65.95
200	105.82	76.34	100.35
300	140.32	92.46	132.98
400	175.29	108.40	171.15
500	208.94	123.78	191.44

The layout of the standard domino circuit, proposed circuit 1 and proposed circuit 2 are implemented using 0.18um standard CMOS technology, have been plotted in Fig.17. Simulation

results of Pre-layout and post –layout, clock frequency and load capacitance were set 200MHz and 100fF are summarized in Table.3. From the table, post layout simulations the delay, power consumption and power delay product reduces as compared to pre-layout simulation. Our proposed circuits require larger area as compared to standard domino circuit is given in Table 4.



(a) (b) (c)

Figure 17. Layout (a) standard domino circuit. (b) Proposed circuit 1. (c) Proposed circuit 2.

Table 3. Pre- and Post-Layout Simulations Results for Power, Delay and PDP of Standard Domino Circuit, Proposed Circuit 1 and Proposed Circuit 2 for 0.18µm Standard CMOS Technology.

	Type	Delay(ps)	Power(µW)	PDP(fJ)
Pre-Layout	Standard domino circuit	683.43	46.04	31.46
	Proposed circuit 1	684.96	31.86	21.82
	Proposed circuit 2	685.51	45.45	31.15
Post-Layout	Standard domino circuit	672	43.51	29.23
	Proposed circuit 1	673.2	29.36	19.76
	Proposed circuit 2	694.76	42.1	29.24

Table 4. Area Comparison of Proposed Circuits and Standard Domino Circuit.

Area(μm^2)	Standard domino circuit	Proposed circuit 1	Proposed circuit 2
	37.02	89.6832	47.11

5. CONCLUSIONS

In this paper, two new buffer circuits are proposed. The main idea of using these circuits to minimize the redundant switching at the output node and saves power as compared to standard domino circuit. These circuits solve the problem of propagation of precharge pulse during precharge phase in standard domino circuit. Proposed circuits and standard domino circuit are simulated in 0.18µm using HSPICE. Performance of the proposed structure is compared with standard domino circuit for different clock frequency, loading condition and temperature.

Carry adder circuit is also simulated by using proposed circuit techniques and standard domino circuit. Result shows maximum power saving for different loading condition as compared to standard domino circuit. Layout of proposed circuits and standard domino circuit are implemented using standard CMOS technology. Post-layout simulation reduces the delay, power consumption and power delay product as compared to pre-layout simulation.

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