MODELING OF BUILT-IN POTENTIAL VARIATIONS OF CYLINDRICAL SURROUNDING GATE (CSG) MOSFETS

Santosh Kumar Gupta[1] and S. Baishya[2]

Department of Electronics & Communication Engineering, National Institute of Technology Silchar, Assam – 788 010, INDIA
[1]santoshty@gmail.com, [2]sb@nits.ac.in

ABSTRACT

Due to aggressive scaling of MOSFETs the parasitic fringing field plays a major role in deciding its characteristics. These fringing fields are now not negligible and should be taken into account for deriving the MOSFET models. Due to this fringing field effect there are some charges induced in the source/drain extension regions which will change the potential barrier at the source-channel from its theoretical nominal values. In this paper an attempt has been made to model variation of built-in potential variation for a cylindrical surrounding gate MOSFET. The model has been verified to be working in good agreement with the variations of gate length and channel radius.

KEYWORDS

Barrier lowering, cylindrical surround gate (CSG) MOSFET, fringing field, short channel effects (SCEs)

1. INTRODUCTION

Silicon technology is spreading widely and supports the IT revolution which is now reshaping society. The technology keeps improving year on year as the chip sizes are going on decreasing with the simultaneous increase in the transistor speeds. However as we reduce the dimensions, short channel effects (SCEs) cause several problems such as threshold voltage lowering, increased substrate bias effect etc. [1]-[3]. To continue the scaling of Si MOSFETs in the nanometre regime, innovative device structures have been proposed. One such structure is the surrounding cylindrical gate MOSFET where the gate has control over the channel from all the directions reducing the short channel effects and improving the sub-threshold characteristics. However this structure is also not free from the SCEs.

But due to scaling of the MOSFETs the fringing field effects are becoming comparable to the gate capacitance and can't be neglected anymore [4], [5]. Due to these fringing fields originating from the sidewalls of the gates are capable of changing the source-channel and drain-channel barriers as well. This change in the barrier heights may contribute to significant change in the electrical characteristics of a highly scaled MOS transistor [6]-[15].

In this paper, an attempt has been made to account for these fringing fields and see the effect on the barrier lowering. The results obtained are encouraging but not as accurate. Even though, this gives an insight about the changes in the barrier potentials due to these fringing fields. In the section II of the paper the preliminary concept of the variation of the built in potential variation has been discussed and a general equation has been derived. In section III, we have derived

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expressions accounting for the fringing field effect of cylindrical surrounding gate MOSFETs. In section IV, the model has been verified to be working almost in agreement with the 3D-TCAD simulations of cylindrical surrounding gate MOSFETs. Variations in the potential barrier due to the change in the radius and length of the channel have been taken into account for the verification of the model developed.

2. MODEL DEVELOPMENT

In this section first we discuss about the general discussion about the built in potential variation. In the latter part of the section the mathematical formulations for the case of cylindrical surrounding gate MOSFET has been derived.

2.1. Variation of Built-in potential at Source-Channel junction

In weak inversion we assume that potential at the source/drain-channel boundary (junction) is fixed at built in potential (ϕ_b) and is given by (for a p-type body, with doping concentration equal to N_A).

$$\phi_b = \frac{E_g}{2} + \frac{kT}{q}\log\left(\frac{N_A}{n_i}\right) \tag{1}$$

Here it is assumed that Fermi energy level in the source is aligned with the source conduction band. E_g is the silicon energy band gap, n_i is the intrinsic carrier concentration, q is the unit charge, T is the absolute temperature in degree Kelvin, and k is the Boltzmann constant. For the doping levels of the order $10^{20} cm^{-3}$, the value of the ϕ_b may be different than predicted by the Fermi-Dirac (FD) statistics. The above equation (1) also assumes that there is no spatial variation of carrier density inside the source/drain. But, the actual case may be very different than the above and ϕ_b may depend upon many other parameters like gate length, film thickness and biasing voltages etc.

For accurate prediction of the source/drain - channel boundary potential, we need to solve the 1-D Poisson's equation inside the source,

$$\frac{d^2\phi}{dy^2} = \frac{q}{\varepsilon_{Si}}(n_s - N_D) \tag{2}$$

Where, n_s is the electron concentration in the source, ε_{Si} is the permittivity of silicon and N_D is the source doping density.

In equilibrium for an undoped body (channel), the electron concentration in the source assuming the Maxwell-Boltzmann (MB) statistics can be given by

$$n_s = n_i e^{\frac{\phi}{V_T}} \tag{3}$$

From (2) and (3) we get

$$\frac{d^2\phi}{dy^2} = \frac{q}{\varepsilon_{Si}}(n_s - N_D) = \frac{q}{\varepsilon_{Si}}\left(n_i e^{\frac{\phi}{V_T}} - N_D\right) = \frac{qN_D}{\varepsilon_{Si}}\left(\frac{n_i}{N_D} e^{\frac{\phi}{V_T}} - 1\right) \tag{4}$$

When $\phi = V_{bi}$, $n_s = N_D$ and we have $N_D = n_i e^{\frac{V_{bi}}{V_T}}$. Substituting this into (4), we get

$$\frac{d^2\phi}{dy^2}=\frac{qN_D}{\varepsilon_{Si}}\left(\frac{n_i}{n_i e^{\frac{V_{bi}}{V_T}}}e^{\frac{\phi}{V_T}}-1\right)=\frac{qN_D}{\varepsilon_{Si}}\left(e^{\frac{(\phi-V_{bi})}{V_T}}-1\right) \tag{5}$$

Integrating the above equation with the boundary conditions $\frac{d\phi}{dy}=0$ at $y=-y_s$ and $\phi=V_{bi}$

Multiplying both sides by $2d\phi/dy$ we get-

$$2\frac{d\phi}{dy}\frac{d^2\phi}{dy^2}=2\frac{d\phi}{dy}\frac{qN_D}{\varepsilon_{Si}}\left(e^{\frac{(\phi-V_{bi})}{V_T}}-1\right)\Rightarrow\left(\frac{d\phi}{dy}\right)^2=\frac{2qN_D}{\varepsilon_{Si}}\left[V_T e^{\frac{(\phi-V_{bi})}{V_T}}-\phi\right]+C_0 \tag{6}$$

Where C_0 is a constant of integration and may be found by using the boundary conditions as follows –

Using $\frac{d\phi}{dy}=0$ at we $y=-y_s$ get-

$$C_0=\frac{2qN_D\left[V_{bi}-V_T\right]}{\varepsilon_{Si}} \tag{7}$$

Substituting above value of C_0 in to (6) we get

$$\left(\frac{d\phi}{dy}\right)^2=\frac{2qN_D}{\varepsilon_{Si}}\left[V_T e^{\frac{(\phi-V_{bi})}{V_T}}-\phi\right]+\frac{2qN_D\left[V_{bi}-V_T\right]}{\varepsilon_{Si}} \tag{8}$$

Above equation can be simplified to

$$\left(\frac{d\phi}{dy}\right)^2=\frac{2qN_D V_T}{\varepsilon_{Si}}\left[e^{\frac{(\phi-V_{bi})}{V_T}}-1-\frac{(\phi-V_{bi})}{V_T}\right] \tag{9}$$

Above equation do not has an analytical solution and needs to be numerically evaluated to get an accurate value of the source-channel boundary potential. Simpler, yet reasonably accurate value of the boundary potential can be obtained using the depletion approximation. Using the boundary potential in terms of the electric field at the boundary may be given by [2]

$$\phi_b=V_{bi}-\frac{\varepsilon_{Si}E_b^2}{2qN_D} \tag{10}$$

Where E_b is the electric field at the source-channel boundary.

2.2. Evaluation of E_b for cylindrical surrounding gate (CSG) MOSFETs

A cylindrical surrounding gate (CSG) MOSFET is symmetrical about its axis so we can use only 2D Poisson's equation for the calculation of the potential variations. For a CSG MOSFET, in the weak inversion the channel potential can be calculated using the following 2-D Poisson's equation-

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial(\phi(r,z))}{\partial r}\right)+\frac{\partial^2(\phi(r,z))}{\partial z^2}=\frac{qN_A}{\varepsilon_{Si}} \tag{11}$$

Where r – is the distance in the radial direction of the cylindrical channel region, $\phi(r,z)$ is the potential variations in the channel region, N_A is the doping concentration in the channel region.

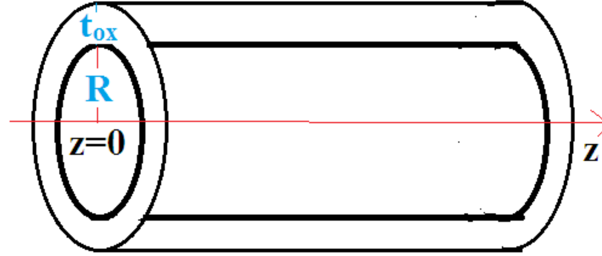


Figure 1 Cylindrical surrounding gate MOSFET (here only channel region with gate oxide is shown for simplicity)

Assume parabolic potential profile in the vertical direction of the channel.

$$\phi(r,z)=c_1(z)+c_2(z)r+c_3(z)r^2 \tag{12}$$

Where $c_1(z)$, $c_2(z)$ and $c_3(z)$ are the constants and can be determined the following boundary conditions-

1. Surface potential is a function of z only at the Si/SiO_2 interface.

$$\phi(R,z)=\phi_S(z) \tag{13}$$

2. The electric field in the center of the silicon pillar is zero due to symmetry along z-axis.

$$\left.\frac{\partial\phi(r,z)}{\partial r}\right|_{r=0}=0 \tag{14}$$

3. The electric field at $r=R$ (Si/SiO_2 interface) is continuous.

$$\left.\frac{\partial\phi(r,z)}{\partial r}\right|_{r=R}=\frac{C_f}{\varepsilon_{Si}}\left[V_{GS}-\phi_s(z)-V_{FB}\right] \tag{15}$$

Where t_{ox} - gate oxide thickness, $\phi_s(z)$ - surface potential, V_{GS} - gate to source voltage, V_{FB} - flat band voltage, $C_f=\varepsilon_{ox}\Big/R\ln\left(1+\frac{t_{ox}}{R}\right)$ is the gate capacitance per unit area,

4. The potential at the source end is

$$\phi(0,0)=\phi_s(0)=\phi_b \tag{16}$$

5. The potential at the drain end is

$$\phi(L,0)=\phi_s(L)=\phi_b+V_{DS} \tag{17}$$

Where V_{DS} is the drain to source voltage.

Solving (13) – (15) constants $c_1(z)$, $c_2(z)$ and $c_3(z)$ are found as:-

$$\begin{aligned} c_1(z)&=\phi_S(z)\left[1+\frac{C_f R}{2\varepsilon_{Si}}\right]-\frac{C_f R}{2\varepsilon_{Si}}\left[V_{GS}-V_{FB}\right] \\ c_2(z)&=0 \\ c_3(z)&=\phi_S(z)\left[1+\frac{C_f R}{2\varepsilon_{Si}}\right]-\frac{C_f R}{2\varepsilon_{Si}}\left[V_{GS}-V_{FB}\right] \end{aligned} \tag{18}$$

Substituting above values in (12) the 2-D potential in the channel is given by-

$$\phi(r,z)=\phi_S(z)\left[1+\frac{C_f R}{2\varepsilon_{Si}}\right]-\frac{C_f R}{2\varepsilon_{Si}}\left[V_{GS}-V_{FB}\right]+\frac{C_f}{2R\varepsilon_{Si}}\left[V_{GS}-\phi_s(z)-V_{FB}\right]r^2 \tag{19}$$

Substituting this value of $\phi(r,z)$ in to (1), we get-

$$\frac{d^2\phi_S(z)}{dz^2}-\lambda^2\phi_S(z)=\beta \tag{20}$$

Where $\lambda^2=2C_f/\varepsilon_{Si}R$ and $\beta=qN_A/\varepsilon_{Si}-\lambda^2\left(V_{GS}-V_{FB}\right)$.

Solution of the above equation is of the form as given by

$$\phi_S(z)=Ae^{\lambda z}+Be^{-\lambda z}-\frac{\beta}{\lambda^2} \tag{21}$$

Where A and B are constants, found using (16) and (17), as given by

$$\begin{aligned} A&=\frac{\left(\phi_b+\dfrac{\beta}{\lambda^2}\right)\left(1-e^{-\lambda L}\right)+V_{DS}}{2\sinh(\lambda L)} \\ B&=\frac{\left(\phi_b+\dfrac{\beta}{\lambda^2}\right)\left(e^{\lambda L}-1\right)-V_{DS}}{2\sinh(\lambda L)} \end{aligned} \tag{22}$$

Now, the electric field at the barrier (source-channel boundary), i.e. at $z=0$, can be given by the potential of the channel at the boundary, i.e.,

$$E_b = -\left.\frac{d\phi(r,z)}{dz}\right|_{z=0} = \left\{\left[-\left(1+\frac{C_f R}{2\varepsilon_{Si}}\right)+\frac{C_f r^2}{2R\varepsilon_{Si}}\right]\frac{d\phi_S(z)}{dz}\right\}_{z=0} \quad (23)$$

Or $E_b = -\left.\frac{d\phi(r,z)}{dz}\right|_{z=0} = \left\{\left[-\left(1+\frac{C_f R}{2\varepsilon_{Si}}\right)+\frac{C_f r^2}{2R\varepsilon_{Si}}\right]\left(Ae^{\lambda z}-Be^{-\lambda z}\right)\lambda\right\}_{z=0}$

$$E_b = (A-B)\lambda\left(\frac{C_f r^2}{2R\varepsilon_{Si}}-1-\frac{C_f R}{2\varepsilon_{Si}}\right) \quad (24)$$

And at the surface, i.e., $r = R$, the electric field will be

$$E_b = -(A-B)\lambda = (B-A)\lambda \quad (25)$$

Now, substituting the above value of the electric field at the boundary in to (10), we get

$$\phi_b = V_{bi} - \frac{\varepsilon_{Si}\left(A^2+B^2-2AB\right)\lambda^2}{2qN_D} \quad (26)$$

Substituting the values of A and B from (22) into (26), we get

$$u^2\varepsilon_{Si}\lambda^2(m-n)^2 + u\left\{4\varepsilon_{Si}\lambda^2(m-n)V_{DS}+2qN_Dd^2\right\}+4\varepsilon_{Si}\lambda^2V_{DS}^2-2qN_Dd^2\left(V_{bi}+\frac{\beta}{\lambda^2}\right)=0 \quad (27)$$

where $\left(\phi_b+\frac{\beta}{\lambda^2}\right)=u \Rightarrow \phi_b = u-\frac{\beta}{\lambda^2}$, $\left(1-e^{-\lambda L}\right)=m$, $\left(e^{\lambda L}-1\right)=n$, $d=2\sinh(\lambda L)$

Solution of the above quadratic equation is given by

$$u = \frac{-\delta \pm \sqrt{\delta^2-4\alpha\gamma}}{2\alpha} \quad (28)$$

Where

$\alpha = \varepsilon_{Si}\lambda^2(m-n)^2$, $\delta = 4\varepsilon_{Si}\lambda^2(m-n)V_{DS}+2qN_Dd^2$, and $\gamma = 4\varepsilon_{Si}\lambda^2V_{DS}^2-2qN_Dd^2\left(V_{bi}+\frac{\beta}{\lambda^2}\right)$.

The above equation can be re-written as

$$u = \frac{-\delta \pm \sqrt{\delta^2-4\alpha\gamma}}{2\alpha} \Rightarrow \phi_b+\frac{\beta}{\lambda^2} = \frac{-\delta \pm \sqrt{\delta^2-4\alpha\gamma}}{2\alpha} \quad (29)$$

From which the value of ϕ_b can be given by

$$\phi_b = \frac{-\delta \pm \sqrt{\delta^2 - 4\alpha\gamma}}{2\alpha} - \frac{\beta}{\lambda^2} \qquad (30)$$

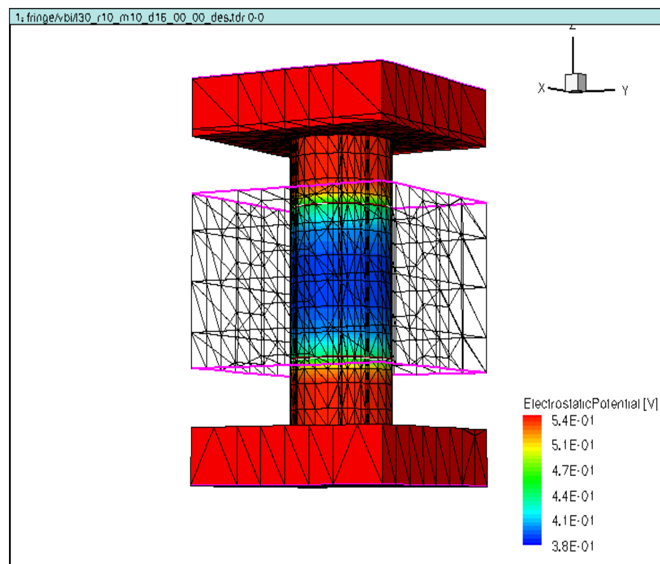
3. RESULTS AND DISCUSSIONS

For the validation of the above model a typical cylindrical surrounding gate (CSG) MOSFET was simulated using the Sentaurus TCAD tool from the Synopsys as shown in Fig. 2. The CSG MOSFET parameters used for the simulation and validation of the model developed are shown in the Table 1. The structures have been generated using the structure editor and the device simulations have been carried using the Sentaurus device tool of Sentaurus TCAD [16]. The potential has been extracted using the Tecplot SV and the current voltage characteristics using the Inspect tool.

The CSG MOSFETs modelled are of n-type with lightly doped channel (Boron, $1\times10^{16}\,cm^{-3}$) and heavily doped source/drain regions (Arsenic, $1\times10^{20}\,cm^{-3}$). The gate is made of Gold (workfunction, $4.8\,eV$) of gate height 10 nm. Source/Drain extension regions used are 10 nm long as shown in Figure 2. The blank entries in Table I show the varying parameter for given structures viz. ***'Gate length'*** and ***'Channel radius'***.

Table I Device parameters used for the device simulation

Structure	Channel radius	Gate length	Oxide thickness	Source/drain extension	Gate height	Channel doping
Gate length	10	---	1	10	10	1.0e+16
Channel radius	---	30	1	10	10	1.0e+16



. Figure 2 3D cross sectional view of the simulated CSG MOSFET with meshing at V_{GS}=0.0 V and V_{DS}=0.0 V

Figure 2 shows the 3D cross sectional view of a simulated CSG MOSFET along with the meshing at zero biasing voltages. The variation of the electrostatic potential through the channel can also be seen in this Fig. The device is simulated using the doping dependence, high field saturation and electric field normal to the direction of current flow dependent mobility models. SRH recombination has been used for all the simulations. The quantum mechanical effects have not been considered for the simulations since the device sizes considered are large enough to ignore this.

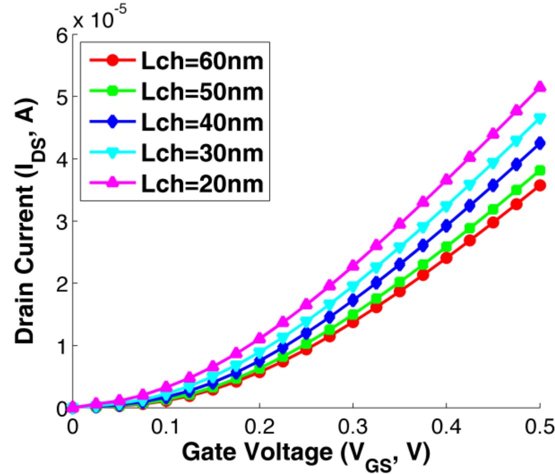


Figure 3 ON state current for different gate lengths of CSG MOSFET at V_{DS}=0.5 V

The current voltage characteristics for CSG MOSFETs with different gate lengths and a channel radius of 10 nm are shown in the Fig. 3. It can be observed that the current increases as the gate length decreases for the same operating voltages. This is due to the reason that the potential barrier at source/channel junction is lowered at smaller gate lengths which in turn increases the drain current. This is due to the fringing field controlling the channel charge and hence effective charge controlled by the gate is reduced which in turn reduces the threshold voltage of the device. Therefore, for the same applied gate voltage the drain current is increased.

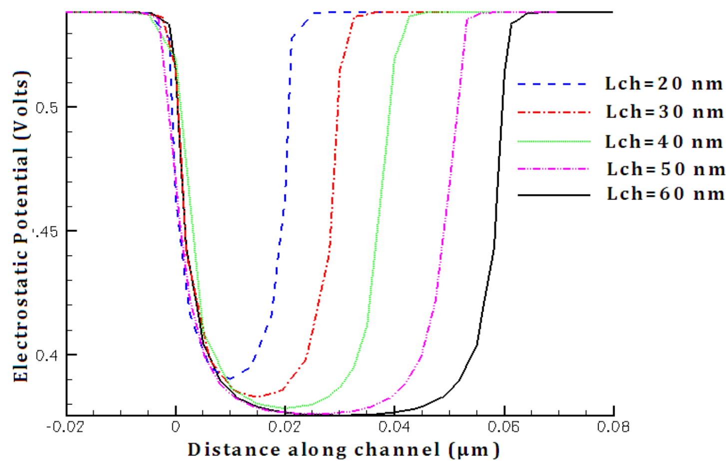


Figure 4 Electrostatic potential variation along the channel for different gate lengths of CSG MOSFET (V_{GS}=0.0 V and V_{DS}=0.0 V). Channel regions start at $0.0\,\mu m$.

In Fig. 4 the simulated electrostatic potential along the gate at Si-SiO_2 interface are shown. It can be observed that the potential at z=0 is not constant for different channel lengths. This variation in the barrier potential is due to the fringing field effects emerging from the sidewalls of the gates.

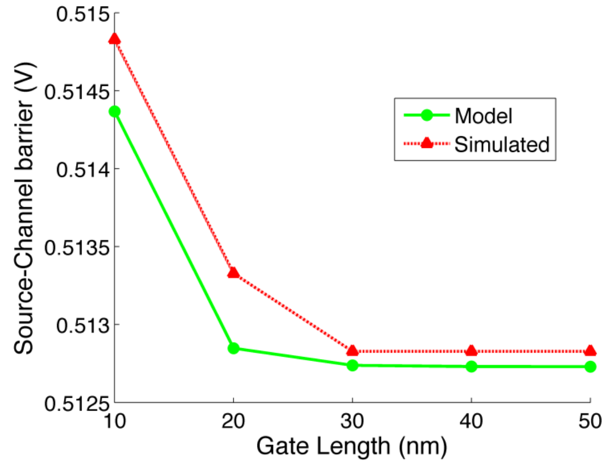


Figure 5 Variation of source-channel barrier potential with gate length (V_{GS}=0.0 V and V_{DS}=0.0 V)

Figure 5 compares the results obtained from 3D device simulations of CSG MOSFETs with different gate lengths (as shown in Table I) to that predicted using the derived model. As can be observed that model developed is in good agreement with the simulated results. In Fig. 6 the variation of the barrier potential of CSG MOSFETs using 3D device simulations for different channel radius has been shown. Again it can be observed that the potential barrier at z=0 (source-channel barrier) are not constant rather they vary. In Fig. 7 the variation of the potential has been compared for different channel radius. It also agrees with the values predicted by the model.

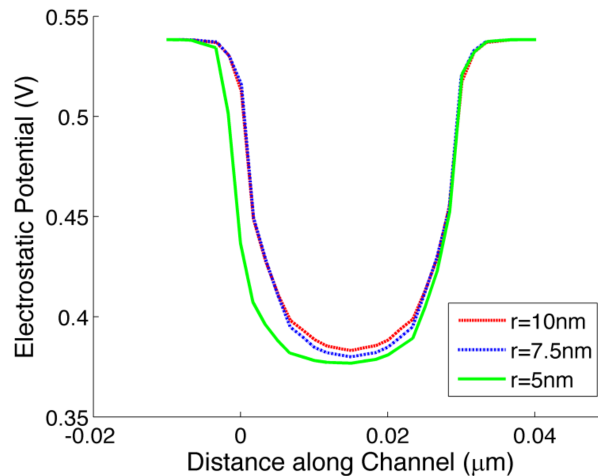


Figure 6 Variation of electrostatic potential along the channel at Si/SiO_2 interface with different channel radius (V_{GS}=0.0 V and V_{DS}=0.0 V). Channel regions start at $0.0\,\mu m$.

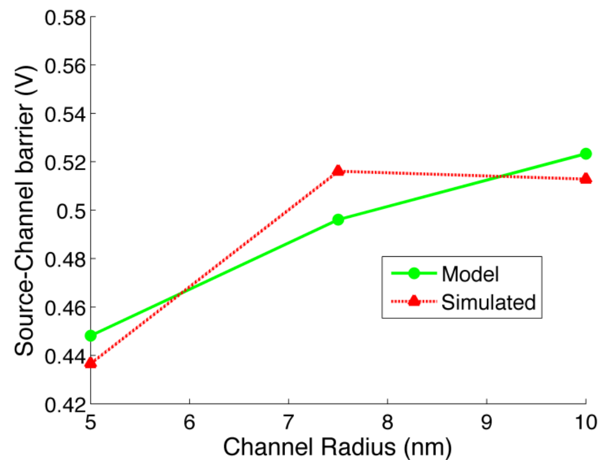


Figure 7 Variation of electrostatic potential along the channel for different channel radius and gate length of 30 nm (V_{GS}=0.0 V and V_{DS}=0.0 V)

3. CONCLUSION

A physical model for source/drain-channel barrier lowering has been derived. The model has been tested for the different physical parameters of a CSG MOSFET like gate length and channel radius and has been found to be working. It can be observed that after certain gate length or channel radius there is no change in the source-channel barrier potential. It is due to the reason that the fringing field effects become negligible for larger dimension. However, there is still scope for improvement in the above derived model by incorporating more non-ideal effects present in small dimensional devices.

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Authors

Santosh Kumar Gupta received his B.E. in Electronics and Communication Engineering from Govind Ballabh Pant Engineering College, Pauri (Garhwal), Uttarakhand, India in 2000, M. Tech. degree in Communication Engineering (Electrical Engineering Deptt.) from Indian Institute of Technology, Mumbai, India in 2002. From 2002 to 2005, he worked as lecturer in the department of Electronics and Communication Engineering at Kumaon Engineering College (Now, Bipin Chandra Tripathi Kumaon Engineering College), Dwarahat, Uttarakhand, India. In September 2005, he joined the department of Electronics and Communication Engineering of National Institute of Technology (NIT), Silchar, India as lecturer and is currently there at the post of Assistant Professor. He is also working towards his PhD degree at NIT Silchar, India. His research area includes modeling and simulation of novel device structures on SOI MOSFETs. He is a member of IEEE.

Dr. Srimanta Baishya received his B.E. in Electrical Engineering from Assam Engineering College, M.Tech. in Electrical Engineering from IIT Kanpur, and Ph.D. in Electronics and Telecommunication Engineering from Jadavpur University. Dr. Baishya is currently working as a Professor, ECE Department, NIT Silchar, India. He has more than 25 publications in National / International Journals / Conferences. His present research interest includes MOS Transistor Modeling, Semiconductor Devices Physics, VLSI circuits, and MEMS. He is a member of IEEE.