HIGH FIN WIDTH MOSFET USING GAA STRUCTURE

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ABSTRACT

This paper describes the design and optimization of gate-all-around (GAA) MOSFETs structures. The optimum value of Fin width and Fin height are investigated for superior subthreshold behavior. Also the performance of Fin shaped GAA with gate oxide HfO2 are simulated and compared with conventional gate oxide SiO2 for the same structure. As a result, it was observed that the GAA with high K dielectric gate oxide has more possibility to optimize the Fin width with improved performance. All the simulations are performed on 3-D TCAD device simulator.

KEYWORDS

Gate all around(GAA),TG FinFET, High K gate oxide, Silicon-On-Insulator(SOI), Work function, Short channel effect, DIBL, Subthreshold Slope,3-D Sentaurus TCAD tool.

1. INTRODUCTION

Non planar three-dimensional devices with multiple gates [1] are more promising candidate for high current drive capability and better short-channel characteristics. The use of ultra-thin body (UTB) and Multiple Gate SOI structures allows the fabrication of fully-depleted devices that offer not only extremely good control of SCEs but also a very good behavior with respect to drain induced barrier-height lowering (DIBL), threshold voltage roll-off, and off-state leakage [1]. DG FinFET[2] is one of the example of non planner multigate MOSFET with superior performance than planner DG MOSFET. The Fin width (W_{fin}) and height h_{fin} characterises the FinFET(Fig1) structure. The channel width ($W = W_{fin} + 2h_{fin}$) of FinFET [3] can be increased without increasing the actual layout area, simultaneously improving the on state current. The current drive of multiple-gate SOI MOSFETs [4-5] is essentially proportional to the total gate width. Considering a pitch P for the fins, the current in a multigate device[1] is given by:

$$I_D = I_{D_0} \frac{\theta \mu_{top} W_{fin} + 2\mu_{side}\, h_{fin}}{\mu_{top} P}$$

Where,

θ

I_{D0} : Current in single gate

W_{fin} : Width of each individual Fin

h_{fin} : Height of each individual Fin

θ : 1, for Triple gate FinFET

Additionally, lots of efforts are being made to enhance the FinFET structure. The important aspects of different FinFET structures are better subthreshold swing (SS) and drain-induced barrier lowing (DIBL) which is possible with optimum ratio of gate length to Fin width[6-7]. It has been widely known that the Fin width in DG MOSFETs should be less than 0.7 times the gate length for proper suppression of short-channel effects [8]. Therefore, the dimension in devices is determined by the fin width mainly and not by the gate length.

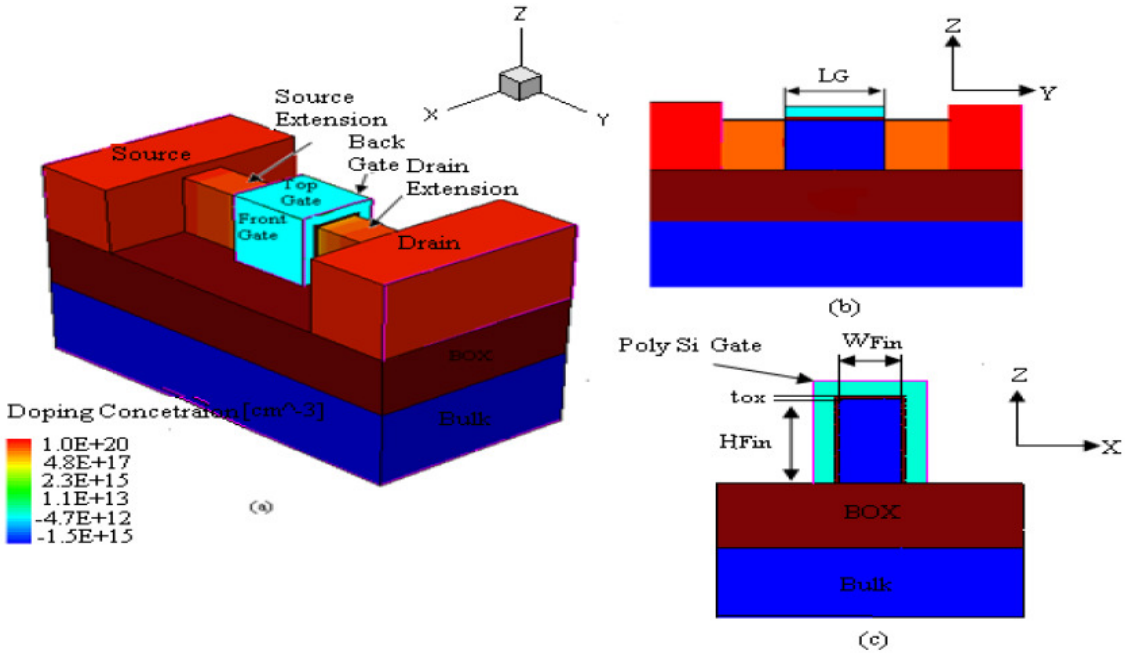

Fig. 1 (a) 3D Structure of TG FinFET (b) Front view of FinFET, (c) Fin structure near Gate

This paper deals with improvement of subthreshold performance of gate-all -around(GAA) structure over tri-gate FinFET structure. The gate-all-around (GAA) MOSFETs[9] in which the gate oxide and the gate electrodes wrap around the channel region exhibit excellent transconductance and short-channel behavior because of the presence of two additional inversion channels (at the top and the bottom of the silicon fin) and the occurrence of strong volume inversion[10]. Using GAA MOSFETs can lead to the increase of the ratio of the Fin width to the gate length. If the parameters of GAA MOSFETs are optimized, the short-channel effects are adequately suppressed even if the fin width is larger than the gate length.

Three-dimensional (3-D) simulations were performed for TG and GAA MOSFETs with various fin widths, Fin heights, and gate-oxide thicknesses to explore short-channel effects. Further, the GAA structure is simulated with high K-dielectric material (HfO2) and it shows better characteristic performance. Further, conventional GAA structure using SiO2 as dielectric material, is compared with GAA structure using high K-dielectric material (HfO2).

2. DEVICE STRUCTURE

Fig.2 shows the bird's eye views GAA MOSFETs used in device simulations. Device simulations were performed by the 3-D TCAD simulator [11-12]. SOI substrate was used in both TG FinFET and GAA MOSFETs having n-type channels and the same physical parameters as follows. Basically, the tri-gate FinFET designed is of 32nm channel length with source/drain doping is 1E20 cm^{-3}(n type). Metal is used as gate contact material and the work function of metal is kept 4.62eV. Silicon dioxide is as gate oxide material. Gate oxide thickness is kept 1.1nm. The channel doping is 1E16(p type) with V_{DD}=1.0V. The FinFET is designed with, 10nm Fin width and 60nm Fin height while GAA is designed with different Fin width between 10nm to 30 nm and Fin height between 20nm to 60nm. For first section of results the gate oxide is material used SiO2 and secondly it is designed with HfO2.

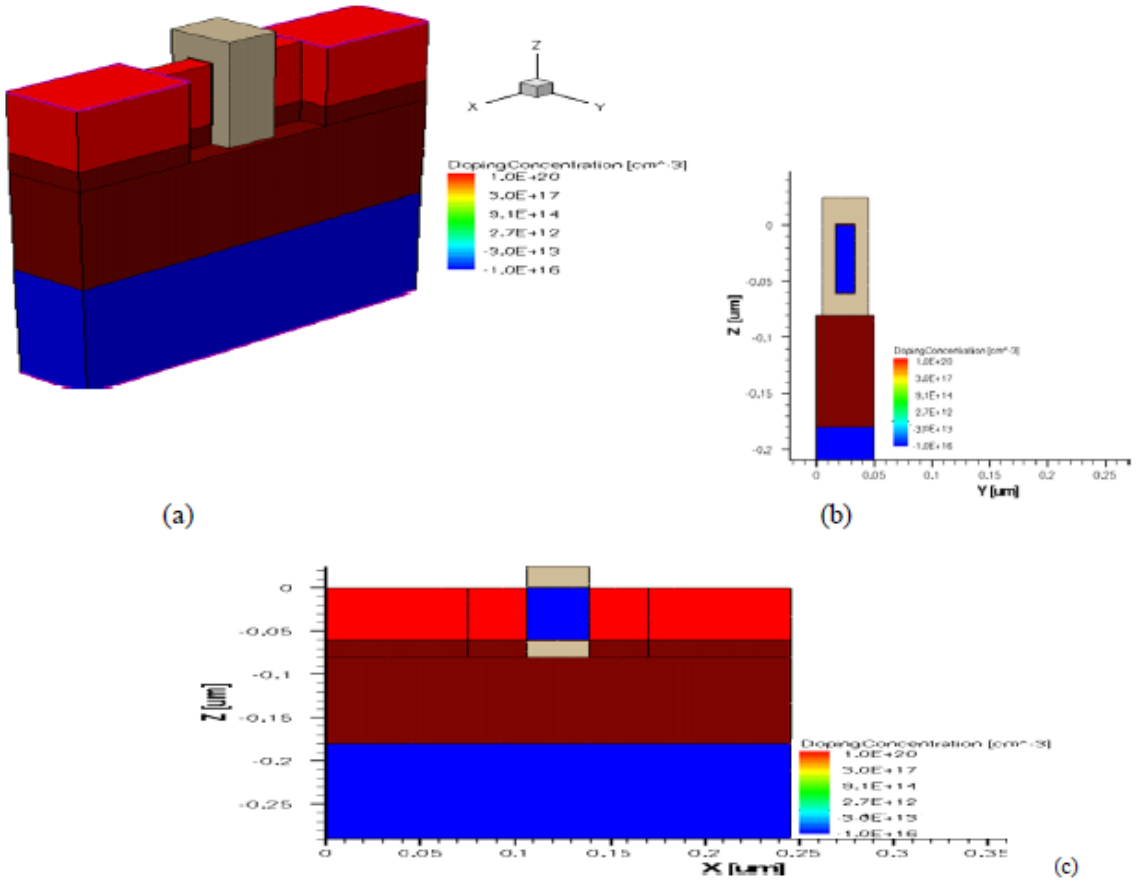

Fig. 2 (a) 3-d structure of GAA MOSFET (b) Y-cut of 3-d GAA structure (c) X-cut of 3-d GAA structure

3. SIMULATION AND RESULTS

For the conventional Bulk FinFET with low channel doping (1E16) Subthreshold slope of 91.78 mV/decade while for SOI FinFET Subthreshold slope of 68.57 mV/decade. Therefore we can

improve subthreshold performance with the use of SOI technology. We can also improve the performance with the increase in channel doping (1E18) for which the subthreshold slope is 79.18 mV/decade. But for low channel doping SOI FinFET is preferred because of its better on current drive(I_{ON}) and lower delay characteristics. Further we can improve the ON/OFF characteristics with the optimum design of GAA structure.

3.1. Effects of W_{fin} and h_{fin} variation on GAA structure

V_{th} plays important role in scaling of device with different technology. In GAA MOSFET structure, V_{th} is the function of W_{fin} and h_{fin}. Change in these parameters shows that for different value of it we cannot use same work function and channel doping. Therefore the need of V_{th} adjustment is required for each h_{fin} and W_{fin} variations. Effect of W_{fin} on V_{th} variation and sensitivity of I_{off} (i.e.effect of W_{fin} variation on I_{off}) is more with high value of h_{fin} as shown in Fig. 3.1, 3.2and 3.3. So, if we optimize the device for high value of W_{fin} then the lower value of h_{fin} is needed. But we require high value of h_{fin} to get higher on current due to high value of gate length. Also high h_{fin} leads to better area efficiency. Therefore, we need to optimize the W_{fin} and h_{fin} to get superior performance.

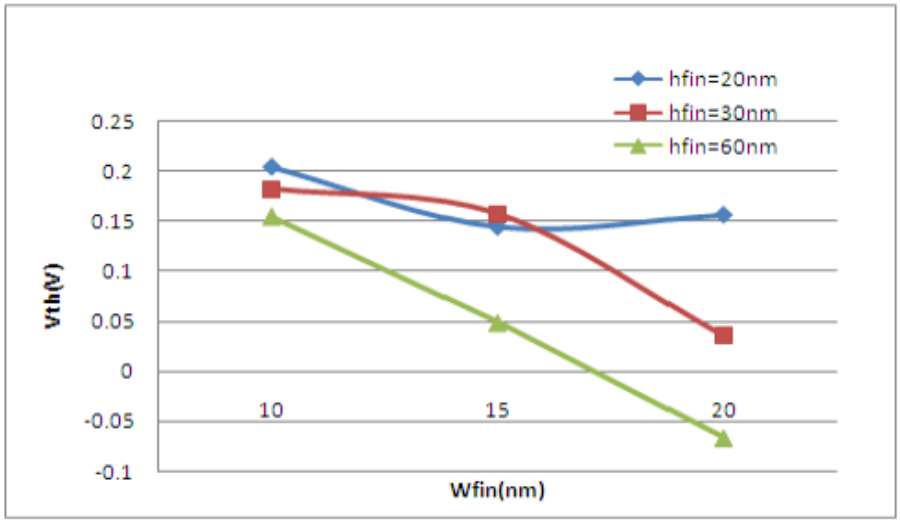

Fig. 3.1V_{th} variation with W_{fin} for different h_{fin}

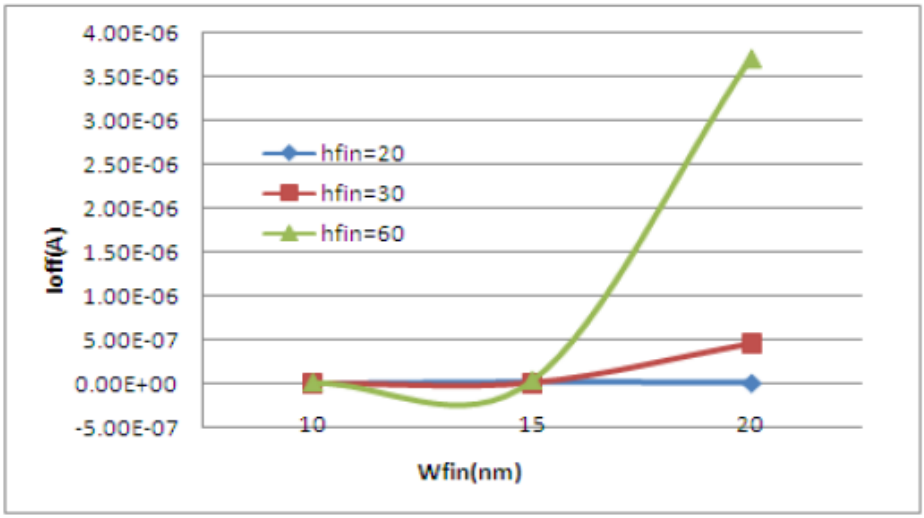

Fig. 3.2 I_{off} Vs W_{fin} for different h_{fin}

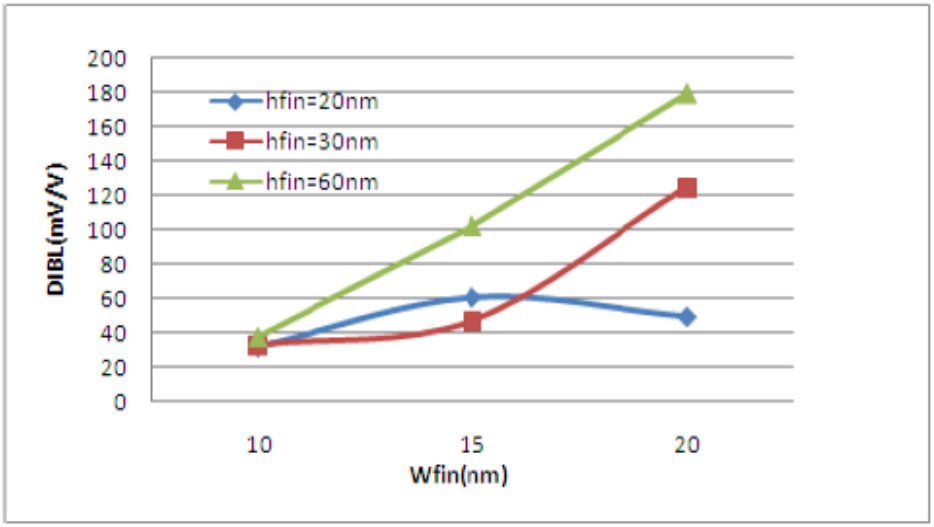

Fig. 3.3 DIBL Vs W_{fin} of GAA structure

Fig. 3.4, 3.5, 3.6 and 3.7 shows the different performance parameter of GAA structure with changing value of h_{fin}. The increase or decrease in performance parameters with increasing value of h_{fin}, is also dependent on W_{fin}. Like for W_{fin}=10nm we got best results at high value of h_{fin}=60nm. For W_{fin}=15 nm the best results are obtained at h_{fin}= 30nm. But if we further decrease h_{fin} upto 20nm performance degrades. Similarly, for h_{fin}=20nm the performance degrades at W_{fin}=20nm and the best results are obtained at h_{fin}=30nm which is higher than optimized Fin height(h_{fin}) of W_{fin}=15nm.

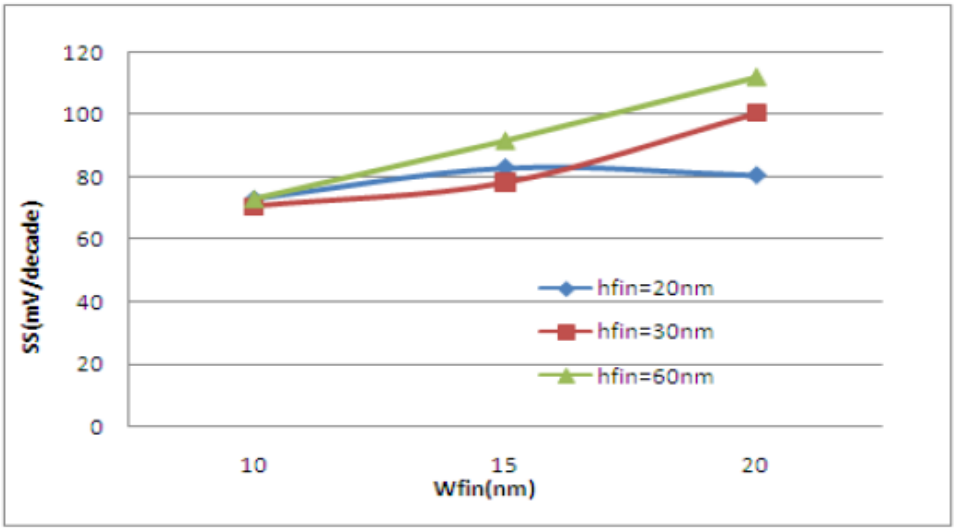

Fig. 3.4 SS Vs W_{fin} of GAA structure

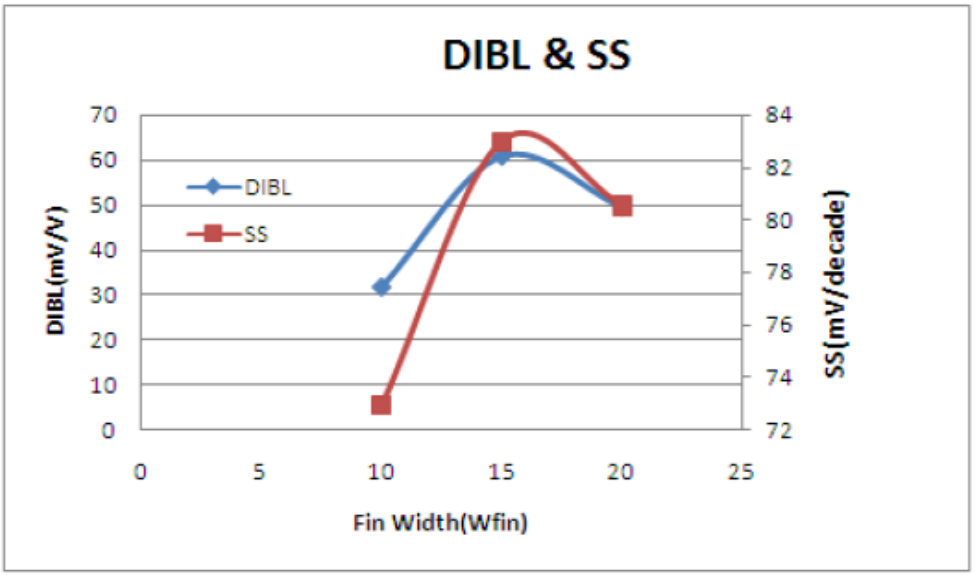

Fig. 3.5 DIBL and SS for different W_{fin}

Fig 3.6 indicate that Fin width increment degrades subthreshold performance if Fin height is taken 30 nm but in next Figure we have observe a significant advantage of having high fin width device its high value of Ion for VDD=1.5 V, almost twice current is obtained for W_{fin}=20 as compare to W_{fin} 10nm and 15nm. Even for VDD=1 V, the amount of Ion is significantly large. So the use of high fin width might solve the problem of low on current value associated with nano-electronics devices.

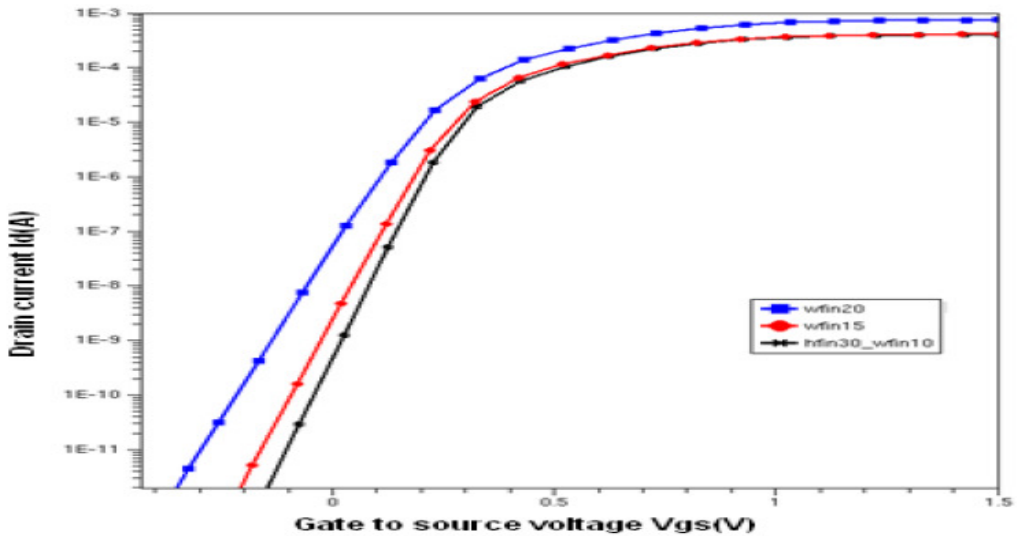

Fig. 3.6 Subthreshold characteristics of GAA structure for different fin width

From Fig. 3.7 ION Vs W_{fin} using GAA structure of h_{fin}=60nm & W_{fin}=10nm , h_{fin} 30nm& W_{fin}=20nm, the same range of Ion is obtained. So, use of higher fin width can be useful for maintaining proper driving current (on current) while using shallow junction (low h_{fin}) devices. Therefore, we can make junction more shallower (lower h_{fin}) for improvement in short channel performance. From Fig. 3.5, 3.7 of DIBL, SS and Ion, it is observed that the performance of "h_{fin}=60 nm & W_{fin}=10nm, h_{fin}=30nm & W_{fin}=15nm, h_{fin}=20nm & W_{fin}=20" GAA are comparable. In, Fig.3.5 DIBL and SS is shown for h_{fin}= 20nm and variable W_{fin} which indicates that performance does not always degrades with increase in W_{fin}. For further improvement in high fin width devices (if high W_{fin} is used) the proper matching of short channel characteristics are needed to maintain performances in desirable range. So, here we discuss the scope of high fin width GAA using high K gate materials.

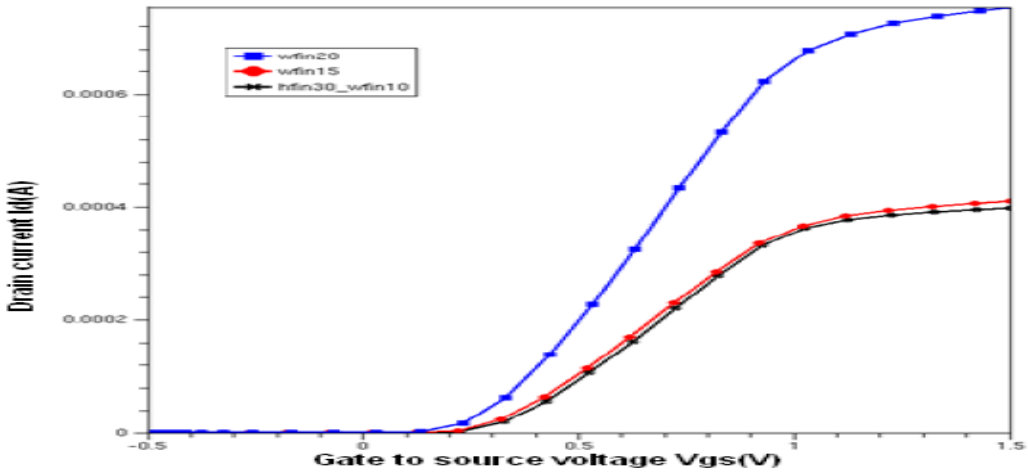

Fig.3.7 Transfer characteristics of GAA structure for different W_{fin}

3.2. Effect of high K dielectric material on GAA structure

The use of high K materials [13-14] as gate oxide results in to the increase in on state current while off state current, subthreshold slope and DIBL decreases, enhancing the FinFET performance due to the fringing electric field[15]. The magnitude of the fringing electric field depends upon the dielectric constant of the medium in which it is getting leaked. The fringing field increases with the use of high k dielectric material for gate oxide. The different high K dielectric material such as Silicon Oxide (SiO2), Silicon Nitride (Si3N4) and Hafnium Oxide (HfO2) having dielectric constants of 3.5, 7.5 and 25 respectively, can be utilized at different places in different MOS devices for performance improvement.

Similarly, in case of GAA structure high K material(HfO2) gate oxide can be used to get improved subthreshold performance with high W_{fin} . It is clear from the characteristics of Fig.3.8 that there is an increase in on state current of the device with the use of high K dielectric material. Simultaneously, the off-state leakage current of the GAA structure decreases with the use of high K dielectric materials as in Fig.3.9. The decrease in off state current is basically because of increase in the barrier potential faced by the carriers in case of high K dielectric materials. The increase in the Ion/Ioff ratio of the device which is very essential for low power operation of the device and the value of it can be controlled by proper design of W_{fin} .

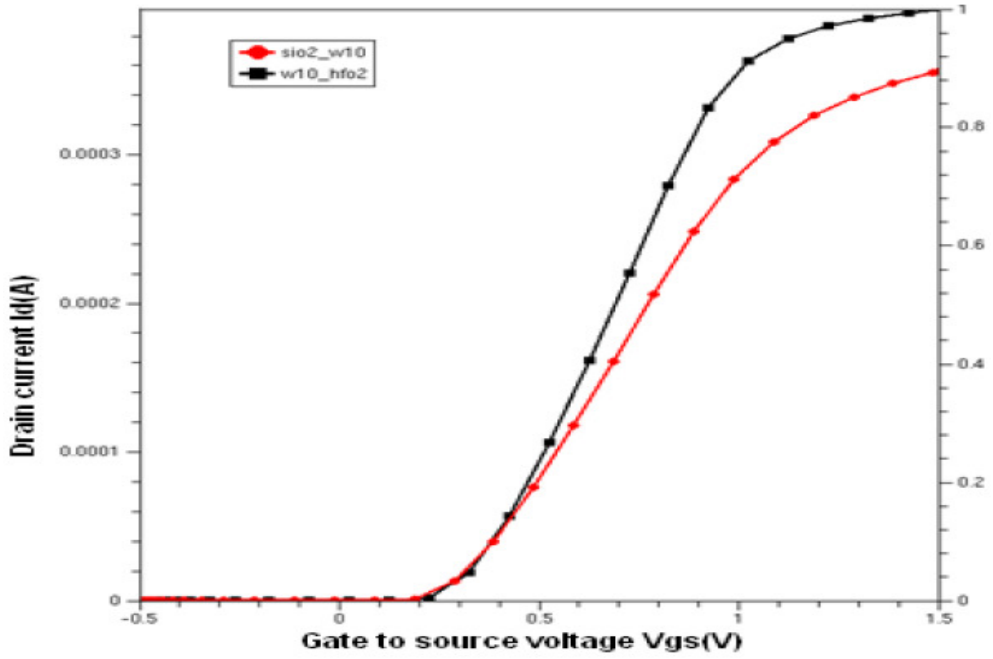

Fig. 3.8 Transfer characteristics of GAA structure with SiO2 and HfO2 gate oxide material for 10nm W_{fin}

The off state current is minimum in case of HfO2 with W_{fin} equal to 10nm but it has low value of on state current. The on state can be increased by increase in W_{fin} (20nm) as the Fig. 3.9 indicate compared to the GAA structure of same size with SiO2 oxide material.

Fig. 3.10, 3.11 shows the comparison between subthreshold characteristics of GAA structure with SiO2 and HfO2 as dielectric material for gate oxide and also gives the comparison among GAA structures with different value of W_{fin}. Both the graph indicate that GAA structure with HfO2 oxide material gives improved Ion/Ioff ratio with the improvement in subthreshold performance.

Here, the Fin shape is cubical in GAA structure but the similar behavior can be obtained with cylindrical Fin[10]. The future device scaling can be done with these GAA structures without compromise in their performances.

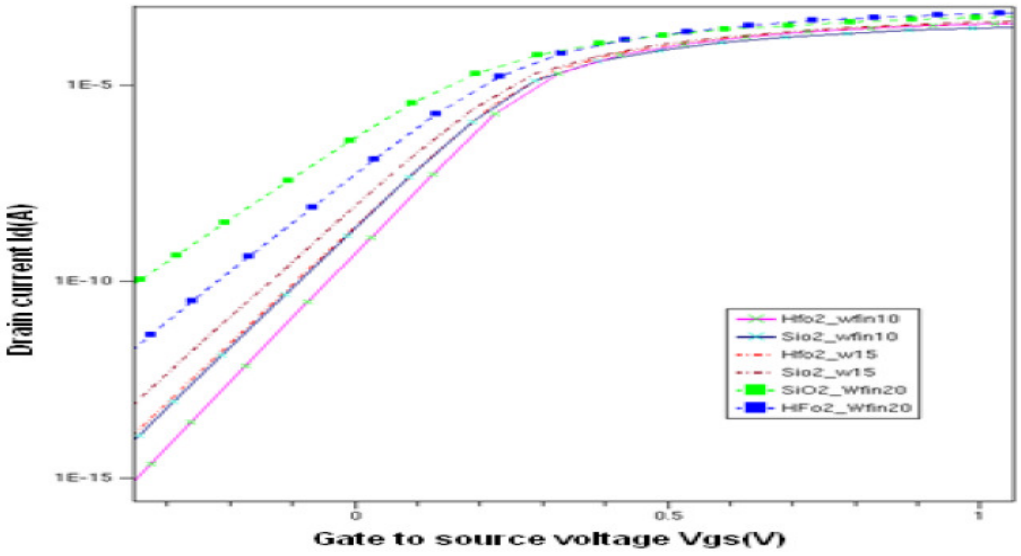

Fig. 3.9 Subthreshold characteristics of GAA with SiO2 and HfO2 gate oxide for different W_{fin}

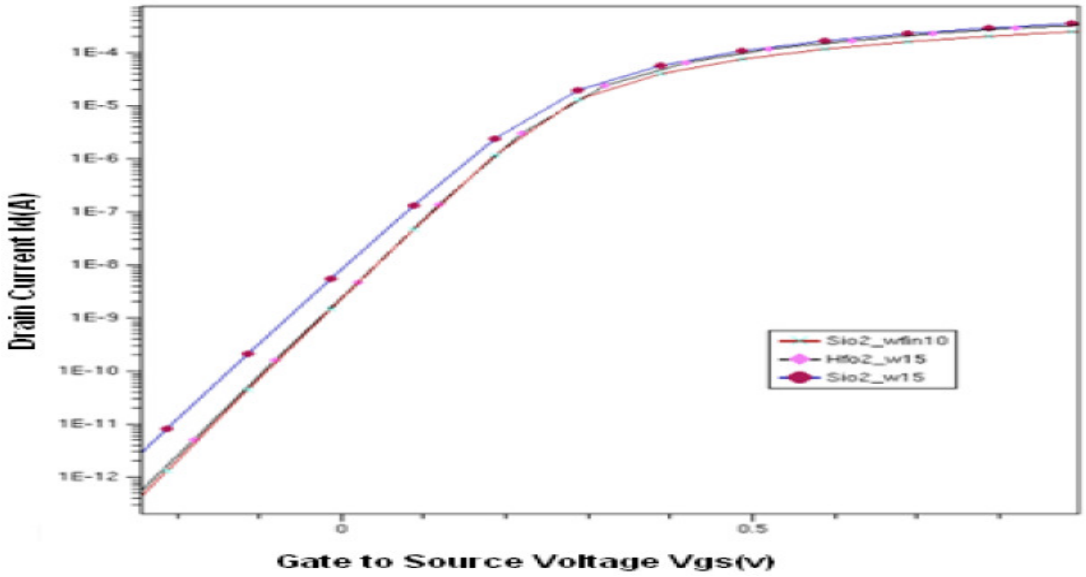

Fig. 3.10 Subthreshold characteristics of GAA with SiO2 and HfO2 gate oxide for 15nm W_{fin}

In in future GAA structures will give better replacement of p-n junction diode as driving device in phase-change memory cells (PCM) with more scalability[16].

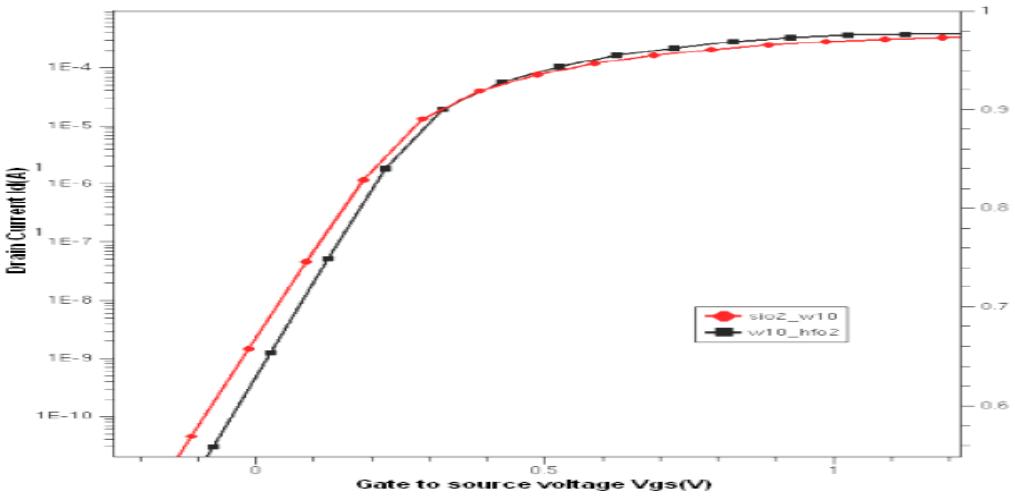

Fig. 3.11 Subthreshold characteristics of GAA with SiO2 and HfO2 gate oxide for 10nm W_{fin}

4. CONCLUSION

"If we required high Fin width MOSFET, FinFET is not a good option" but if we use GAA instead of FinFET more volume inversion is obtain and after a certain Fin height the performance of GAA increases while decreasing h_{fin}. This paper shows that for low value of h_{fin}, high performance GAA can be structured even for High Fin width. Therefore, the condition of low Fin width is no longer be a problem for GAA structure because of it' s superior performance with high Fin width. Further we extended our results to high-K Gate oxide materials to obtain more improvement in device performance. The graph of Fig.3.9,3.10&3.11 are showing that GAA with high K gate oxide materials has superior performance for the same Fin width. The GAA structure on Bulk can also be designed and its performance can be improved with high Fin width using high K dielectric gate oxide materials.

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