DESIGN & ANALYSIS OF A CHARGE RE-CYCLE BASED NOVEL LPHS ADIABATIC LOGIC CIRCUITS FOR LOW POWER APPLICATIONS

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ABSTRACT

This paper focuses on principles of adiabatic logic, its classification and comparison of various adiabatic logic designs. An attempt has been made in this paper to modify 2PASCL (Two Phase Adiabatic Static CMOS Logic) adiabatic logic circuit to minimize delay of the different 2PASCL circuit designs. This modifications in the circuits leads to improvement of Power Delay Product (PDP) which is one of the figure of merit to optimize the circuit with factors like power dissipation and delay of the circuit. This paper investigates the design approaches of low power adiabatic gates in terms of energy dissipation and uses of Simple PN diode instead of MOS diode which reduces the effect of Capacitances at high transition and power clock frequency. A computer simulation using SPECTRE from Cadence is carried out on different adiabatic circuits, such as Inverter, NAND, NOR, XOR and 2:1 MUX.

KEYWORDS

Adiabatic logic, Low-power, Two phase clocked, Energy recovery, Split-level, Diode based logic, Power Delay Product (PDP), LPHS (Low Power High Speed).

1. INTRODUCTION

The popularity of complementary MOS (CMOS) technology can be gauged from the fact that it has lower power consumption and high speed. However, the current trend towards ultra low-power has made researchers search for techniques to recycle energy from the circuits within. In conventional CMOS level-restoring logic, the switching event of circuits with rail-to-rail output voltage swing, causes an energy transfer from the power supply to the output node or from the output node to the ground. During a 0-to-V_{DD} transition of the output, the total output charge $Q = C_{load} V_{DD}$ is drawn from the power supply at a constant voltage. Thus, an energy of $E = C_L V_{DD}^2$ is drawn from the power supply during this transition. Charging the output node capacitance to the voltage level V_{DD} means that at the end of the transition, the amount of stored energy in the output node is $E = ½ C_L V_{DD}^2$. Thus, half of the injected energy from the power supply is dissipated in the PMOS network while only one half is delivered to the output node. During a subsequent VDD-to-0 transition of the output node, no charge is drawn from the power supply and the energy stored in the load capacitance is dissipated in the NMOS network.

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To reduce the dissipation, the circuit designer can minimize the switching events, decrease the node capacitance, reduce the voltage swing, or apply a combination of these methods. Yet in all these cases, the energy drawn from the power supply is used only once before being dissipated. To increase the energy efficiency of the logic circuits, other measures can be introduced for recycling the energy drawn from the power supply. A novel class of logic circuits called adiabatic logic [1],[2] offers the possibility of further reducing the energy dissipated during the switching events, and the possibility of recycling, or reusing, some of the energy drawn from the power supply. To accomplish this goal, the circuit topology and the operating principles have to be modified as per the need arises. The amount of energy recycling [3] achievable using adiabatic techniques is also determined by the process technology, switching speed, and the voltage swing.

In conventional CMOS logic we use constant voltage source to charge the load capacitance but in case of adiabatic logic switching circuits we use constant current source instead of constant voltage source. Figure 1. depicts clearly how this can be achieved with subsequent explanation.

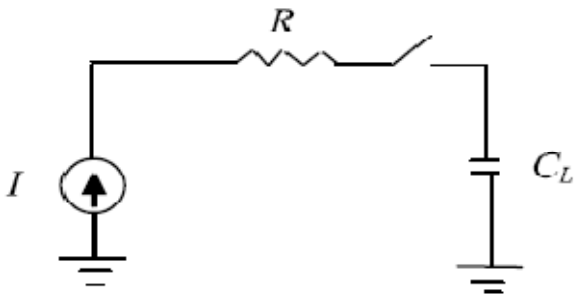

Figure 1. Constant current source used for adiabatic logic circuit

Dissipation in the switch = I^2*R
Energy during charging $E=(I^2*R)*T$

Also,

The voltage across the switch = I*R

$$Q=C_L*Vdd \ , I = (C_L *Vdd)/T \quad (1.1)$$

$$E=(I^2*R)*T = (R\ C_L) / T * C_L *Vdd^2 \quad (1.2)$$

Where,

E is the energy dissipated during charging time
Q is the charge transferred to the load
C_L is the value of the load capacitance
R is the on resistance of the PMOS switch
V_{DD} is the final value of the voltage at the load
T is the charging time

As explained above, the adiabatic switching power dissipation is asymptotically proportional to inverse of the charging time therefore, one can achieve very low energy dissipation [4] by slowing down the speed of operation and also the charge stored in the load capacitors can be recycled by using AC type power supply rather than DC.

Now, couple of observations can be made based on Equation (1.2) as follows:

i. The energy dissipated for adiabatic circuits is smaller if the charging time T is larger than $2RC_L$.

ii. Since, the dissipated energy is proportional to R thus reducing the on-resistance of the PMOS reduces the energy dissipation.

Figure 2 shows the model of an adiabatic logic showing an ideal switch in series with resistance and two complementary voltage supply clocks.

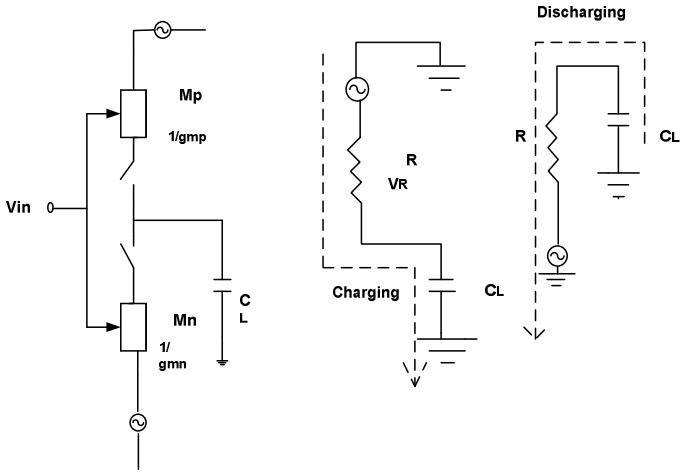

Figure 2. Model of adiabatic logic.

In this paper, we propose a low-power high speed (LPHS) adiabatic logic circuit to achieve an optimized result between power dissipation and delay which significantly reduces PDP upto 40% when compared with 2PASCL logic circuit,also power consumption is compared with that of a conventional CMOS circuit.

2. PREVIOUS WORK

Several adiabatic or Energy recovery logic architectures have been proposed over the years. They are based on the similar principle, but the structure and complexity, differ by, number of operation clock, Single- Dual rail style, Charging and discharging path etc.

2.1. Adiabatic logic structures are mainly of two types:

Partially adiabatic logic. They are classified as –

i) Efficient charge recovery logic (ECRL)
ii) Quasi Adiabatic Logic(QAL) [5]
iii) Positive feedback adiabatic logic (PFAL)
iv) NMOS energy recovery logic
v) True single phase adiabatic logic (TSAL)

Fully adiabatic logic. They are classified as-

i) Pass transistor adiabatic logic
ii) 2 Phase adiabatic Static CMOS logic (2PASCL)
iii) Split rail charge recovery logic (SCRL)

The previous work, using 2PASCL adiabatic logic shows that the power dissipation reduces by 60-70 % but delay of the circuit increases by as much as 30% as compared to the conventional CMOS circuit. These delays of the circuit occurred due to the MOS diode present in the discharging path of the circuit, because of the circuit operating at very high frequencies (10-100 MHz.) and at high frequency large number of capacitors are present which affects the time constant of the circuit. Time constant of the circuit increases due to charging and discharging of these capacitors at high power clock frequencies [6]. Therefore, delay of the circuit increases.

3. DESIGN APPROACHES AND PROPOSED CIRCUIT

Before we discuss more about the proposed and 2PASCL circuit, let us discuss a Partially adiabatic logic circuit for e.g QAL (Quasi Adiabatic Logic). Figure 3 shows the schematic of Quasi adiabatic logic circuit design which can be extended to 4 Inverter chain.

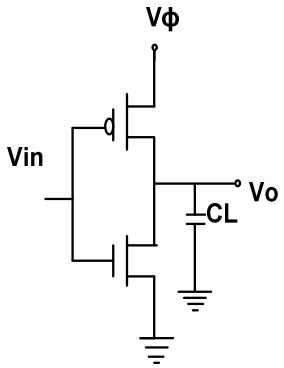

Figure 3. Quasi adiabatic logic.

In the Quasi Adiabatic Logic circuit, the circuit components are driven by a sinusoidal supply power clock instead of a constant supply (DC supply) as used in Conventional CMOS circuit. The QAL inverter shown above in the schematic uses a power clock of sinusoidal supply, therefore, the power dissipation of the circuit improves 60-70%.

Also the present paper discusses QAL using Pseudo nMOS, with MOS diode in charge recovery path. Due to these changes, we can save energy upto 15% as compared to conventional QAL. Both the schematic designs using Pseudo nMOS are shown below-

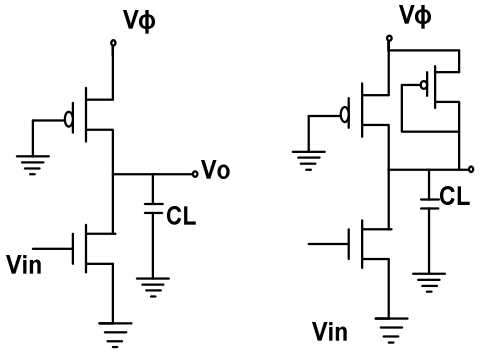

Figure 4. Proposed inverter (Pseudo nMOS implemented with Adiabatic Logic)

A novel method for reducing delay in the Proposed circuit, Low Power High Speed (LPHS) adiabatic circuit involves Simple PN diode instead of MOS diode uses in 2PASCL logic circuit. At high frequencies of 10-100MHz, capacitances acting on MOS diode in 2PASCL charges and discharges at every power clock cycle which would effectively increase the capacitances of circuit that leads to increases in the time constant resulting in increases of delay. For low power digital design [7] it has always been the focus point of the engineers to keep the load capacitance under control so that the delay is under check.

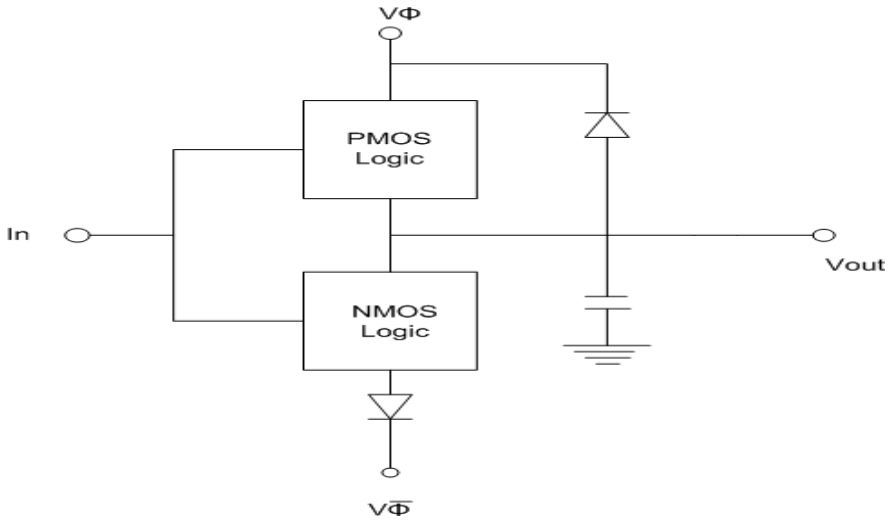

Figure 5. General diagram of LPHS Adiabatic logic circuit

LPHS Adiabatic logic is similar to CMOS circuits except few changes which make this logic much more energy efficient than CMOS with lesser delay as compared to 2PASCL as well as some other adiabatic logic circuits also [8]. The notable difference between LPHS and static CMOS logic gate is the two diodes, one from the output node to the power clock supply and another one is placed next to the nMOS logic to another power clock. Both PN diodes are used to re-cycle the charges from the output node, to improve discharging speed of internal signal nodes. This is especially advantageous for signal nodes with a long chain of switches.

The other difference is that split-level sinusoidal power clock supplies, Vø and Vø bar are used to replace the Vdd and the Vss. Substrate of pMOS is connected to Vø whereas for nMOS, it is connected to Vø bar. From the simulation, we found that split- level sinusoidal gives a lower energy dissipation compared to trapezoidal power clock supply even if we set the T_{rise} and T_{fall} of the trapezoidal waveforms to maximum values. By using two split-level sinusoidal waveforms where each peak-to-peak is 0.9 V, we can reduce the voltage difference, thus reducing the charging and discharging activities. Sinusoidal waveforms can also be generated with higher energy efficiency than trapezoidal waveforms.

The circuit operates in 2 phases –

I. Evaluation phase: When the output node is LOW and pMOS tree is turned ON, Load capacitor is charged through pMOS transistor resulting in the HIGH state at the output. When the output is LOW and nMOS is ON, no transition occurs. The same result is obtained when the output node is HIGH and pMOS is ON. Finally, when output node is HIGH and nMOS is ON, discharging via nMOS takes place resulting in the decrease of output voltage to Vt(threshold voltage) value where the logical state is “0” [9].

II. Hold phase: Now due to the diodes, the state of output when preliminary state is LOW remains unchanged. When the preliminary state of the output node is HIGH, it will change to Vt, the threshold voltage of the diode. At this point, discharging via diode D1 occurs.

From the operation of LPHS adiabatic logic as explained in evaluation and hold phase, less dynamic switching are observed as circuit nodes are not necessarily charging and discharging on every clock cycle which reduces the node switching activities significantly. This significantly lowers the switching activity lowering the energy dissipation.

4. CIRCUIT SIMULATION AND RESULTS

Schematic design and simulation results of INVERTER, NAND, NOR, XOR and 2:1 MUX are shown where comparison has been made for a non cascaded gate to those design using conventional CMOS and 2PASCL logic circuits with their power dissipation, delay and PDP. These results well conform for ultra low power applications using these logic gates [9].

The simulation in this paper were performed using a SPECTRE circuit simulator with a 0.18 um, 1.8 V standard CMOS process. The width and Length of the nMOS and pMOS logic gates were 0.6 um and 0.18 um respectively. A load capacitance of 0.01 pF was connected to the output node. The frequency of the power supply clock was set to a value same as the transition frequency. In this era of digital integrated circuits [10] maintaining the logic level with less degradation in the logic levels is the objective and the authors with the result have tried to prove this point.

4.1. Simulation Results

The logic function of these fundamental logic circuits which may form a basic cell for a design are based on LPHS Adiabatic logic and has been observed that the circuits conform to operate accordingly as shown in the corresponding figures. The results have been categorized and well tabulated. The time scale on the horizontal axis is in terms of nsecs. The other symbols have their usual meaning.

i. Schematic and Simulated waveforms of different logic circuits

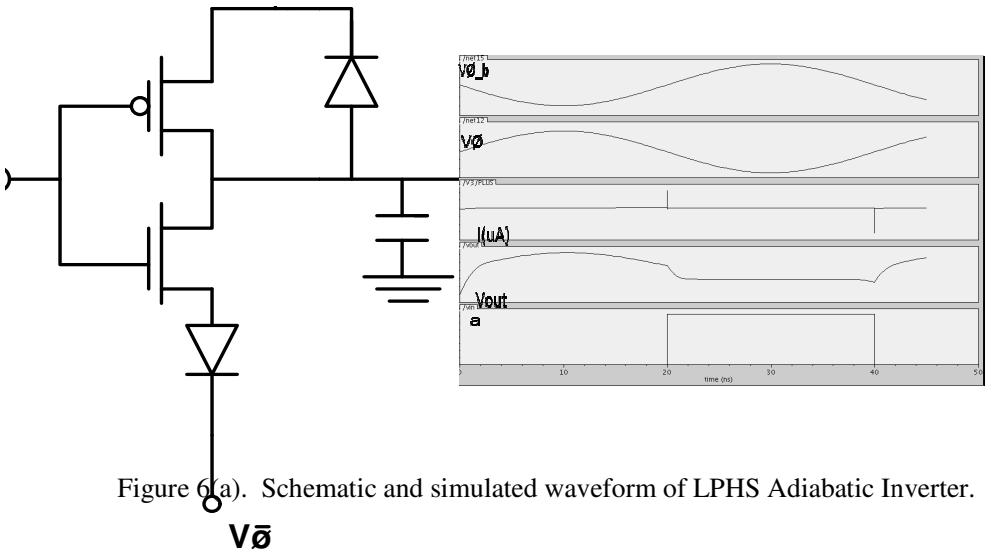

Figure 6(a). Schematic and simulated waveform of LPHS Adiabatic Inverter.

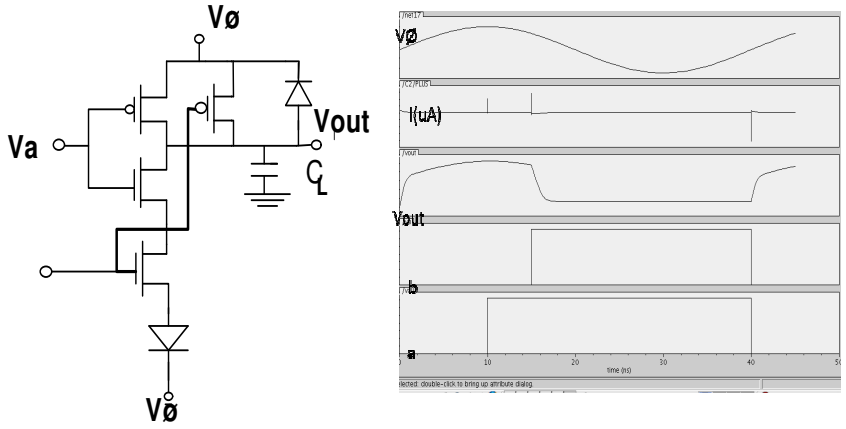

Figure 6(b). Schematic and simulated waveform of LPHS Adiabatic NAND Gate

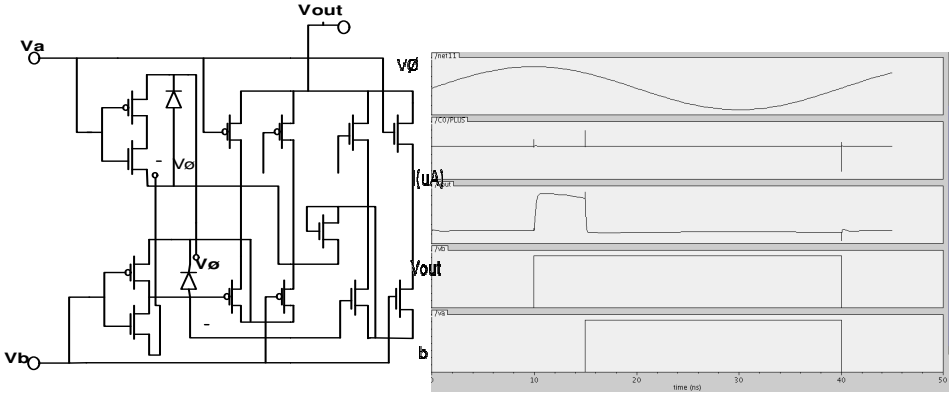

Figure 6(c). Schematic and simulated waveform of LPHS Adiabatic XOR Gate

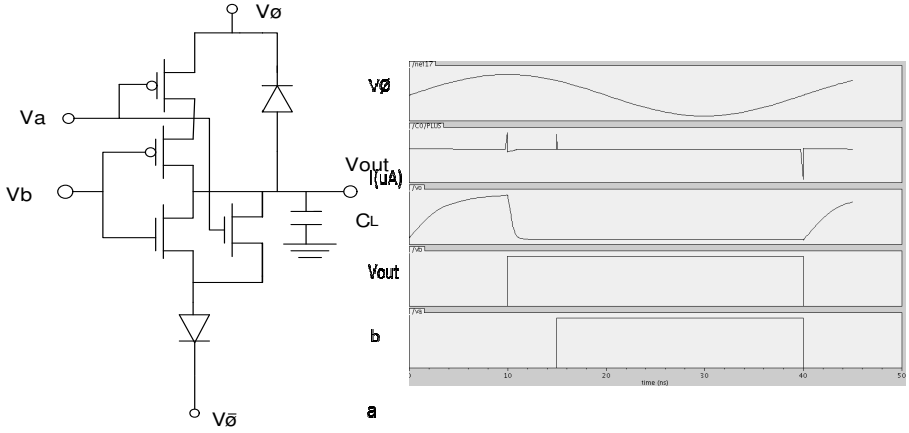

Figure 6(d). Schematic and simulated waveform of LPHS Adiabatic NOR Gate

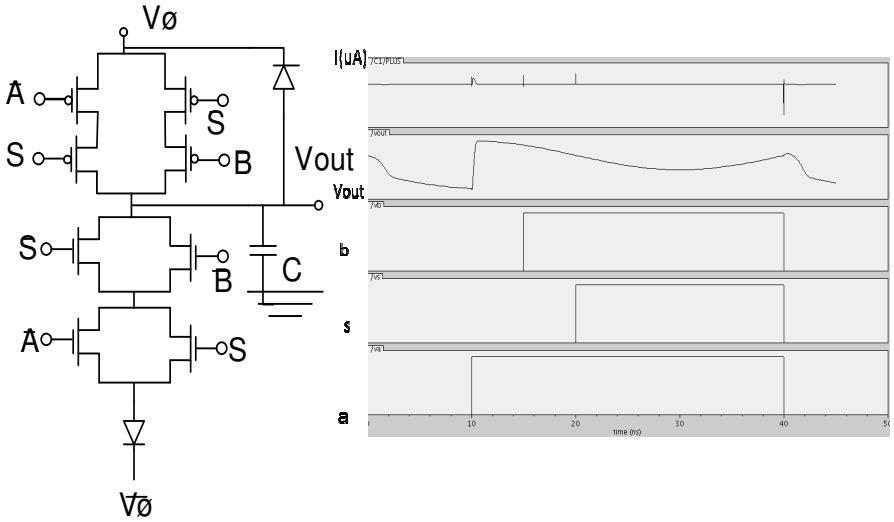

Figure 6(e).Schematic and simulated waveform of LPHS Adiabatic 2:1 MUX Gate

Figure 6(a) to 6(e) shows the simulated waveforms for the corresponding circuits of different gates where for each gate the current and output voltage has been shown for the applied inputs. The symbols shown in the figure have their usual meaning.

i. Tables.

Table 1 describes the power dissipation comparison of different logic gates for PD-CMOS,PD-2PASCL & PD-LPHS structures at 10fF capacitance and transition frequency of 25 MHz.

Table 1.PD comparison at C_L= 10fF and transition frequency = 25 MHz

Designed Logic	PD- CMOS	PD- 2PASCL	PD- LPHS
Inverter	7.1224 E-7	3.5568 E-7	3.5857 E-7
NAND	7.12 E-7	3.55 E-7	3.604 E-7
NOR	7.088 E-7	3.423 E-7	3.6631 E-7
XOR	7.782 E-7	1.88 E-7	2.135 E-7
2:1 MUX	7.244 E-7	2.412 E-7	2.614 E-7

Table 2 describes the delay comparison of different logic gates for PD-CMOS,PD-2PASCL & PD-LPHS structures at 10fF capacitance and transition frequency of 25 MHz. Note that 2:1 MUX has also been used in the comparison of different structures.

Table 2. Delay comparison C_L= 10fF and transition frequency =25 MHz

Designed Logic	CMOS Delay	2PASCL Delay	LPHS Delay
Inverter	5.7878 E-11	9.05454E11	3.302 E-11
NAND	3.254 E-11	4.665 E-11	1.928 E-11
NOR	1.4094 E-11	2.251 E-11	1.1587E-11
XOR	5.925 E-11	7.225 E-11	4.9842E-11
2:1 MUX	3.442 E-11	4.4572 E-9	3.29189E-9

Table 3 describes the power delay product of different logic gates for PD-CMOS,PD-2PASCL & PD-LPHS structures at 10fF capacitance and transition frequency of 25 MHz.

Table 3.PDP comparison at C_L= 10fF and transition frequency 25= MHz

Designed Logic	PDP -CMOS	PDP -2PASCL	PDP - LPHS
Inverter	4.122 E-17	3.22 E-17	1.84 E-17
NAND	2.2897 E-17	1.224 E-17	0.695 E-17
NOR	9.122 E-17	6.872 E-17	4.244 E-17
XOR	1.064 E-16	8.232 E-16	6.325 E-16
2:1 MUX	13.38 E-16	11.64 E-16	8.62-16

iii. Figures:PD comparison between CMOS, 2PASCL and LPHS Adiabatic logic

Figures 7 to Figure 10 shows the power dissipation comparison of CMOS, LPHS & 2PASCL structures at different output load capacitances which have been plotted for different logic gates.

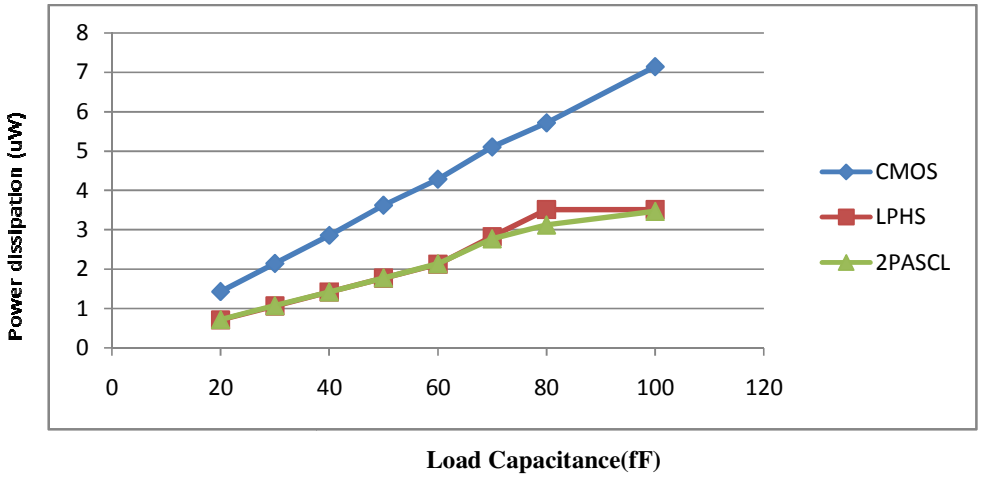

Figure 7. PD Versus C_L Comparison(Inverter)

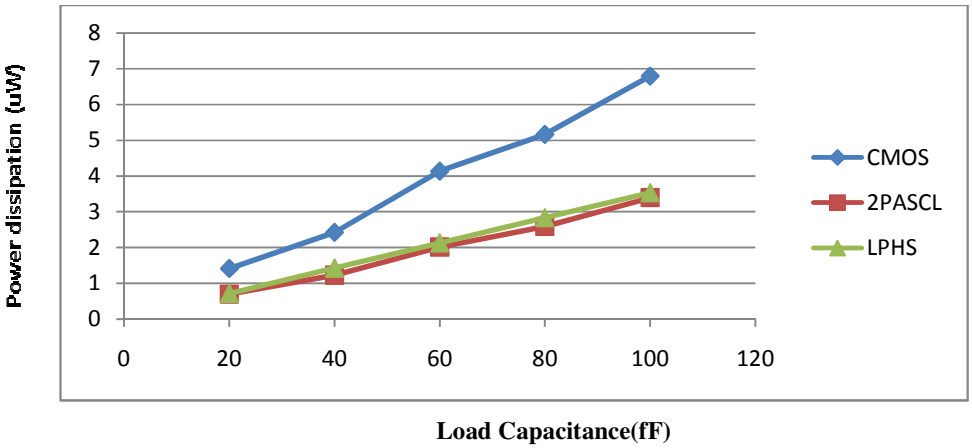

Figure 8. PD Versus C_L Comparison(NAND)

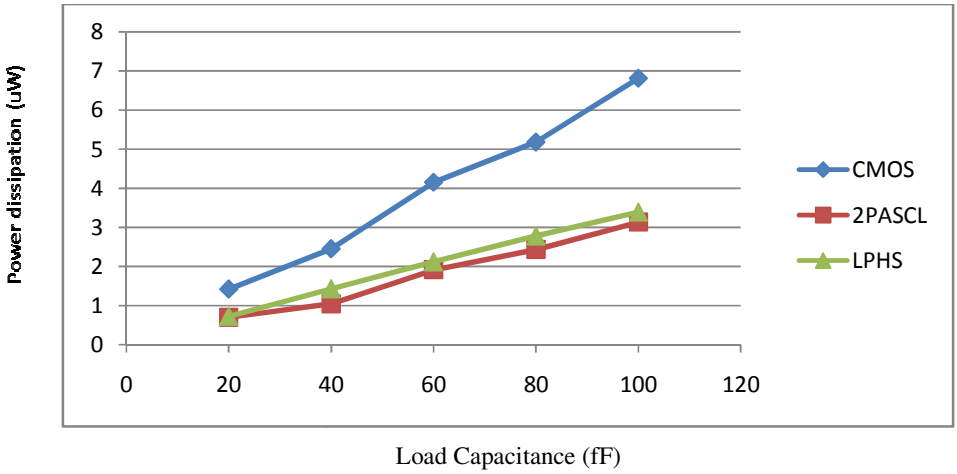

Figure 9. PD Versus C_L Comparison (NOR)

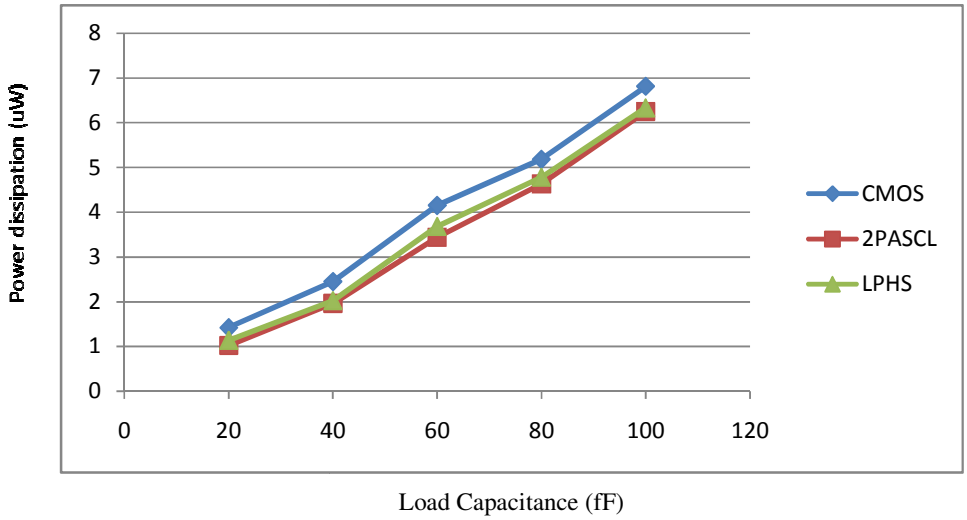

Figure 10. PD Versus C_L Comparison (XOR)

iv. Figures: Four Inverter chain Comparisons.

Figures 11 shows the power dissipation comparison of four inverter chain for CMOS, QAL, Pseudo NMOS QAL, Pseudo NMOS structures at different output load capacitances. Figure 12 shows the delay comparison for the mentioned structures at different loads and Figure 13 shows the Power Delay Product for the different structures at different load. The results have been verified using Cadence tool.

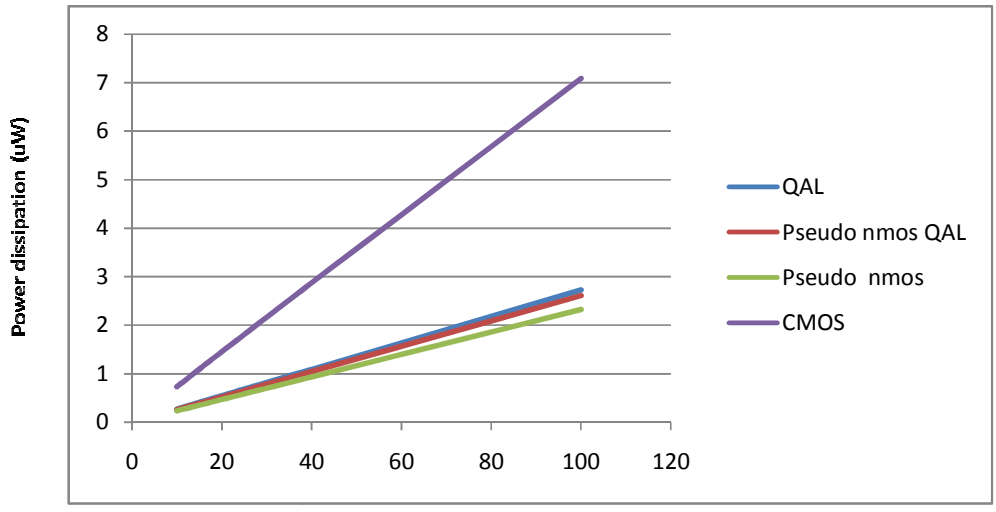

Figure11. PD(µw) Versus C_L Comparison

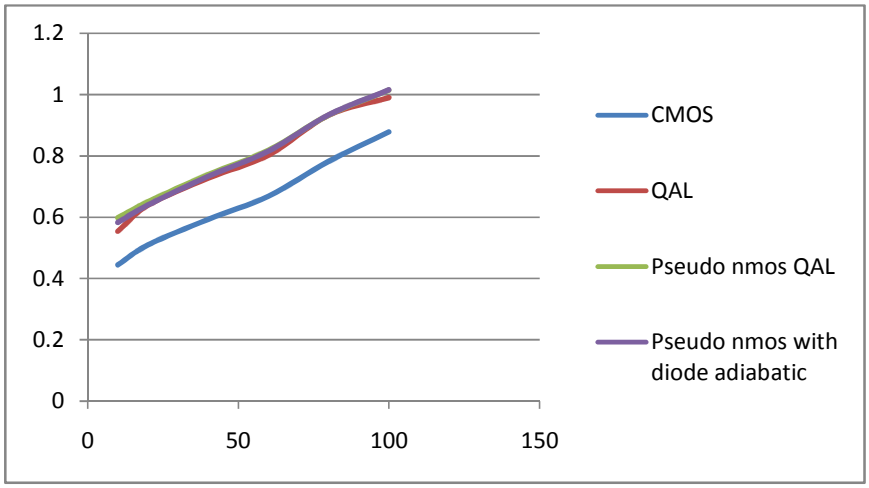

Figure 12. Delay (ns) Versus C_L comparison

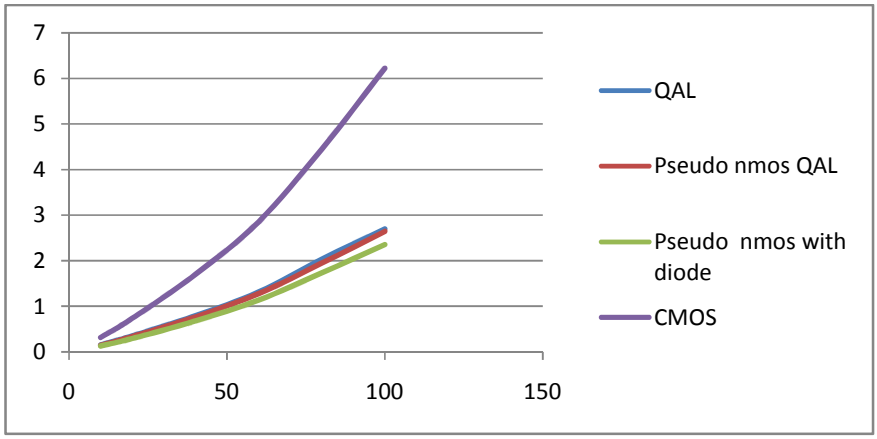

Figure 13. PDP Versus C_L comparison

The functionality of the proposed circuit with variation in different parameters (like load capacitance, frequency and voltage) has been examined. Using proposed adiabatic logic [11], we can reduce delay upto 40% compared with the 2PASCL. LPHS reduces delay at the cost of power dissipation and output swing of the circuit. Output swing reduces from 0.5-1.8 to 0.7-1.8.

Further, it is important to note that the clock plays a very important role for these type of digital circuits not because charge recycling has been employed but due the dependence power consumption on it, there whether single phase clock is being used on two phase it is utmost important to control the clock [11-14].

5. CONCLUSION

This paper primarily focuses on the design of low power high speed CMOS cell structures. A family of full-custom conventional CMOS Logic and an Adiabatic Logic units were designed in Cadence Design Architect using standard TSMC 0.18 µm technology and further the analysis of

the average dynamic power dissipation and delay with respect to the load capacitance was done. It was found that the Proposed adiabatic logic style is advantageous in applications where power reduction as well as speed is of prime importance as in high performance battery-portable digital systems running on batteries such as note-book computers, cellular phones, personal digital assistants, etc. We have achieved an improvement of 60 to 70% in power consumption as compared with Conventional CMOS circuits. This reduction in power consumption is achieved by adiabatic logic with split level power supply. The comparison of the 2PASCL circuit with Conventional CMOS has proved that power consumption with 2PASCL logic is far less as compared to CMOS based technique but delay increases. Delay comparatively increases in 2PASCL but using modified logic we can optimize the circuit between delay, power and output swing.

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