DEVICE CHARACTERISATION OF SHORT CHANNEL DEVICES AND ITS IMPACT ON CMOS CIRCUIT DESIGN

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ABSTRACT

Semiconductor technology has reached an end in the manufacture of conventional Metal Oxide semiconductor Field Effect Transistor (MOSFET). The continuous scaling of semiconductor devices has kept pace with Moore's law and transistors below 1μm are grouped under deep sub-micron (DSM) technology node. But this trend seem to end beyond deep sub micron levels due to main design constraints such as short channel effects (SCE) , and variations in process design parameters leading to high leakage currents. Silicon material processes technology has undergone a change in process material and technology beyond 180nm node. For DSM technology nodes leakage current dominates the devices. Circuit designing using MOSFETs at deep sub micron levels, needs a careful study of the behaviour of short channel devices for the parameter variations such as threshold voltage, channel length leading to high leakage currents and poor performance of devices. In this paper we have presented the behaviour of NMOS metal oxide semiconductor field effect transistor (MOSFETs) for 90nm technology node in detail and finally compared with 180nm and 45nm nodes. The simulations have been carried out using libraries from TSMC foundry and the device has been simulated using Virtuoso Cadence Spectre Simulator version 6.1.5 with HSPICE.

KEYWORDS

MOSFETs; Technology node; process parameter variations; Short Channel Effects; DIBL; leakage current; low power;

1. INTRODUCTION

Scaling down of transistors to Nano meter dimensions has given lot of advantages to circuit designers with respect to area, power and speed optimisation leading to the advancements in chip design. But to keep pace with Moore's law the numbers of transistors per chip have to double every 18 month. In order to improve transistor density periodically is a scaling challenge for circuit designers. The channel length of the transistors is the major focus for controlling manufacturing variations and shorter channel effects. The major design challenges faced due to scaling down of transistors to deep sub micron levels are: threshold variations due to Drain Induced Barrier Lowering (DIBL) and aspect ratio, various leakage currents, channel length modulation (CLM), Gate Induced Barrier Lowering (GIDL) and velocity saturation [4].

The process variation in MOSFETS has been a research challenge in CMOS literature in recent years and has been a critical element in semiconductor fabrication. This observation on process

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parameter random variation was discussed by Shockley in 1961[3] and has been extensively studied and tried to solve in recent 45nm devices. Since the gate of the transistor cannot get much stronger transistor designers are working on two more strategies. They are fully depleted SOI and Fin FETs or Tri-Gate transistors [2]. The impact of scaling down of transistors to Nano- meter nodes has directly influenced power dissipation in VLSI circuits and grows with shrinking node as shown in figure 1. It can be seen from fig.1 that, there is growth in both static and dynamic power consumption in chips. Even though, dynamic power dissipation is found to be lesser at smaller nodes for a given circuit, it increases due to rise in integration density per silicon area. This leads to increase in more no. of switching transistors for given instant, leading to increase in dynamic power dissipation.

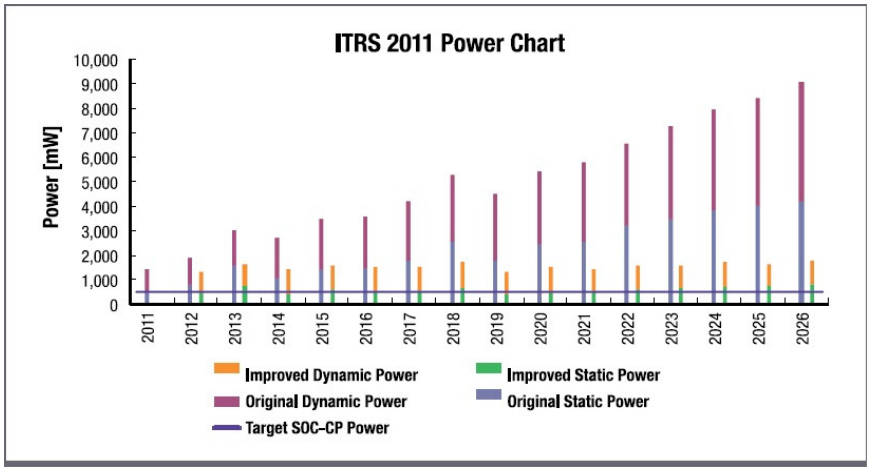

Figure 1. Low power chart showing power dissipation predictions in VLSI chips, ITRS-2011[5]

The ITRS roadmap predicts 2000mW of power dissipation in 2012 and increase by 6000mW by 2020.This paper has been divided in four sections. Section I gives the introduction to the technology scaling, and its importance in semiconductor industry. In section II, we have discussed the impact of scaling on power dissipation in short channel devices and the short channel effects. In section III we have discussed about the device characterisation for different regions of operation. In last section gives a comparative analysis for basic CMOS circuits with respect to power using 180nm, 90nm and 45nm devices.

2. POWER DISSIPATION IN SHORT CHANNEL DEVICES

The power consumption in CMOS circuits with short channel devices is mainly due to the static power dissipation caused due to the leakage currents. As transistor dimensions shrink, supply voltage also has to be scaled down and further threshold voltage is also reduced to maintain the performance. But lower threshold can be achieved only with variation of the process material. But this lowering of threshold voltage has caused new challenges as devices have high off-state leakage currents which reduce the battery life. Power dissipation in CMOS circuits is given by the equations (1) and (2) as below:

$$P_{dyn} = \alpha C_L V_{DD}^{\ 2} fo \quad (1)$$

$$P_{stat} = V_{DD} I_{stat} \quad (2)$$

Where

α = Switching activity of transistors

C_L = Load capacitance

V_{DD} = Supply voltage

f_o = Operating frequency

$I_{leakage}$ = Leakage current when device is in OFF/idle state

P_{dyn} represents equation for dynamic power dissipation caused mainly due to switching activity of the transistors. P_{stat} is the static power dissipation caused due to leakage currents flowing in the device due to various factors. It has been observed that, even though dynamic power dissipation is reduced, static power increases as the technology node shrinks. But overall total power dissipation increases in VLSI chips due to high component density on single chip and high leakage currents.

2.1 Leakage Currents

There are mainly four types of unwanted currents found in short channel devices and these can be further classified as leakage currents and crowbar or short circuit current. The three types of leakage currents in a CMOS circuit are as shown in figure 2 and are as discussed below:

1. Source/Drain junction leakage current;
2. Gate direct tunnelling leakage
3. Sub-threshold leakage through channel of an OFF transistor

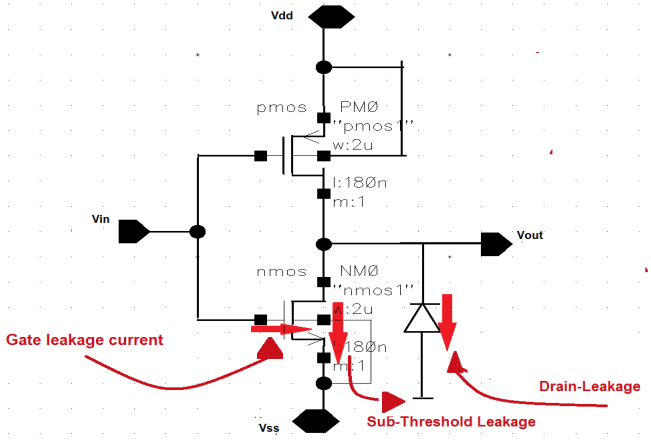

Figure 2. Leakage currents in DSM CMOS circuits

The junction leakage flows from source or drain to the substrate due to reverse biased diodes when a transistor is OFF. This is also called as drain/source leakage current and its magnitude depends on the area of drain diffusion determined by the process technology.

The gate direct tunnelling leakage current flows from the gate though the oxide insulation to the substrate. Its magnitude increases exponentially with the gate oxide thickness T_{ox} and supply voltage V_{DD}. According to the 2001 ITRS, high-k gate dielectric material reduced direct tunnelling current and it has been used in the fabrication of 45nm MOSFETs to control thee leakage current.The sub threshold current is drain-source current of an OFF transistor. This is due

to the diffusion current of the minority carriers in the channel of a MOS device operating in the weak inversion mode (i.e. sub threshold region).Short circuit or crowbar currents are due to simultaneously switching ON of both PMOS and NMOS transistors, where current may flow from V_{DD} to GND for a very short duration.

2.2 Sub-threshold leakage current (I_{sub})

The sub-threshold current is main concern of power dissipation in short channel devices. This is the current which flows in a CMOS circuit below threshold voltage of the devices. It has been investigated that as devices shrink to deep sub micron levels this leakage component increases. It is due to short channel effects of secondary order. That is, as V_{DD} increases, threshold voltage decreases leading to flow of source-drain current. The equation for sub threshold current in weak inversion region is given by equation (3).

$$i_{sub} = \frac{W}{L} I_{DO} \exp\left(\frac{V_{GS}}{\eta(kT/q)}\right) \tag{3}$$

Where,

η = Sub threshold I slope factor ($1<\eta<3$)

I_{DO} = Process dependent parameter and depends on VSB

W/L = is the width to length ratio of leaking MOS device

V_{GS} = Gate to Source voltage

3. DEVICE CHARACTERISATION

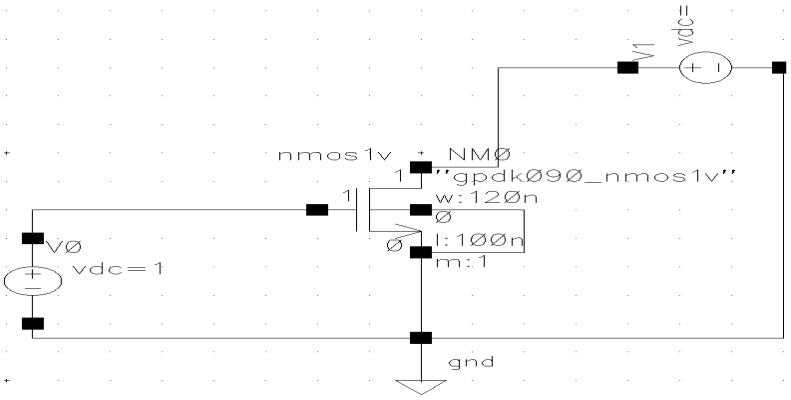

Figure 3. Schematic of NMOS device for dc analysis

Behaviour of short channel devices has been studied using NMOS device, since it shows more design parameter variations compared to PMOS device. The schematic setup for 90nm NMOS transistor is given in figure 3. This device consists of four terminals and they are: source, drain, and gate and body substrate.

In case of NMOS device, source and substrate terminals are grounded whereas drain is connected to supply voltage, V_{DD} and gate is the input terminal which is also connected to dc supply for dc analysis. A MOSFET consists of four regions of operations. First region is triode or linear region where V_{DS} is less than V_{GS}.

This region is also called as sub threshold region of operation. Second and third region form the saturation region. It has been investigated that, second region of operation is dominated by SCE

such as channel length modulation and the third region is dominated by DIBL effect. Fourth region of operation shows substrate current Induced body effect (SCBE) [6].

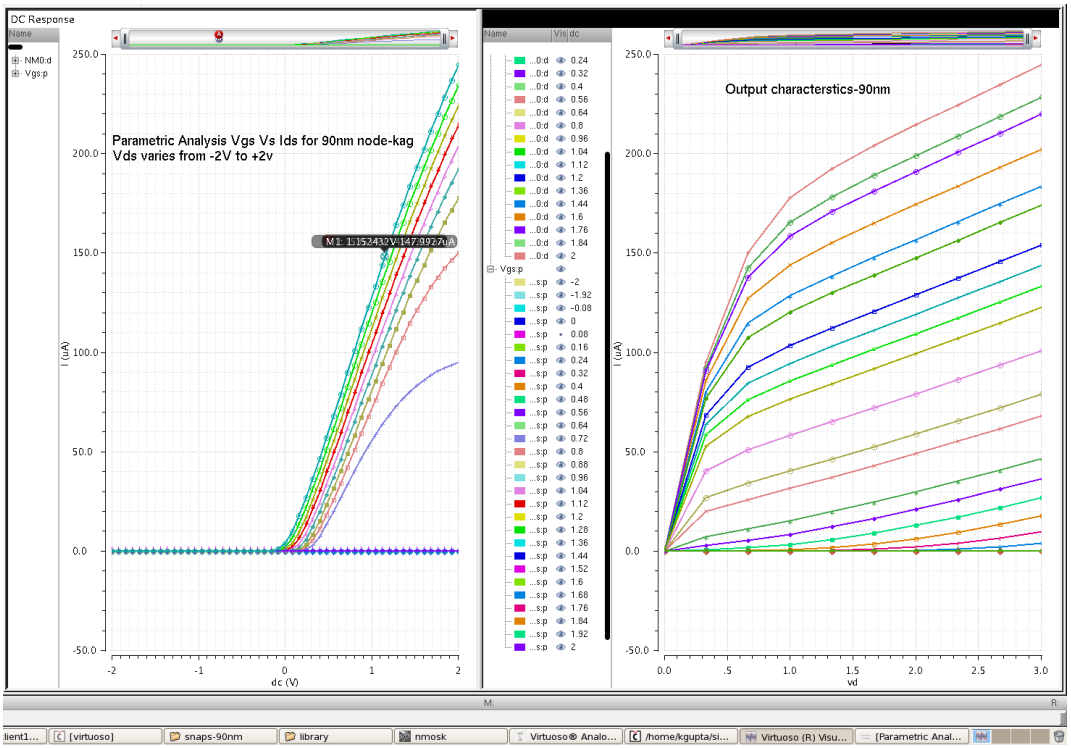

Figure 4. Snapshot of simulation of NMOS Device for 90nm node. Transfer characteristics (left- side) and Drain characteristics (right- side)

Figure 4 shows the parametric DC analysis of 90 nm MOSFET for both transfer and output characteristics. The simulations for transfer characteristics have been carried out for drain voltage V_{DD} ranging from -2 Volts to +2 Volts. In this graph x-axis represents gate voltage and y-axis represents drain current. In this section we have studied behaviour of drain current (I_D) with respect to input voltage and drain voltage. Transfer characteristics curves clearly indicate DIBL effect, which is threshold voltage (V_{GS}) varies for different drain voltages. Study of flow of drain current I_D gives insight into various leakage currents and static power dissipation in CMOS VLSI circuits. Parametric analysis of output characteristics represent plot of V_{DD} Vs I_D for various gate voltages. It can be observed that drain current flows for V_{DD} as low as 0Volts.

3.1 Variation of I_D vs. V_{DD} (Drain Characteristics)

The variation of drain current with drain voltage is called as the output characteristics or drain characteristics. The parametric analysis of I_D Vs V_{DD} for various gate voltages is as shown in figure 4 and 5. In this plot x-axis represents drain voltage and y-axis represents drain current. These curves are used to study the effect of input gate voltage and drain voltage on drain current. It can be observed from fig.4 that there exists OFF-state leakage current for gate voltages below 0 volts. The magnitude of OFF-state current is about 2-7µA.

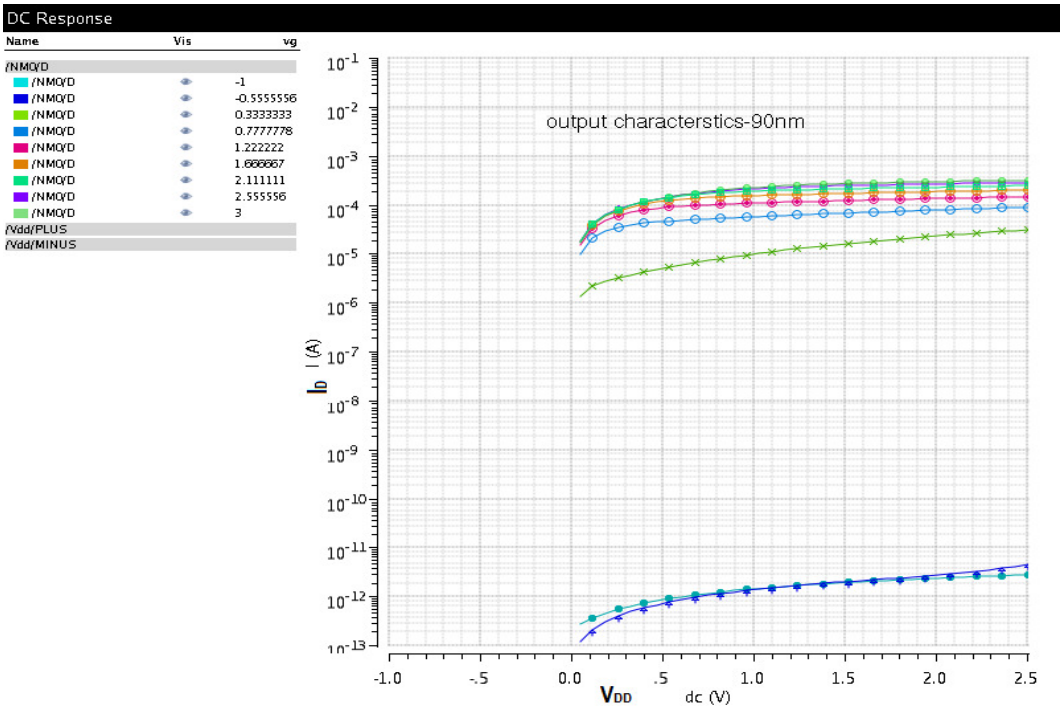

Figure 5. Drain characteristics showing OFF-state and sub-threshold leakage currents.

Table 1 shows the readings tabulated for 90nm NMOS device for different gate voltages. Threshold voltage for 90nm device is around 280mV .We observe that, Sub-threshold voltage (i.e. below threshold voltage) for 0.24V is about 5 microamperes and OFF state leakage current between -1V to 0 Volts ranges from 1.54pA to 61.46nA. These readings have been tabulated for drain voltage of 1.1V.

Table 1. Leakage currents for 90nm NMOS device

Sl	V_{GS} (V)	Drain current
1.	-1	1.54 pA
2	-0.55	1.51 pA
3	-0.11	2.08 nA
4	0	61.46 nA

3.2 Variation of I_D vs. Gate voltage

Transfer characteristics are the plot of drain current versus gate voltage with respect to drain voltage. Fig.6 shows parametric analysis of transfer characteristics for different drain voltages

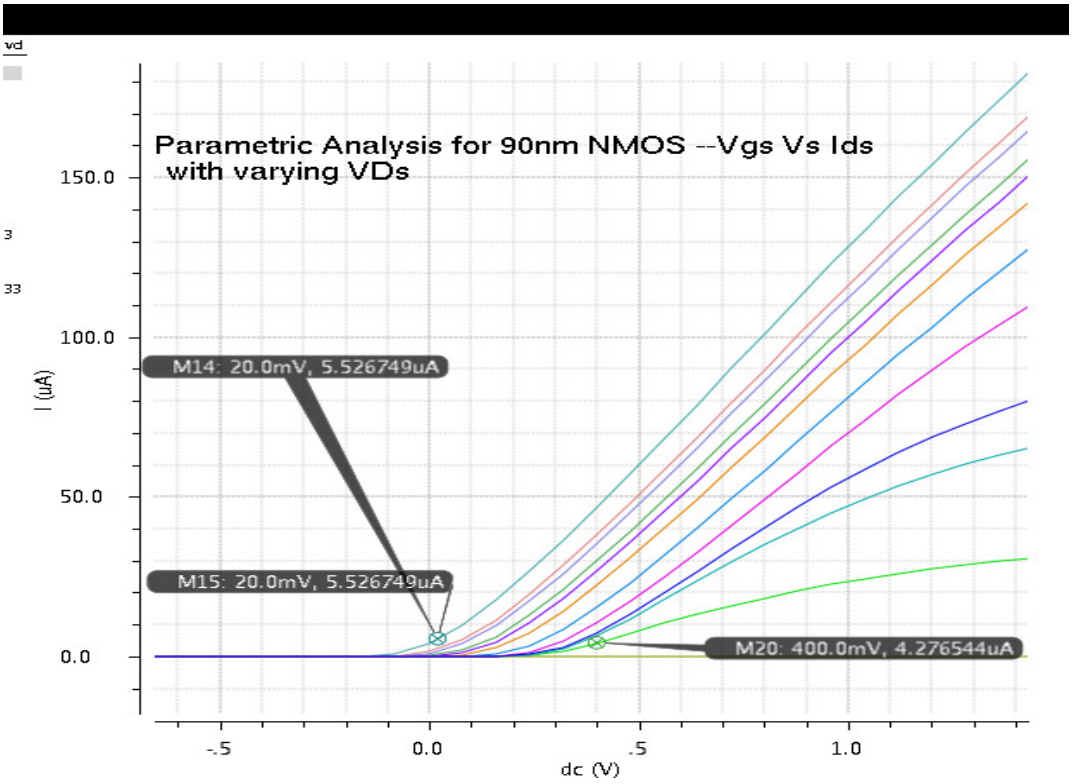

Figure 6. Transfer characteristics of 90nm NMOS transistor

From figure 6, we conclude that there exists leakage current even at V_{GS} below threshold voltage and confirms with the results of previous section. For example, drain current is 5.526uA for V_{GS} very much below threshold voltage i.e. 20mV for higher drain current. But almost same value of I_D can be seen at point M20 for V_{GS} =400mV and VDD=0V. Leakage currents of this magnitude can be very destructing components in VLSI chips. Thus we infer from transfer characteristics that there is reduction in threshold voltage with increase in V_{DD} resulting in more I_D. This is due to short channel effect called drain induced barrier lowering –DIBL and has been discussed in [8].

3.3 Variation of I_D with temperature

In this section we have observed the effect of temperature on various components of leakage current that may flow in NMOS device. The simulations were performed for 90nm technology node for temperature variations from -2°C to 150°C for transfer characteristics as shown in fig.7 and fig.8. It can be observed from curves that I_D decreases with increasing temperature.

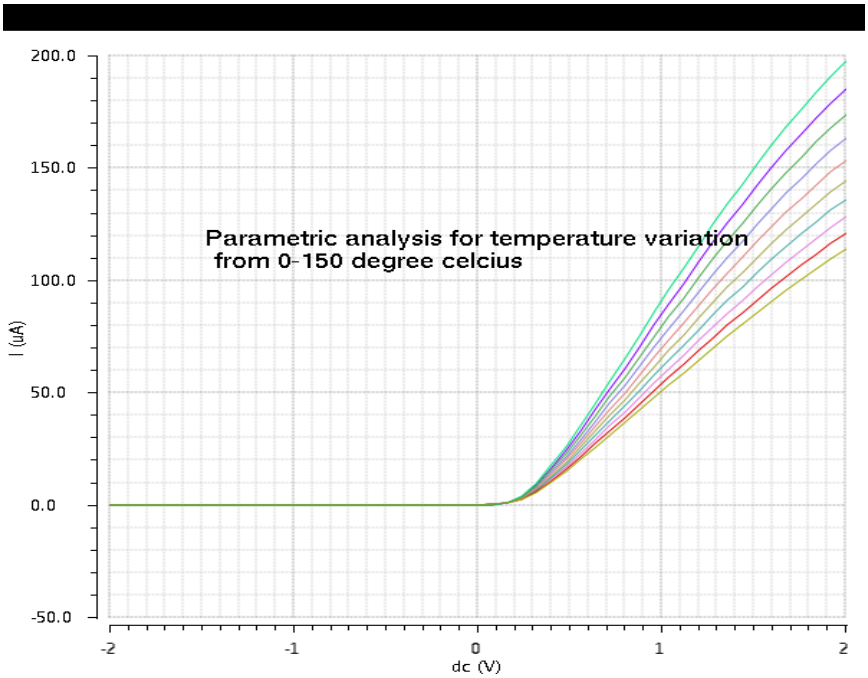

Figure 7. Behaviour of NMOS (90nm) device with respect to temperature

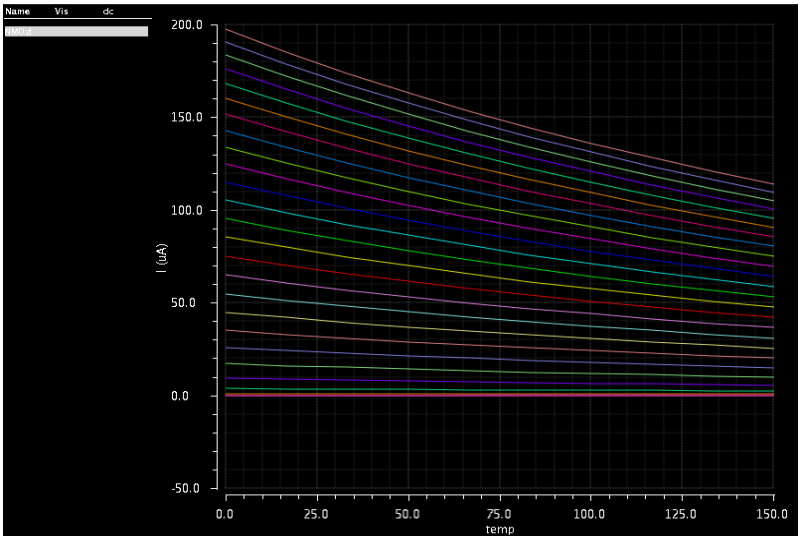

Figure 8. Decrease in I_D with rise in temperature

4. RESULTS AND DISCUSSION

In this section we have compared design parameters with respect to three technology nodes. Table 2 gives the design parameters measured at 27°C and has been extended from previous work [8]. We investigate from the following results that maximum leakage current, I_{OFF} increases as device dimensions shrink. This has become a big challenge for VLSI circuit designers to achieve long battery life for portable devices. Maximum value of I_{OFF} has been identified for gate voltages ranging from -2V to 0V. Interestingly, we see that for 45nm device OFF state current is in micro

amperes at negative voltages example for V_{GS} =-2V, I_{OFF} is 1.6 micro amperes. I_{OFF} is least for 180nm devices.

It can also be observed that, the maximum power is consumed by 180nm device due to dynamic power and more supply voltage. As seen already from eqn. (1) and eqn. (2), both dynamic and static power dissipation directly depends on supply voltage VDD. Since VDD is almost double in case of 180nm device compared to 90 and 45nm devices, total power consumption also increases.

Table 2: Design parameters for MOSFET at DSM technology node

Technology node	**Temp=27˚C**					
	W/L (M) default	***Operating Voltage (V)***	Ids (A)	***Vth (V)***	***Pwr (W)***	***Max. I_{OFF} leakage current (A)***
180nm	2µ/180n	1.8	1.19E-3	0.5429	2.14E-3	2.05E-11
90nm	120n/100n	1.1	83.4E-6	0.274	91.81E-6	61.46E-9
45nm	120n/45n	1	73E-6	0.5872	128.3E-6	1.616E-6

Though total power consumption is less in short channel devices, static power dissipation is more due to leakage currents such as OFF state current and sub-threshold current.

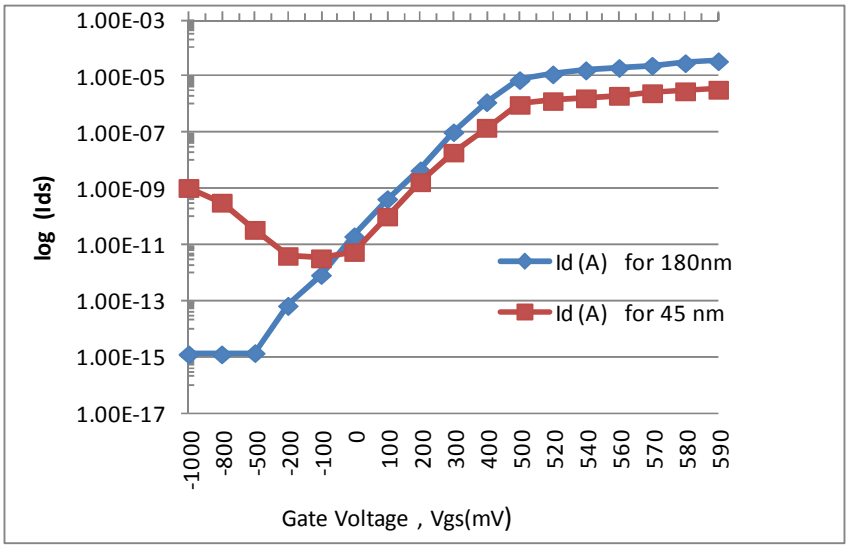

Figure 9. Sub-threshold leakage current curves [8]

Sub-threshold current, I_{sub} is the channel current which flows when gate voltage, V_{GS} is lesser than threshold voltage V_{th}. This is also another important component for leaky transistors and static power dissipation in short channel devices. In can be observed from fig.9, I_{OFF} and sub-threshold leakage current is higher in case of 45nm devices compared to 180nm. From table 2, it can also be observed that leakage current dominates 45 nm devices in spite of changing process technology to improve the threshold voltage compared to 90nm devices to minimise leakage effects. The DIBL effect and leakage currents have been improved in 45nm devices by changes in the process material technology [1]. Thus it has been concluded that as technology node shrinks, leakage currents and threshold variations due to DIBL effect are the main design challenges for CMOS circuit designs.

5. CONCLUSION

Shrinking device parameters have led to chip designers to opt for different design techniques to find trade-off between power and speed. Though low technology nodes have given benefits of high speed VLSI circuits, they have caused serious challenges in the form of leakage currents which will reduce the battery life of systems with portability requirements. In this paper an effort has been made to investigate the behaviour of short channel devices and other short channel effects and their impact on leakage currents at deep sub micron levels. Here, we have considered 180nm, 90nm and 45 nm technology nodes for our study and investigations. We conclude that apart from sub threshold current, off state currents are major design constraints which reduce the battery backup for hand-held low power devices. These design issues still dominate the chips at smaller nodes giving rise to a need of fundamental change of transistor structure or introduction of new circuit design techniques to overcome this problem. A change in the device structure is a major issue in terms of economy and technology replacement. These results give an overview of the impact of leakage currents on CMOS circuit design, being caused due to process technology, gate voltage, supply voltage and temperature variations. The ultimate goal of low power circuit design still remains a challenge to minimize or nullify the leakage currents and SCE which directly degrade performance and reduce longer battery life.

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