OPTIMIZED MULTIPLIER USING REVERSIBLE MULTI-CONTROL INPUT TOFFOLI GATES

H R Bhagyalakshmi[1] and M K Venkatesha[2]

[1]Department of Electronics and Communication Engineering, B M S College of Engineering, Visvesvaraya Technological University, Bangalore, Karnataka
hrbbmsce@gmail.com

[2]Department of Electronics and Communication Engineering, R N S Institute of Technology, Visvesvaraya Technological University, Bangalore, Karnataka
mkvenkatesha@gmail.com

ABSTRACT

Reversible logic is an important area to carry the computation into the world of quantum computing. In this paper a 4-bit multiplier using a new reversible logic gate called BVPPG gate is presented. BVPPG gate is a 5 x 5 reversible gate which is designed to generate partial products required to perform multiplication and also duplication of operand bits is obtained. This reduces the total cost of the circuit. Toffoli gate is the universal and also most flexible reversible logic gate. So we have used the Toffoli gates to construct the designed multiplier.

KEYWORDS

Reversible logic gates, Toffoli gates, partial products, multiplier, quantum computing, Nanotechnology, Future computing.

1. INTRODUCTION

In 1961, Rolf Landauer [2] in his principle stated that the heat coming from computation was due to the destruction of information (wiping out bits of information) and not to the processing of bits. Landauer showed that for every bit of information that is erased during an irreversible logic computation KTln2 joules of heat energy is generated, where K is the Boltzmann constant and T is the temperature in Kelvin at which the system is operating. The heat generated due to the loss of one bit of information is very small at room temperature but when the number of bits is more as in the case of high speed computational works the heat dissipated by them will be so large that it affects the performance and results in the reduction of lifetime of the components.

In 1965, according to 'Moore's law', stated by Gordon Moore, Intel Co-founder, the performance of integrated circuits improve at an exponential rate with the performance per unit cost increasing by a factor of 2 every 18 months. This resulted in shrinking the dimensions on integrated structures to make it possible to operate at higher speed for the same power per unit area [1]. One should not forget that there is a minimum of quantum energy associated with elementary events which puts a fundamental limit on the miniaturization. So the question is, will Moore's law going to end? Using current technology more and more components are getting packed onto the chip and at the same time the power dissipation in the present day computer is very high. So, one of the major current research trends is towards saving of the power. Later C. H. Bennett, in 1973, showed that in order to avoid KTln2 joules of energy dissipation in a circuit it must be built from reversible circuits [3]. Reversible logic ensures zero information loss and low power dissipation.

DOI : 10.5121/vlsic.2012.3603

Groups like the Semiconductor Industries Association (SIA) [4], in their annual study report called the International Technology Roadmap for Semiconductors (ITRS) predict that many areas where technological breakthroughs will be needed to ensure continued progress in the field computation. Reversible logic is one such breakthrough to carry the Moore's law into the future computing.This has motivated many research scholars and scientists to explore the area of reversible logic from various perspectives.

In the present work 4-bit multiplier circuit is constructed using the multi-control input Toffoli synthesis. Toffoli gate is an universal reversible gate and it is used very frequently for the synthesis of a reversible circuit compared to the other gates like Fredkin gate. Toffoli gate synthesis is known to result in a minimum cost circuit, a primary goal of optimization. The reversible logic circuit synthesised usually results in a circuit with higher cost. The reversible logic gates used for the construction of a circuit needs to be implemented using universal gates. This design is presented in this paper which is organized as follows: In Section 2 basic reversible logic gates are discussed. In section 3, the new reversible logic gate, BVPPG gate which is implemented using Toffoli gates is discussed. In Section 4, the design 4-bit multiplier using optimized reversible logic gates and its Toffoli synthesis is presented. In section 5 comparison of the design with the other existing designs is presented. Section 6 presents conclusions with scope for further research.

2. REVERSIBLE LOGIC GATES

A reversible logic gate is an n-input, n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. Also in the synthesis of reversible circuits, direct fan-out is not allowed as one–to-many concept is not reversible. However fan-out in reversible circuits is achieved using additional gates. A reversible circuit should be designed using minimum number of reversible logic gates. So an optimized design of a reversible logic circuit is very important to have the best cost metrics. The important cost metrics [5] which are used to measure the performance of a reversible logic circuit are,

- Gate count-GC- The number of reversible gates used in circuit.
- Line count-LC- Number of circuit lines
- Quantum cost- QC - Cost of the circuit in terms of the cost of a primitive gate.
- Garbage outputs- GO - Number of unused outputs present in a reversible logic circuit

2.1. Basic Reversible logic gates

2.1.1 Feynman Gate

Figure 1 shows a 2*2 Feynman gate [6]. Quantum cost of a Feynman gate is 1.Feynman gate is called as Controlled NOT gate or CNOT gate. It is equivalent to single control input Toffoli gate.

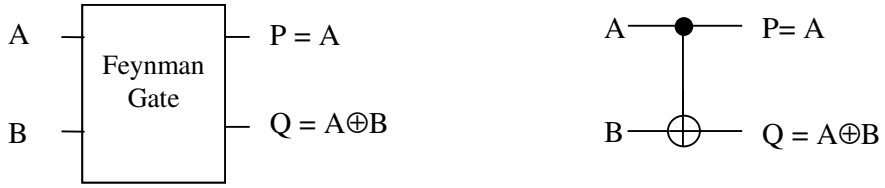

Figure 1: Feynman gate and its symbolic representation

2.1.2. Toffoli Gate

Figure 2 shows a 3*3 Toffoli gate [7] The input vector is I(A, B, C) and the output vector is O(P,Q,R). The outputs are defined by P=A, Q=B, R=AB⊕C. Quantum cost of a Toffoli gate is 5. It has two control inputs.

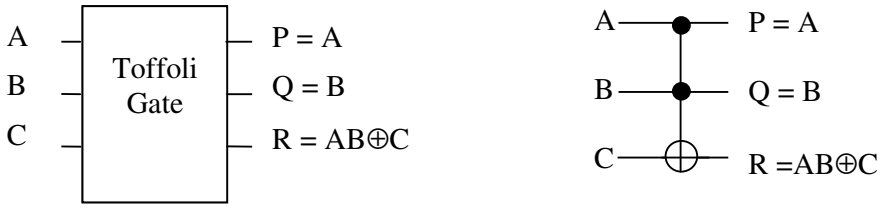

Figure 2: Toffoli gate and its symbolic representation

2.1.3. Peres Gate

Figure 3 shows a 3*3 Peres gate [8]. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P = A, Q = A⊕B and R=AB⊕C. Quantum cost of a Peres gate is 4. It is needs two Toffoli gates for its construction.

Figure 3. Peres gate and its Toffoli gate representation

2.1.4. Double Peres Gate

Figure 4 shows a Double Peres Gate [14, 26] and its Toffoli representation. The quantum cost of a DPG gate is calculated to be equal to 6 from its quantum realization.

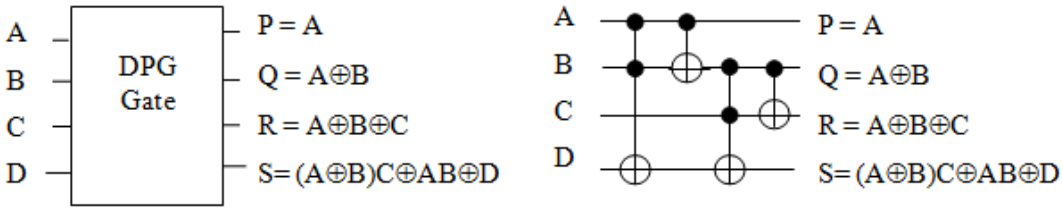

Figure 4. DPG gate and its Toffoli representation

3. NEW REVERSIBLE LOGIC GATE

3.1 BVPPG gate

BVPPG gate is a 5 * 5 reversible gate and its logic diagram is as shown in figure 6. Its quantum cost is 10. Ffoli representation of the BVPPG gate is a shown in the figure 7. The truth table of BVPPG is as shown in the Table -1.

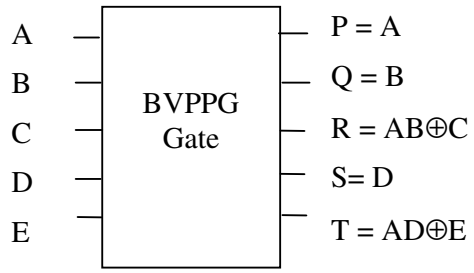

Figure 6. BVPPG gate

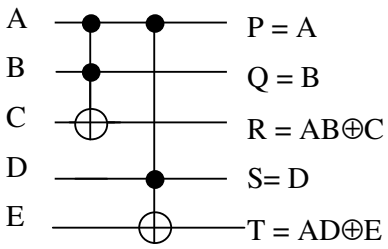

Figure 7: Toffoli gate representation of BVPPG gate

The BVPPG gate is used to construct the partial product generator which has resulted in least number of gates, least quantum cost and least number of garbage outputs. The two product terms are available at the outputs R and T of the BVPPG gate with C and E inputs maintained constant at 0. The other outputs namely P, Q and S are used for fan-out of the multiplier operands as shown in figure 8.. This reduces the number of external fan-out gates to zero in our design which is main design feature. The proposed design is compared with the existing designs [11-22].

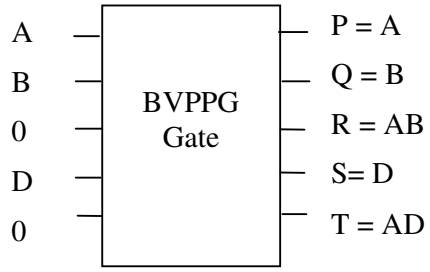

Figure 8: BVPPG gate producing product terms and duplication of the inputs.

Table 1: Truth table of BVPPG gate

Truth table									
INPUTS					OUTPUTS				
A	**B**	**C**	**D**	**E**	**P**	**Q**	**R**	**S**	**T**
0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	0	0	1	0
0	0	0	1	1	0	0	0	1	1
0	0	1	0	0	0	0	1	0	0
0	0	1	0	1	0	0	1	0	1
0	0	1	1	0	0	0	1	1	0
0	0	1	1	1	0	0	1	1	1
0	1	0	0	0	0	1	0	0	0
0	1	0	0	1	0	1	0	0	1
0	1	0	1	0	0	1	0	1	0
0	1	0	1	1	0	1	0	1	1
0	1	1	0	0	0	1	1	0	0
0	1	1	0	1	0	1	1	0	1
0	1	1	1	0	0	1	1	1	0
0	1	1	1	1	0	1	1	1	1
1	0	0	0	0	1	0	0	0	0
1	0	0	0	1	1	0	0	0	1
1	0	0	1	0	1	0	0	1	0
1	0	0	1	1	1	0	0	1	1
1	0	1	0	0	1	0	1	0	0
1	0	1	0	1	1	0	1	0	1
1	0	1	1	0	1	0	1	1	1
1	0	1	1	1	1	0	1	1	0
1	1	0	0	0	1	1	1	0	0
1	1	0	0	1	1	1	1	0	1
1	1	0	1	0	1	1	1	1	1
1	1	0	1	1	1	1	1	1	0
1	1	1	0	0	1	1	0	0	0
1	1	1	0	1	1	1	0	0	1
1	1	1	1	0	1	1	0	1	1
1	1	1	1	1	1	1	0	1	0

4. DESIGN OF 4-BIT MULTIPLIER

Multipliers are very important in various processing steps of a computational operation. There are different approaches of a multiplier design using reversible logic gates [11-22]. The proposed multiplier uses parallel multiplier consists of two steps.

- Part I: Partial Product Generation (PPG)
- Part II: Multi-Operand Addition (MOA)

The operation of a 4*4 reversible multiplier is shown in figure 9. It consists of 16 Partial product bits of the X and Y inputs to perform 4 * 4 multiplications. However, it can extended to any other n * n reversible multiplier.

Partial Product Generation					x_3	x_2	x_1	x_0
					y_3	y_2	y_1	y_0
					P_{03}	P_{02}	P_{01}	P_{00}
				P_{13}	P_{12}	P_{11}	P_{10}	
Multi operand Addition			P_{23}	P_{22}	P_{21}	P_{20}		
		P_{33}	P_{32}	P_{31}	P_{30}			
	Z_7	Z_6	Z_5	Z_4	Z_3	Z_2	Z_1	Z_0

Figure 9. Operation of the 4×4 parallel multiplier.

4.1 Partial Product Generator (PPG)

The proposed design of a 4 x 4 multiplier circuit in reversible logic requires 4 copies of each operand bit. In the existing literature on multiplier [13-16] operand bits are copied using 24 Feynman gates and in [14] the fan-out of input operands is achieved using 12 BVF gates. In [11] built-in fan-out using Toffoli gates and Peres gates is used .But in the proposed multiplier design duplication of the operands is achieved without using external fan-out gates.

BVPPG gates are used instead of Peres gates [12] for the construction of partial product generator. The BVPPG gate is a 5 x 5 reversible logic gate and has a quantum cost of 10. It has a unique feature that it can pass through three inputs. Also it can produce two product terms simultaneously with two constant inputs. This feature of BVPPG gate reduces the number of reversible gates of the circuit compared to the designs of [12-22]. The figure 10 shows the partial product generator using new BVPPG gates. The new BVPPG gate is similar to a double Toffoli gate or it is equal to a Toffoli gate with 4 control inputs

The input operands x_3, x_2, x_1, x_0 and y_3, y_2, y_1, y_0 are used directly and only once. The BVPPG gate outputs the operands along with the product terms which are used as inputs to the next BVPPG gate to generate other product terms. To the best of our knowledge ours is the first design to get partial products without using fan-out gates with only 8 reversible gates and also to construct the Toffoli gate structure of the multiplier. In paper [12], 7 Peres gates and 9 Toffoli gates are used to generate the product terms without fan-out gates but number of gates is more than that used in our design.

.

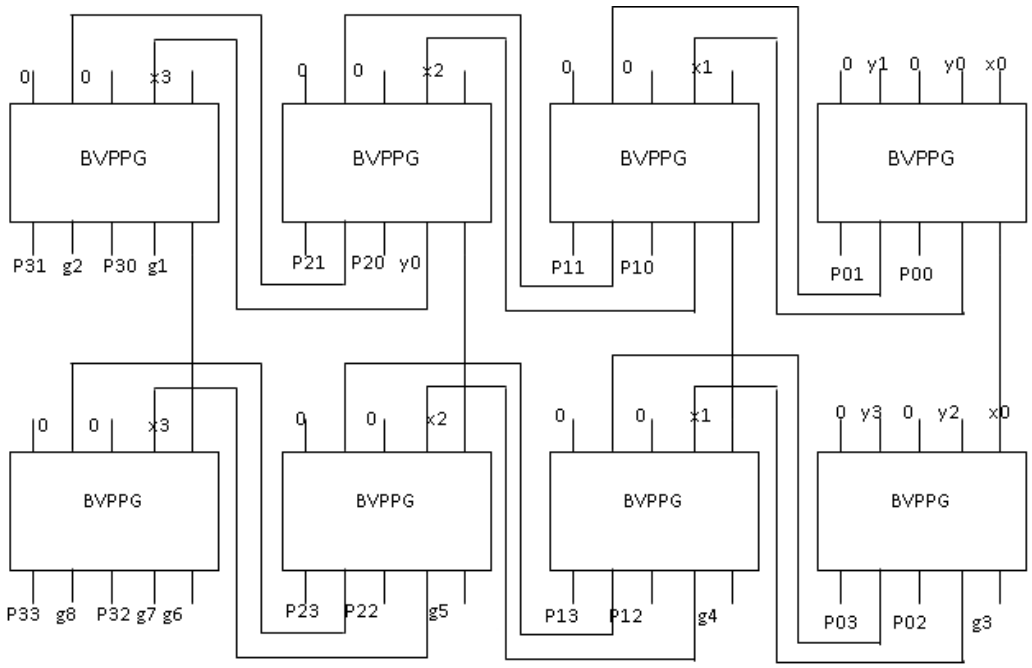

Figure 10. Partial product generator using BVPPG gates

The Toffoli gate implementation of the partial product generator obtained using RevKit-tool [9, 10, 23] is as shown in the figure 11.

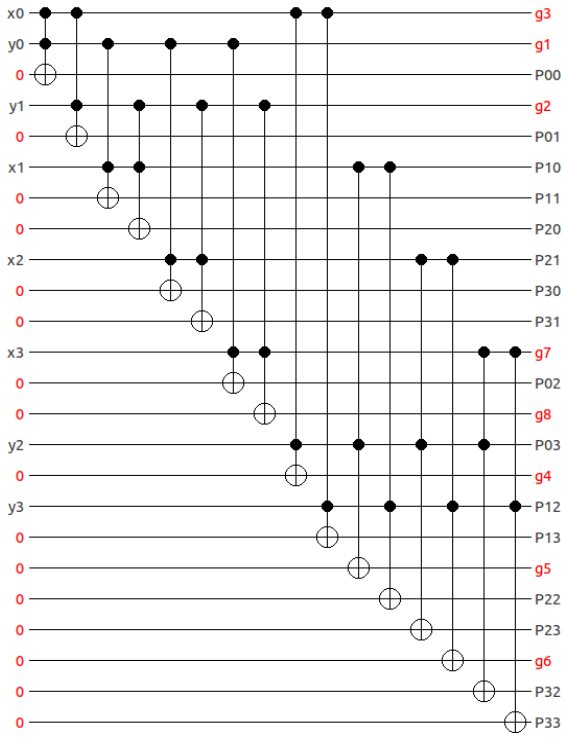

Figure 11. Toffoli cascade of Partial product generator using BVPPG gates

The partial products generator using BVPPG gates is simulated using Revkit and Dinotrace waveform simulator. The simulation result is as shown in the figure 12.

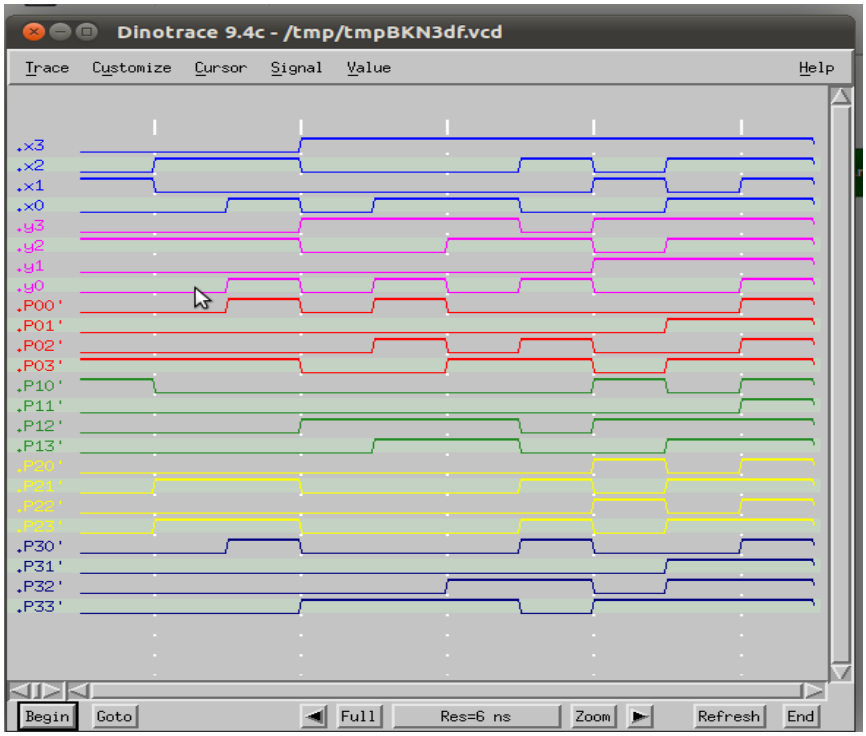

Figure 12. Simulation result of partial product generator using BVPPG gates

4.2. Multi-Operand Addition (MOA)

As proposed in [8], to implement an n operand addition circuit part a carry save adder (CSA) is used. The CSA tree reduces the four operands to two. Thereafter, a Carry Propagating Adder (CPA) adds these two operands and produces the final 8-bit product. The proposed four operand adder shown in the figure 13 uses DPG gate as a reversible full adder and Peres gate as half adder.

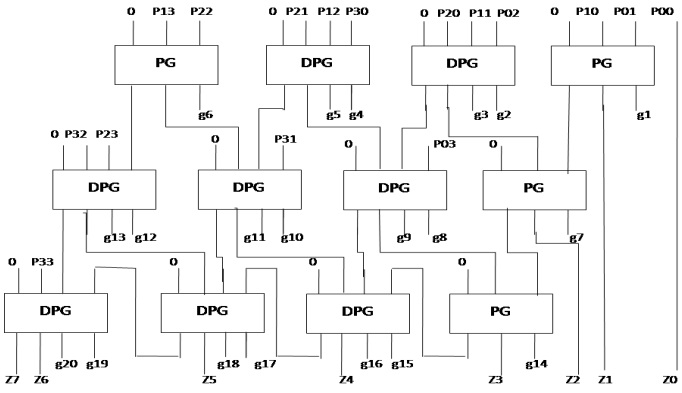

Figure 13. Four operand addition circuit-MOA

The existing 4*4 gates namely DPG [12], HNG [13], PFAG [14], MKG [15] and TSG [16], and can be individually used as an adder. It is shown that use of DPG gate [12] reduces the quantum cost of the multiplier to a minimum value.

In the designed reversible multi-operand addition circuit 8 DPG gates and 4 Peres gates are used and the total quantum cost of multi-operand addition circuit is 64. The multiple control Toffoli gate is frequently used for the synthesis of reversible circuits [19-22]. The Toffoli gate implementation of the multi-operand addition circuit obtained using RevKit [19, 20] is as shown in the figure 14.

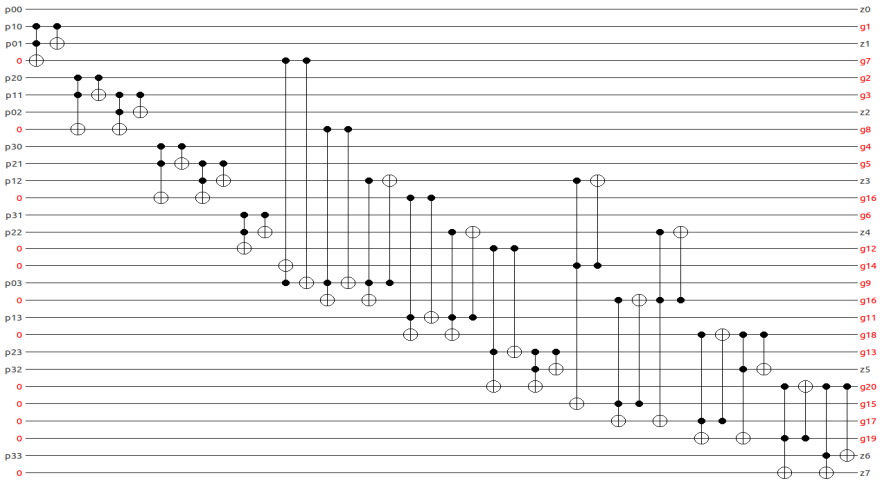

Figure 14. Toffoli cascade of multi-operand adder(MOA) block

The multi-operand addition circuit simulated using Revkit and Dinotrace waveform simulator is as shown in the figure 15.

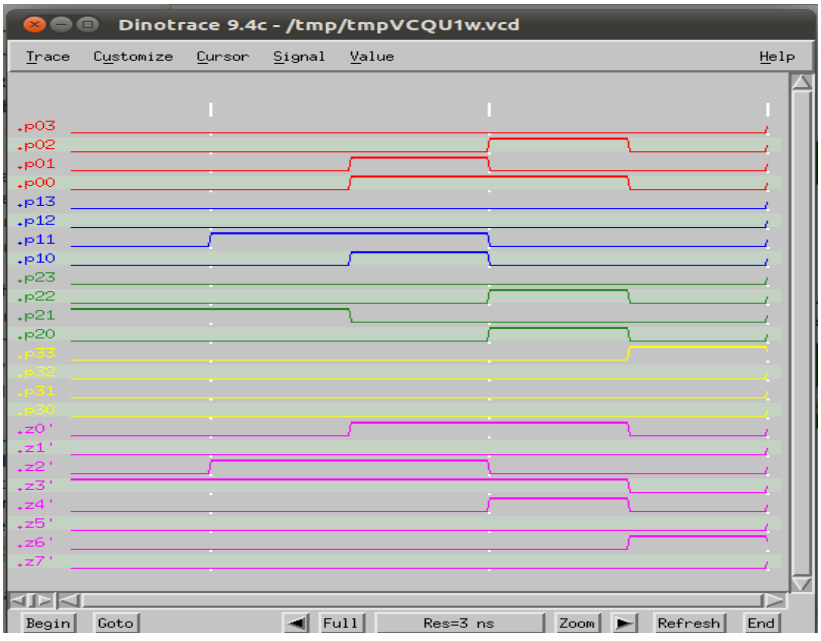

Figure15. Simulation waveform of MOA block

The complete multiplier circuit is simulated using Revkit and Dinotrace waveform viewer. The block diagram of the multiplier circuit is as shown in the figure 16 and the simulation result obtained using Dinotrace waveform viewer is as shown in the figure 17.

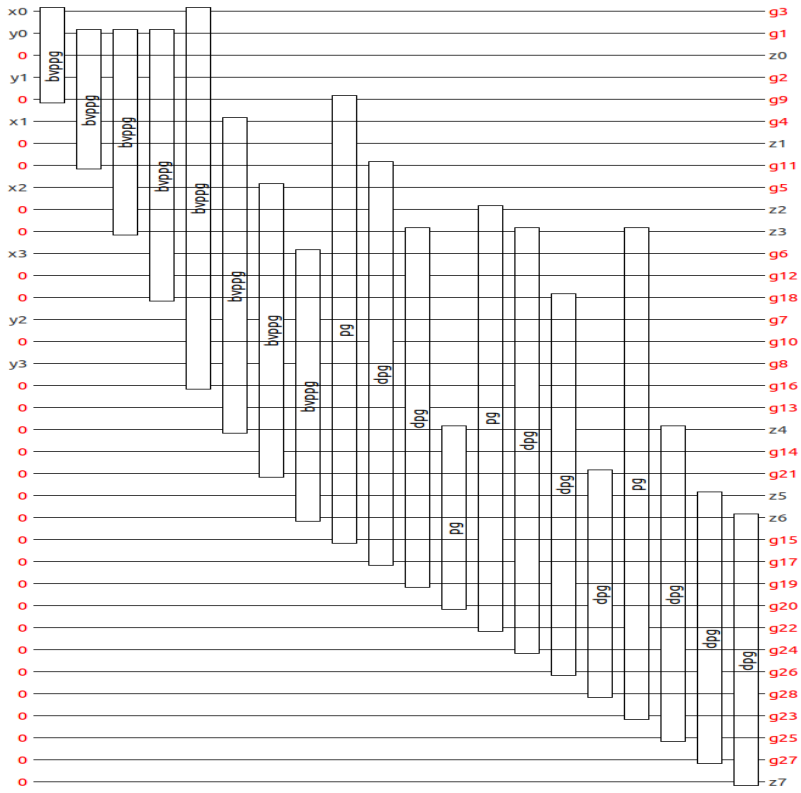

Figure16.RevKit implementation of the complete multiplier circuit

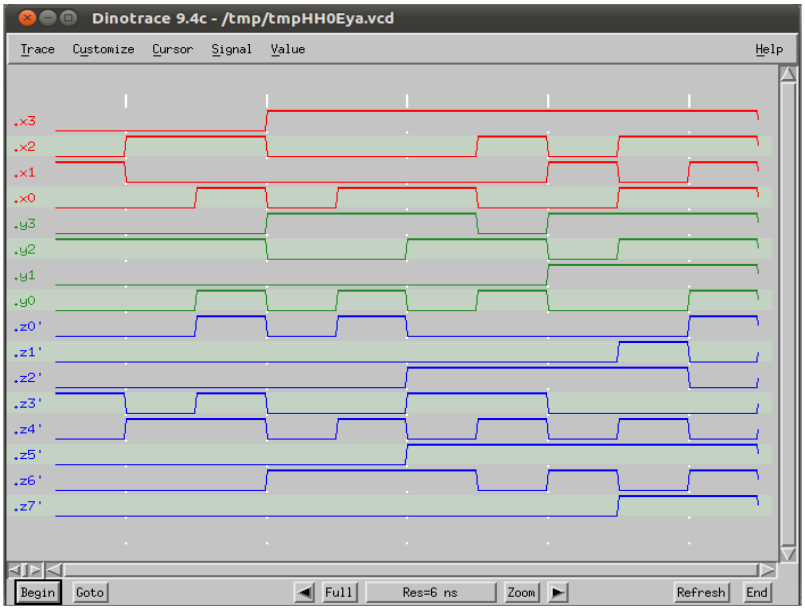

Figure17. Simulation waveform of the complete 4-bit multiplier

5. RESULTS AND DISCUSSION

The table 2 shows the parameters of the Toffoli implementation of the presented design obtained by simulating the circuit using RevKit. Each BVPPG gate needs two Toffoli gates having two control inputs. Similarly a Peres gate is constructed using two 2-control input Toffoli gates. The parameter line count directly indicates the number of Qubits (quantum bits) and the circuit cost , a useful parameter for building the quantum circuit. The number of circuit lines and quantum cost can be further reduced by post synthesis optimization technique which is beyond the scope of our design approach. The parameter 'Transistor Cost' refers to the number of transistors required if the CMOS technology is adopted for the design[5,23, 24].

Table 2: Parameters of the Toffoli implementation of the design

Parameters	PPG	MOA	Multiplier
Gate count	16	40	56
Line count	24	28	36
Garbage output	8	20	28
Quantum cost	80	120	200
Transistor cost	256	480	736

Table 3 shows the comparison of partial product generator of our design with the other existing designs [12-22]. In this paper only 8 BVPPG gates are used to generate the same and is a better circuit as it has less hardware complexity and least quantum cost compared to other designs [14-22]. The number of constant inputs and number of garbage outputs is reduced by more than 50% which makes this circuit a very optimized compared to the other designs existing in the literature.

Table 3 Comparison of different designs of Partial product generator

Designs	Gate count N	Constant inputs CI	Garbage outputs GO	Quantum cost QC	Types of Gates used
Proposed Design	**8**	**16**	**8**	**80**	**BVPPG-8**
Paper[12]	16	16	8	73	PG-7;TG-9
Paper[13]	28	28	20	76	PG-16;FG-12
Paper[14]	28	40	32	88	PG-16;BVF-12
Paper[15]	40	40	32	88	PG-16, FG-24
Paper[16]	40	40	32	88	PG-16, FG-24
Paper[17]	40	40	32	88	PG-16, FG-24
Paper[18]	40	40	32	88	PG-16, FG-24
Paper[19]	40	40	32	88	PG-16, FG-24
Paper[20]	24	32	32	96	FRG-16;F2G-8
Paper[21]	28	28	32	104	FRG-16;F2G-8
Paper[22]	40	40	32	104	FRG-16;FG-24

Table 4 shows the comparative study of the Multi-operand adder block of the design with the existing designs and table 5 gives the comparison of the complete multiplier designs.

Table 4: Comparison of different designs of Multi-operand adder circuit

Designs	Gate count N	Constant inputs CI	Garbage outputs GO	Quantum cost QC	Gates used -
Proposed design	**12**	**12**	**20**	**64**	**PG-4; DPG-8**
Paper[12]	12	12	20	64	PG-4;HNG-8
Paper[13]	12	12	20	64	PG-4; DPG-8
Paper[14]	12	12	20	64	PG-4; DPG-8
Paper[15]	12	12	20	64	PG-4;PFAG-8
Paper[16]	12	12	20	64	PG-4;HNG-8
Paper[17]	12	12	20	64	PG-4;HNG-8
Paper[18]	12	12	20	80	PG-4;PFAG-8
Paper[19]	12	16	24	120	MKG-12
Paper[22]	13	18	26	130	TSG-13
Paper[20]	20	24	32	140	IG-20
Paper[21]	20	24	32	140	MIG-20

Table 5: The comparison of the proposed multiplier design with other existing multipliers

Designs	Gate count N	Constant inputs CI	Garbage outputs GO	Quantum cost QC
Proposed Design	**20**	**28**	**28**	**144**
Paper[12]	28	28	28	137
Paper[13]	40	40	40	140
Paper[14]	40	52	52	152
Paper[15]	52	52	52	152
Paper[16]	52	52	52	152
Paper[17]	52	52	52	152
Paper[18]	52	52	52	168
Paper[19]	52	56	56	208
Paper[20]	44	56	64	236
Paper[21]	48	52	64	244
Paper[22]	53	58	58	234

6. CONCLUSIONS

The focus of this paper is the application of a reversible logic gate to realize a 4-bit multiplier using a new reversible logic gate which is designed keeping in view the optimization factors of the reversible circuits and is synthesized using Toffoli synthesis. Toffoli gate circuits has been demonstrated as a promising alternative to achieve minimal reversible circuits than that achieved using heuristic synthesis approach namely the transformation-based method.
The quantum costs directly depend on the used Toffoli gates and its control inputs. The table 6 shows the cost of Toffoli gates with different control inputs [9, 25, and 27].

Table 6: Quantum costs of Toffoli gates with multiple control inputs

Number of Control inputs	Quantum cost
0	1
1	1
2	5
3	13
4	26- if atleast 2 lines are unconnected 29-otherwise
5	38- if atleast 3 lines are unconnected 52- if atleast 1-2 lines are unconnected 61-otherwise
6	50- if atleast 4 lines are unconnected 80- if atleast 1,2 or 3 lines are unconnected 125-otherwise

The design presented in this paper uses BVPPG gate , a new reversible logic gate whose Toffoli equivalent shows that the number of control inputs equal to 4 but however the quantum cost obtained by implementing it using RevKit tool shows 10. Hence it is an optimized gate and using BVPPG gate for the construction of partial product generator of 4-bit multiplier has optimized the circuit. It is observed that the design presented in this work has a level of optimization more than the optimization level of the existing designs and it is improved version of our previous work [14]. Other synthesis methods and post synthesis optimization techniques are under investigation as a future work.

ACKNOWLEDGEMENTS

The authors wish to thank ECE department of BMS college of Engineering, Bangalore, Karnataka, India for supporting this work.

REFERENCES

[1] Gordon E. Moore, “Cramming more components onto integrated circuits”, Electronics Volume 38, number 8, April 19, 1965.
[2] R. Landauer, "Irreversibility and heat generation in t he computing process," IBM Journal. Research and Development, vol. 3, pp. 183-191, July 1961.
[3] C. H. Bennett, "Logical reversibility of computation," IBM J. Research and Development, pp. 525-532, November 1973.
[4] DeBenedictis, E. Will Moore’s Law be Sufficient? in proceedings of supercomputing, 2004.

[5] R. Drechsler R. Wille. "Towards a design flow for reversible logic", Springer, 2010.
[6] R. Feynman, "Quantum Mechanical Computers," Optics News, Vol.11, pp. 11–20, 1985.
[7] T.Toffoli, "Reversible computing", technical report, Tech memo MIT/LCS/TM-151, MIT Lab for Computer Science, 1980.
[8] A. Peres, "Reversible Logic and Quantum Computers", Physical review A, 32:3266- 3276,1985.
[9] G. W. Dueck D. Maslov and D. M. Miller. "Toffoli network synthesis with templates".Vol. 24, pp , 807–817. IEEE Transaction on CAD, 2005.
[10] M. Soeken R. Wille and R. Drechsler. "Reducing the number of lines in reversible circuits". pp 647–652, In Design Automation Conference (DAC), 2010.
[11] Anindita Banerjee and Anirban Pathak 'An analysis of reversible multiplier circuits', arXiv: 0907.3357 (2009), 1-10.
[12] Mohammad Assarian, Majid Haghparast and Keivan Navi, "Delay Reduction in Optimized Reversible Multiplier Circuit", Research Journal of Applied Sciences, Engineering and Technology 4(1): 27-32, 2012,ISSN: 2040-7467, January 01, 2012.
[13] Mihail Cutitaru, Lee A. Belfore II, "Improved Cost Reversible Multiplier Design", WORLDCOMP'11 - The 2011 World Congress in Computer Science, Computer Engineering, and Applied Computing, July 18-21,2011,Old Dominion University, Norfolk, Virginia, USA.
[14] H. R. Bhagyalakshmi, M. K. Venkatesh, "An Improved Design of a Multiplier using Reversible Logic Gates," in International Journal of Engineering Science and Technology, Vol. 2, No. 8, 2010.
[15] Fateme Naderpour, Abbas Vafaei "Reversible Multipliers: Decreasing the Depth of the Circuit" ICECE 2008, 20-22 December 2008.
[16] Maryam Ehsanpour , Payman Moallem, Abbas Vafaei, "Design of a Novel Reversible multiplier Circuit Using Modified Full Adder", 2010 International Conference On Computer Design And Applications, 1389, (ICCDA 2010).
[17] M. Haghparast, S. Jafarali Jassbi, K. Navi and O. Hashemipour, "Design of a Novel Reversible Multiplier Circuit Using HNG Gate in Nanotechnology", World Applied Science Journal Vol. 3 No. 6, pp. 974-978, 2008.
[18] M.S. Islam et al., "Low cost quantum realization of reversible multiplier circuit", Information technology journal, Vol.8, pp 208-213, 2009.
[19] M. Shams, M. Haghparast and K. Navi, "Novel Reversible Multiplier Circuit in nanotechnology", World Applied Science Journal Vol. 3, No. 5, pp. 806-810, 2008.
[20] Nidhi Syal, Dr. H.P. Sinha, "Design of fault tolerant reversible multiplier", International Journal of Soft Computing and Engineering (IJSCE) ISSN: 2231-2307, Volume-1, Issue-6, January 2012.
[21] Somayeh Babazadeh and Majid Haghparast, "Design of a Nanometric Fault Tolerant Reversible Multiplier Circuit", Journal of Basic and Applied Scientific Research, Text Road Publication, 2(2)1355-1361, 2012,ISSN 2090-4304,www.textroad.com
[22] H. Thapliyal and M.B. Srinivas, "Novel Reversible Multiplier Architecture Using Reversible TSG Gate", Proc. IEEE International Conference on Computer Systems and Applications, pp. 100-103, March 2006.
[23] M. Soeken,S. Frehse,R. Wille and R. Drechsler, " RevKit: An Open Source Toolkit for theDesign of Reversible Circuits", Springer- Lecture Notes in Computer Science, vol- 7165, pages 64-76, in Reversible Computation 2011,RevKit is available at www.revkit.org.
[24] R. Wille, D. Grobe, G. W. Dueck and R. Drechsler, " RevLib: An Online Resource for Reversible Functions and Reversible Circuits", International Symposium on Multiple-Valued Logic (ISMVL), pages 220–225, 2008.
[25] R. Wille D. M. Miller and Z. Sasanian. "Elementary quantum gate realizations for multiple-control toffoli gates". International Symposium on Multi-Valued Logic, IEEE, 2011.
[26] Md Belayet Ali , Md Mosharof Hossin and Md Eneyat Ullah, " Design of Reversible Sequential Circuit Using Reversible Logic Synthesis " , International Journal of VLSI design and Communication Systems (VLSICS) Volume 2, No.4, December 2011.
[27] D. Große, R. Wille, G.W. Dueck, and R. Drechsler, "Exact multiple control Toffoli network synthesis with SAT techniques" , IEEE Trans. On CAD, 28(5):703–715, 2009.