REALIZATION OF TRANSMITTER AND RECEIVER ARCHITECTURE FOR DOWNLINK CHANNELS IN 3-GPP LTE

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ABSTRACT

Long Term Evolution (LTE), the next generation of radio technologies designed to increase the capacity and speed of mobile networks. The future communication systems require much higher peak rate for the air interface but very short processing delay. This paper mainly focuses on to improve the processing speed and capability and decrease the processing delay of the downlink channels using the parallel processing technique. This paper proposes Parallel Processing Architecture for both transmitter and receiver for Downlink channels in 3GPP-LTE. The Processing steps include Scrambling, Modulation, Layer mapping, Precoding and Mapping to the REs in transmitter side. Similarly demapping from the REs, Decoding and Detection, Delayer mapping and Descrambling in Receiver side. Simulation is performed by using modelsim and Implementation is achieved using Plan Ahead tool and virtex 5 FPGA.Implemented results are discussed in terms of RTL design, FPGA editor, power estimation and resource estimation.

KEYWORDS

PBCH, PMCH, PDCCH, PDSCH, PCFICH, OFDM, MBSFN, MBMS

1. INTRODUCTION

The LTE PHY is a highly efficient means of conveying both data and control information between an enhanced base station and mobile user equipment. LTE physical layer is quite complex and consists of mixture of technologies. LTE takes advantage of OFDMA, a multi-carrier scheme that allocates radio resources to multiple users. LTE standard has six physical layer channels namely, physical Hybrid ARQ Indicator Channel (PHICH), Physical Control format Indicator Channel(PCFICH), Physical Downlink Control Channel (PDCCH), Physical Broadcast channel (PBCH), Physical Multicast Channel (PMCH) and Physical Downlink Shared Channel (PDSCH) for downlink operation[1]. The control signals are transmitted at the start of each subframe.

LTE supports peak data rates of up to 100 Mbps on the downlink and 50 Mbps on the uplink when using a 20 MHz channel bandwidth.LTE supports both frequency-division duplex (FDD) and time-division duplex (TDD), as well as a wide range of system bandwidths in order to operate in a large number of different spectrum allocations. Throughout this specification, unless

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otherwise noted, the size of various fields in the time domain is expressed as a number of time units T_s=1/ (15000 x 2048) seconds. Downlink and uplink transmissions are organized into radio frames with T_f=307200xT_s=10 ms duration. Two radio frame structures are supported and FDD type is adopted in this paper.Frame structure type 1 is applicable to both full duplex and half duplex FDD. Each radio frame is T_f =307200xT_s=10 ms long and consists of 20 slots of length T_{slot}=15360xT_s=0.5 ms, numbered from 0 to 19. A subframe is defined as two consecutive slots where subframe i consists of slots 2i and 2i+1.

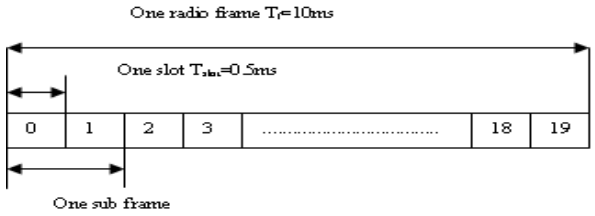

Figure 1 Frame Structure for FDD

The transmitted signal in each slot is described by a resource grid of subcarriers and OFDM symbols. The resource grid structure is illustrated in Figure 2. The quantity N_{RB}^{DL} depends on the downlink transmission bandwidth configured in the cell and shall full fill which is given in (1).

$$N_{RB}^{min,DL} \le N_{RB}^{DL} \le N_{RB}^{max,DL} \quad \text{..... (1)}$$

Where $N_{RB}^{min,DL} = 6$ and $N_{RB}^{max,DL} = 110$ are the smallest and largest downlink bandwidths, respectively, supported by the current version of this specification [1]. The number of OFDM symbols in a slot depends on the cyclic prefix length and subcarrier spacing configured. In case of multi-antenna transmission, there is one resource grid defined per antenna port. An antenna port is defined by its associated reference signal. The set of antenna ports supported depends on the reference signal configuration in the cell.Cell-specific reference signals support a configuration of one, or two antenna ports and the antenna port number shall fulfil 0 or 0 and 1 respectively. MBSFN reference signals are transmitted on antenna port 3.Each element in the resource grid for antenna port P is called a resource element and is uniquely identified by the index pair (*k,l*) in a slot where $k = 0,..., N_{RB}^{DL} N_{sc}^{RB} - 1$ and $l = 0,..., N_{symb}^{DL} - 1$ are the indices in the frequency and time domains, respectively. Resource blocks are used to describe the mapping of certain physical channels to resource elements. A physical resource block is defined as consecutive OFDM symbols in the time domain and consecutive subcarriers in the frequency domain. A physical resource block thus consists of product of the above two resource elements, corresponding to one slot in the time domain and 180 kHz in the frequency domain. Resource element groups are used for defining the mapping of control channels to resource elements. A resource-element group is represented by the index pair (*k',l'*) of the resource element with the lowest index *k* in the group with all resource elements in the group having the same value of *l*. The set of resource elements (*k,l*) in a resource-element group depends on the number of cell-specific reference signals configured. Mapping of a symbol-quadruplet <z(i), z(i+1), z(i+2), z(i+3)> onto a resource-element group represented by resource-element *(k',l')* is defined such that elements *z(i)* are mapped to resource elements *(k,l)* of the resource-element group not used for cell-specific reference signals in increasing order of *i* and *k*.

This paper is organized as follows: Section 2 discusses about the LTE Physical downlink channels and their functions. Section 3 describes the system model of transmitter and receiver for the Physical downlink channels based on 3GPP specifications. Section 4 discusses the proposed architecture for the SISO, MISO and MIMO transmitters and receivers. Section 5 gives the

simulated and implemented results for the proposed system of transmitter and receiver. Finally this paper is concluded with section 6.

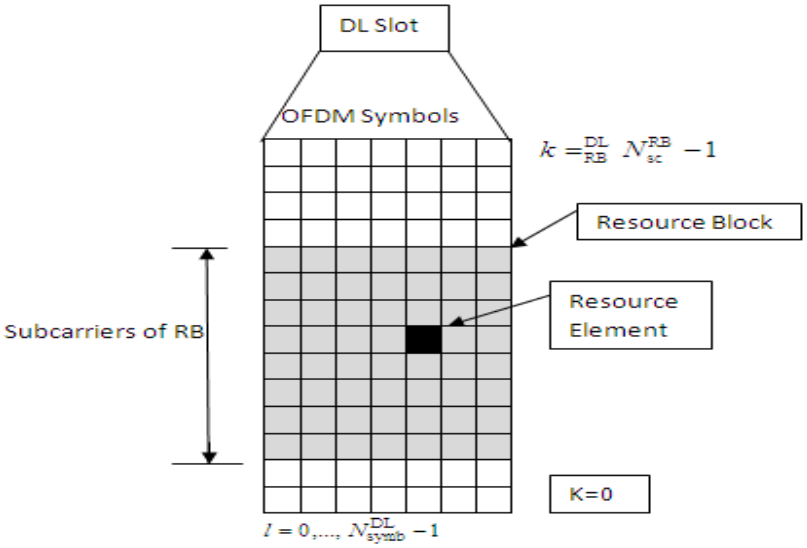

Figure 2 Downlink Resource Grid of LTE

2. LTE PHYSICAL DOWNLINK CHANNELS

The Physical Downlink Shared Channel (PDSCH) is used to send common user data and control information such as paging messages to all mobile devices operating within its coverage area. The user data is carried on the Physical Downlink Shared Channel. The PDSCH is utilized basically for data and multimedia transport. It is designed for very high data rates. Modulation schemes in PDSCH include QPSK, 16QAM and 64QAM. The PDSCH is the main data bearing channel which is allocated to users on a dynamic and opportunistic basis. In typical cellular systems the basic system information which allows the other channels in the cell to be configured and operated is carried by a Broadcast Channel. The Physical broadcast channel (PBCH) in LTE is Physical Broadcast Channel. This data are classified into two categories such as Master Information Block and System Information Block. PBCH is used to carry the system information to all mobile devices. The PBCH is transmitted using Space Frequency Block Code (SFBC), a form of transmit diversity, in case of multiple antennas thereby allowing for greater coverage. The PBCH is designed to be detectable without prior knowledge of system bandwidth and to be accessible at the cell edge.

Physical Multicast Channel (PMCH) is used for the multimedia data transport. Multimedia Broadcast and Multicast Services (MBMS) enables a set of eNBs to transfer information simultaneously for a given duration. This transmission is known as Multicast/Broadcast over a Single Frequency Network (MBFSN). Multimedia Broadcast Multicast Services (MBMS) are performed either in a single cell or a multi cell. Transmission of PDSCH and PMCH in the same subframe is not possible.The Physical Downlink Control Channel (PDCCH) is the most important control channel. The Physical Downlink Control Channel carries downlink control information, including downlink scheduling assignments, uplink scheduling grants and uplink power control commands. PDCCH carries the downlink resource allocation related to the Physical Downlink Shared Channel (PDSCH) which is a transport channel. The control information carried by PDCCH is known as Downlink Control Information (DCI) which is transmitted as an aggregation of Control Channel Elements (CCEs).

CCEs consists of Resource Element Groups (REGs) each containing four Resource Elements (REs) with a RE carrying two bits. PDCCH carries information about the Resource Block (RB) allocation, modulation, coding scheme and power control information. PDCCH occupies the first 1, 2, 3 OFDM symbols of a subframe. A cyclic redundancy check (CRC) bits are appended to the DCI for error detection

The Physical Control Format Indicator Channel (PCFICH) carries the information of number of OFDM symbols used by the PDCCH to carry the scheduling assignments and other control information. The information carried by the PCFICH is called as Control Format Indicator (CFI) and is located in the first OFDM symbol of each subframe. The CFI can take the values of 1, 2, 3 and 4 (Reserved) and are represented using two bits [2].The Physical Hybrid Indicator Channel (PHICH) is the hybrid indicator channel indicates acknowledgement for the uplink channel PUSCH. The acknowledgement may be positive (ACK) or negative (NACK) depending upon whether the transmitted data is correctly received or not. If NACK is received then data should be retransmitted. Multiple PHICHs are mapped to the same set of resource elements (REs). This set of REs constitutes a PHICH group. The PHICHs within a PHICH group are separated through different orthogonal sequences. Each PHICH group is mapped to RE groups that have not already been assigned to the PCFICH.A PHICH group is not dedicated to a single mobile, instead it is shared amongst eight mobiles, by assigning each mobile a different orthogonal sequence index. Together the PHICH group number and orthogonal sequence index are known as a PHICH resource.

3. SYSTEM MODEL

In LTE, the data which is given to the transmitter should experience the following channel processing steps. Figure 3 shows the channel processing steps of transmitter. Figure 4 shows the channel processing steps of receiver.

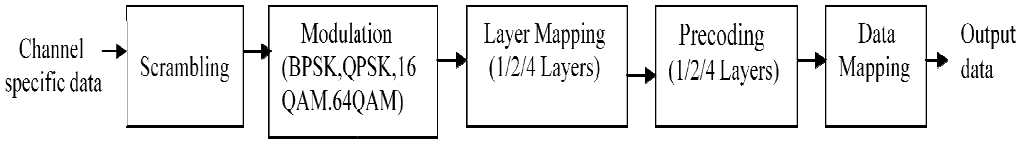

Figure 3 General Modules for Transmitter

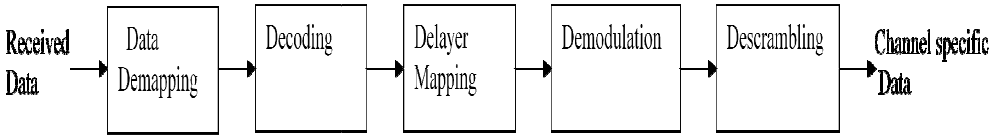

Figure 4 General Modules for Receiver

3.1 CHANNEL PROCESSING STEPS OF TRANSMITTER

3.1.1 Scrambling

The bit by bit code word is bit wise EX-OR ed with a cell specific scrambling sequence, which is a pseudo random sequence generated using a length 31 gold sequence generator. The cell specific sequence is used for the purpose of inter-cell interference rejection. The data which are to be transmitted are passed through this module initially [3]. It is the process of making the code as an unintelligible to the intruder. The scrambling is performed using (2)

$$\tilde{b}^{q}(i) = b^{q}(i) + c(i) \quad \text{... (2)}$$

Where q represents the codeword, c is the gold sequence used, *b* is the encoded sequence. The gold sequence is generated using the formulae of (3), (4) and (5)

$$c(n) = \left(x_1(n+N_c) + x_2(n+N_c)\right) \bmod 2 \quad \text{... (3)}$$

$$x_1(n+31) = \left(x_1(n+3). + x_1(n)\right) \bmod 2 \quad \text{... (4)}$$

$$x_2(n+31) = \begin{pmatrix} x_2(n+3). + x_2(n+2) \\ + x_2(n+1) + x_2(n) \end{pmatrix} \bmod 2 \quad \text{... (5)}$$

where the first m-sequence shall be initialized with $x_1(0) = 1, x_1(n) = 0, n = 1,2,...,30$. The initialization of the second m-sequence is denoted by $c_{\text{init}} = \sum_{i=0}^{30} x_2(i) \cdot 2^i$ with the value depending on the application of the sequence. In 4, $x_2(n)$ is varying for every channel.

Expressions (6),(7) and (8) are used to generate x2(n) for PDSCH, PBCH and PMCH respectively and the golden sequence $c_{(i)}$ is initialised for the channels PDCCH, PCFICH and PHICH by (9), (10) and (11) [6].

$$x_2(i) = n_{RNTI} \,.\, 2^{14} + q.2^{13} + \left\lfloor \frac{ns}{2} \right\rfloor .2^9 + N_{ID}^{cell} \quad for\ PDSCH \quad \text{... (6)}$$

$$x_2(i) = N_{ID}^{cell} \quad for\ PBCH \quad \text{... (7)}$$

$$x_2(i) = \left\lfloor \frac{ns}{2} \right\rfloor .2^9 + N_{ID}^{MBSFN} \quad for\ PMCH \quad \text{... (8)}$$

$$c_{init} = \left\lfloor \frac{n_s}{2} \right\rfloor .2^9 + N_{ID}^{cell} \quad for\ PDCCH \quad \text{... (9)}$$

$$c_{init} = \left(\left\lfloor \frac{n_s}{2} \right\rfloor + 1\right) \cdot \left(2N_{ID}^{cell} + 1\right) \cdot 2^9 + N_{ID}^{cell} \quad for\ PCFICH \quad \text{... (10)}$$

$$c_{init} = \left(\left\lfloor \frac{n_s}{2} \right\rfloor + 1\right) \cdot \left(2N_{ID}^{cell} + 1\right).2^9 \quad for\ PHICH \quad \text{... (11)}$$

Where n_{RNTI} is the Radio Network Temporary Identifier, q refers to the codeword number, ns is slot number and N_{ID}^{cell} is the physical layer cell identity. N_{ID}^{MBSFN} is the MBSFN Area Identity for PMCH.

3.1.2 Modulation

In general LTE follows four different types of modulation techniques such as BPSK, QPSK, 16 QAM and 64 QAM. Channels and their corresponding modulation techniques are shown in Table 1.

Table 1 Channel and Modulations

Channels	**Type of Modulation**
PBCH,PCFICH,PDCCH	QPSK
PDSCH	QPSK, 16 QAM, 64 QAM
PMCH	QPSK, 16 QAM, 64 QAM
PHICH	BPSK

The scrambled sequence is then modulated to create a block of modulated symbols. In QPSK modulation pairs of bits are mapped to complex valued modulation symbols I+ jQ, as shown in Table 2 and hence the all the bits are converted to 16 complex modulated symbols. The outputs are represented by 16 bit numbers. Similarly the distributed arithmetic processing is applied for 16QAM, 64QAM [1].

Table 2 QPSK Modulation

b(i),b(i+1)	I	Q
00	$1/\sqrt{2}$	$1/\sqrt{2}$
01	$1/\sqrt{2}$	$-1/\sqrt{2}$
10	$-1/\sqrt{2}$	$1/\sqrt{2}$
11	$-1/\sqrt{2}$	$-1/\sqrt{2}$

3.1.3 Layer Mapping

The modulated symbols are then layer mapped to one or more layers depending upon the number of antenna ports selected .The complex modulated input symbols $d^{(0)}(i)$ are mapped to layers $x^{(0)}(i)$, $x^{(1)}(i)$,... $x^{(v-1)}(i)$. The input symbols are mapped to layers according to the Table 3[1]

Table 3 Layer Mapping to different layers

Number of layers	Layer mapping i=0,1,..., M^{layer}_{symb}-1
1	$X^{(0)}(i)=d^{(0)}(i)$
2	$X^{(0)}(i)=d^{(0)}(2i)$ $M^{layer}_{symb}=M^{(0)}_{symb}/2$ $X^{(1)}(i)=d^{(0)}(2i+1)$
4	$X^{(0)}(i)=d^{(0)}(4i)$ $X^{(1)}(i)=d^{(0)}(4i+1)$ $X^{(2)}(i)=d^{(0)}(4i+2)$ $M^{layer}_{symb}=M^{(0)}_{symb}/4$ $X^{(3)}(i)=d^{(0)}(4i+3)$

3.1.4 Precoding

The precoder takes a block from the layer mapper $x^{(0)}(i)$, $x^{(1)}(i)$,... $x^{(v-1)}(i)$, and generates a sequence for each antenna port, $y^{(p)}(i)$, p is the transmit antenna port number and is {0},{0,1} or {0,1,2,3}[4]. For transmission over a single antenna port processing is carried out by (12).

$$y^{(p)}(i) = x^{(0)}(i) \qquad \ldots.(12)$$

Precoding for transmit diversity is available on two or four antenna ports. In two antenna port precoding, an Alamouti scheme is used for precoding. This precoding procedure for two antenna case is defined by (13)

$$\begin{bmatrix} y^{(0)}(2i) \\ y^{(1)}(2i) \\ y^{(0)}(2i+1) \\ y^{(1)}(2i+1) \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 0 & j & 0 \\ 0 & -1 & 0 & j \\ 0 & 1 & 0 & j \\ 1 & 0 & -j & 0 \end{bmatrix} \begin{bmatrix} \mathrm{Re}\left(x^{(0)}(i)\right) \\ \mathrm{Re}\left(x^{(1)}(i)\right) \\ \mathrm{Im}\left(x^{(0)}(i)\right) \\ \mathrm{Im}\left(x^{(1)}(i)\right) \end{bmatrix} \qquad \ldots (13)$$

For $i = 0,1,...,M_{\text{symb}}^{\text{layer}} - 1$ with $M_{\text{symb}}^{\text{ap}} = 2M_{\text{symb}}^{\text{layer}}$.During transmission on four antenna ports, $p \in \{0,1,2,3\}$, the output $y(i) = \left[y^{(0)}(i) \quad y^{(1)}(i) \quad y^{(2)}(i) \quad y^{(3)}(i)\right]^T$, $i = 0,1,...,M_{\text{symb}}^{\text{ap}} - 1$ of the precoding operation is defined by (14)

$$\begin{bmatrix} y^{(0)}(4i) \\ y^{(1)}(4i) \\ y^{(2)}(4i) \\ y^{(3)}(4i) \\ y^{(0)}(4i+1) \\ y^{(1)}(4i+1) \\ y^{(2)}(4i+1) \\ y^{(3)}(4i+1) \\ y^{(0)}(4i+2) \\ y^{(1)}(4i+2) \\ y^{(2)}(4i+2) \\ y^{(3)}(4i+2) \\ y^{(0)}(4i+3) \\ y^{(1)}(4i+3) \\ y^{(2)}(4i+3) \\ y^{(3)}(4i+3) \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 0 & 0 & 0 & j & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 & j & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & j & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & -j & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & j & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 0 & 0 & j \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & j \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & -j & 0 \end{bmatrix} \begin{bmatrix} \text{Re}\left(x^{(0)}(i)\right) \\ \text{Re}\left(x^{(1)}(i)\right) \\ \text{Re}\left(x^{(2)}(i)\right) \\ \text{Re}\left(x^{(3)}(i)\right) \\ \text{Im}\left(x^{(0)}(i)\right) \\ \text{Im}\left(x^{(1)}(i)\right) \\ \text{Im}\left(x^{(2)}(i)\right) \\ \text{Im}\left(x^{(3)}(i)\right) \end{bmatrix} \quad \text{..... (14)}$$

For $i = 0,1,...,M_{\text{symb}}^{\text{layer}} - 1$ with $M_{\text{symb}}^{\text{ap}} = \begin{cases} 4M_{\text{symb}}^{\text{layer}} & \text{if } M_{\text{symb}}^{(0)} \bmod 4 = 0 \\ \left(4M_{\text{symb}}^{\text{layer}}\right) - 2 & \text{if } M_{\text{symb}}^{(0)} \bmod 4 \neq 0 \end{cases}$.

3.1.5 Mapping to Resource Elements

The data channels modulated symbols are mapped to the resource element groups (REG), and data is mapped only in the first OFDM symbol of each subframe and are transmitted through the channel. To do this module the designer has know the row, column and slot value.

3.2 CHANNEL PROCESSING STEPS OF RECEIVER

3.2.1 Demapping From Resource Elements

While data is received on the antenna ports, the block of complex-valued symbols $y^{(p)}(0),..., y^{(p)}(M_{\text{symb}}^{\text{ap}} - 1)$ shall be demapped in sequence starting with $y^{(p)}(0)$ from resource elements (k,l).

3.2.2 Decoding

The decoder takes as input a block of vectors $y(i) = \left[.. \quad y^{(p)}(i) \quad ...\right]^T$, $i = 0,1,...,M_{\text{symb}}^{\text{ap}} - 1$ demapped from resources on each of the antenna ports, where $y^{(p)}(i)$ represents the signal from antenna port p and generates a block of vectors $x(i) = \left[x^{(0)}(i) \quad ... \quad x^{(\upsilon-1)}(i)\right]^T$, $i = 0,1,...,M_{\text{symb}}^{\text{layer}} - 1$ for the delayer mapping. For reception on a single antenna port, decoding is defined by (15). Similarly for reception on two antenna ports, $p \in \{0,1\}$, the output of the decoding operation is defined by (16).

$$x^{(0)}(i) = y^{(p)}(i) \quad \text{... (15)}$$

$$\begin{bmatrix} \mathrm{Re}(x^{(0)}(i)) \\ \mathrm{Re}(x^{(1)}(i)) \\ \mathrm{Im}(x^{(0)}(i)) \\ \mathrm{Im}(x^{(1)}(i)) \end{bmatrix} = \sqrt{2} \begin{bmatrix} 1 & 0 & 0 & 1 \\ 0 & -1 & 1 & 0 \\ j & 0 & 0 & -j \\ 0 & j & j & 0 \end{bmatrix} \begin{bmatrix} y^{(0)}(2i) \\ y^{(1)}(2i) \\ y^{(0)}(2i+1) \\ y^{(1)}(2i+1) \end{bmatrix} \quad ...(16)$$

3.2.3 Delayer Mapping

The complex-valued symbols for each of the code words to be received are demapped from one or several layers [5]. Complex-valued symbols $d^{(q)}(0),...,d^{(q)}(M^{(q)}_{\text{symb}}-1)$ for codeword q shall be demapped from the layers $x(i)=\left[x^{(0)}(i) \quad ... \quad x^{(\upsilon-1)}(i)\right]^T$, $i=0,1,...,M^{\text{layer}}_{\text{symb}}-1$ where υ is the number of layers and $M^{\text{layer}}_{\text{symb}}$ is the number of symbols per layer. Delayer mapping for single antenna is defined by (17). Similarly for two antenna port, delayer mapping is defined by (18)

$d^{(0)}(i)=x^{(0)}(i)$ with $M^{0}_{\text{symb}}=M^{\text{layer}}_{\text{symb}}$ ..... (17)

$d^{(0)}(2i)=x^{(0)}(i)$
$d^{(0)}(2i+1)=x^{(1)}(i)$ with $M^{0}_{\text{symb}}=2M^{\text{layer}}_{\text{symb}}$ ..... (18)

3.2.4 Demodulation

The complex-valued symbols $d^{(q)}(0),...,d^{(q)}(M^{(q)}_{\text{symb}}-1)$ of code word q, shall be demodulated using a demodulation scheme which is reverse of transmitter, resulting in a block of bits $\tilde{b}^{(q)}(0),...,\tilde{b}^{(q)}(M^{(q)}_{\text{bit}}-1)$

3.2.5 Descrambling

The demodulated symbols in a code word q, after descrambling results in the block of bits $b^{(q)}(0),...,b^{(q)}(M^{(q)}_{\text{bit}}-1)$, where $M^{(q)}_{\text{bit}}$ is the number of bits in code word q received on each control channels in one sub frame. The descrambling is defined by (19).

$$b^{(q)}(i) = \left(\tilde{b}^{(q)}(i)+c^{(q)}(i)\right) mod 2 \quad ..... (19)$$

where $c^{(q)}(i)$ is the generated pseudo random Gold sequence. The descrambling sequence is initialized with same values as that of the transmitter at start of each subframe.

4. NOVEL ARCHITECTURE OF PHYSICAL DOWNLINK CHANNELS FOR LTE

4.1 TRANSMITTER ARCHITECTURE

The transmitter side of the architecture consists of Scrambling, Modulation, Layer Mapping, Precoding and Mapping to the Resource Elements as shown in figure 6.

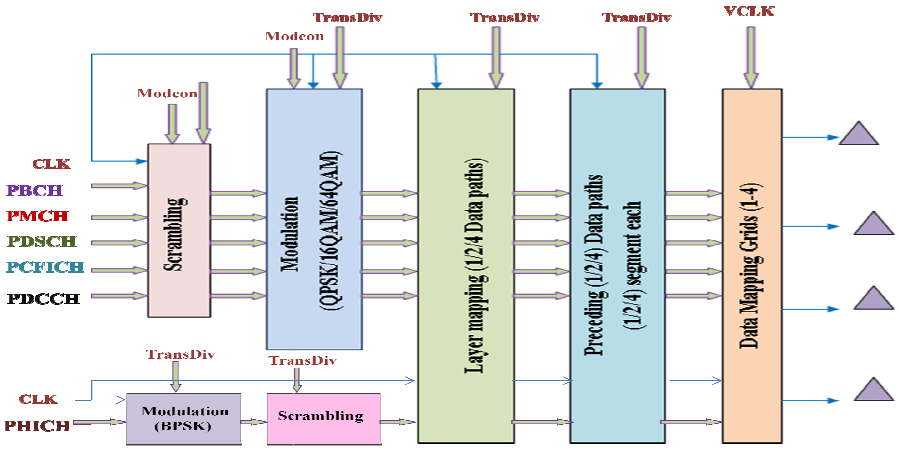

Figure 6 Parallel Processing Architecture of Transmitter for downlink Channels in LTE

Scrambling is common for all the six channels. For this the 32 bit input codeword is XORed with the 32 bit Gold sequence. Based on the type of modulation and transmitter diversity, the number of scrambling bits to be generated varies. The following Table 4 depicts the number of scrambling bits generated and so the number of Hardware lines. The PBCH, PCFICH and PDCCH channels employ QPSK modulation. For this, the maximum number of hardware lines is 8. The PDSCH and PMCH employ QPSK, 16QAM, 64QAM modulations. The maximum number of hardware lines required is 24 for PDSCH. Since PMCH is transmitted only on 4th antenna, the maximum number of hardware lines required is 8.

Table 4 Number of Scrambling bits generated

Channel	Type of Modulation	Layers	No. of Scrambling bits to be generated
PBCH	QPSK	1/2/4	2/4/8
PDSCH	QPSK 16 QAM 64 QAM	1/2/4	2/4/8 4/8/16 6/12/24
PMCH	QPSK/16QAM/64 QAM	1	2/4/6
PCFICH	QPSK	1/2/4	2/4/8
PDCCH	QPSK	1/2/4	2/4/8
PHICH	BPSK	1/2/4	1

PHICH uses BPSK modulation. In modulation process, a pair of scrambled bit is converted to corresponding complex-valued modulated output.Layer mapping involves mapping of the modulated symbols to different layers. For SISO the modulated bits get transmitted as such, no mapping is needed. When two antenna ports are used, modulator output is layer mapped as a block of vector in two layers. When four antenna ports are used, modulator output is layer mapped as a block of vector in four layers. Precoding is the process of creating vectors for layer mapped data. Similar to layer mapping, precoding can also be performed on single, two or four layers. Precoded data are mapped to the LTE grid structure.

4.2 RECEIVER ARCHITECTURE

The receiver side of the architecture consists of Demapping from the Resource Elements, Decoding and Detection, Delayer Mapping and Descrambling as shown by the Figure 7. The receiver architecture is designed with two receiving antennas. When the transmitter diversity is SISO (1x1) or MISO (2x1 and 4x1) antenna 1 is enabled to receive. Similarly when MIMO (2x2 and 4x2) case occurs both the antennas are enabled to receive. In the receiver side, the first step is to demap the data from the grids.

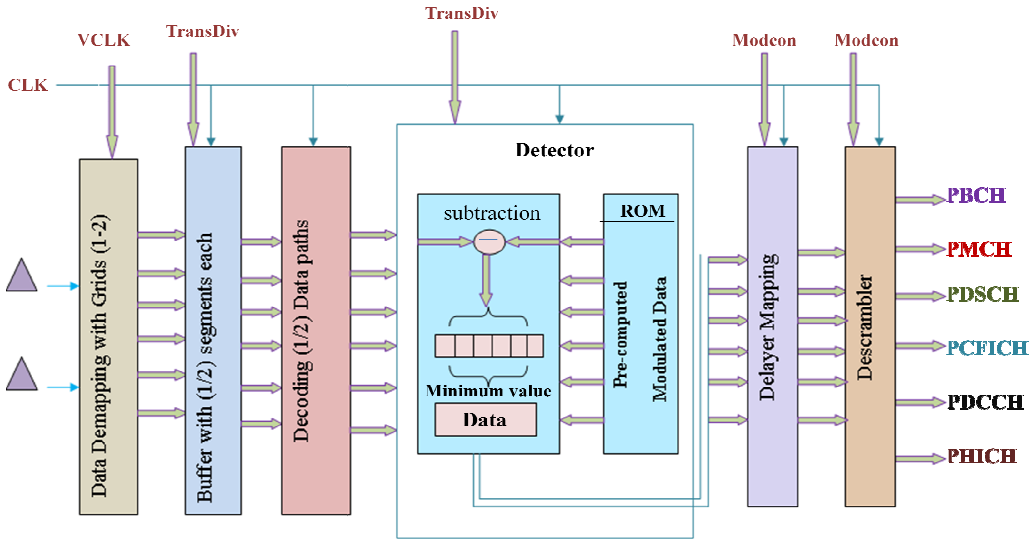

Figure 7 Parallel Processing Architecture of Receiver for downlink Channels in LTE

After demapping the data from the grid, decoding is performed by the receiver. The output of the demapping module is given to a buffer in order to store 16 bit data for the SISO (1x1), MISO (2x1) and MISO (4x1) .For MIMO(2x2) and MIMO(4x2) the buffer will store two segments of data in two layers. The data from the buffer module is given to the decoding. Based on the transmitter diversity the 16 bit data is stored for further processing. Detection process is performed by comparing the decoded results with the predefined modulation values and generating the resultant bits corresponding to the modulation scheme. The resultant bits are 2 for QPSK modulation, 4 for 16 QAM and 6 for 64 QAM modulations respectively. Demodulated and detected bits are concatenated to form a single layer in delayer mapping module. The descrambling is performed by XORing the detected bits with the same Gold sequence used in the transmitter and produces the original control and data messages.

5. RESULTS AND DISCUSSIONS

5.1 Simulation output for SISO transmitter

The Simulation output for the SISO transmitter for PDCCH channel is shown in Figure 8. The variables clk, rst, td, and 'mod_pdcch' are the inputs given. The PDCCH employs QPSK modulation. So based on the 'mod_pdsch' and td, the number of scrambling bits generated and the number of hardware lines varies. For QPSK 'scr_pdcch1' and 'scr_pdcch2' are made to generate the output thus giving 2 input bits to the modulation mapper to produce a single segment at a single clock cycle. Variable 'canc_pdcch' is the clock generated from the scrambling module. Scrambling output is directly given as the input to modulation module. Variable 'modpdcchpara1' is the modulated output of the modulation module which is given to the layer mapping module. The layer mapped output is given by 'layer1pdcch'. Layer mapped output is given to the

precoding module. The output of the precoding module is one segment represented as 'prelayer1_pdcch'. The final transmitted output through the antenna is given by 'transmit_0'.This explanation suits well for all the other channels.

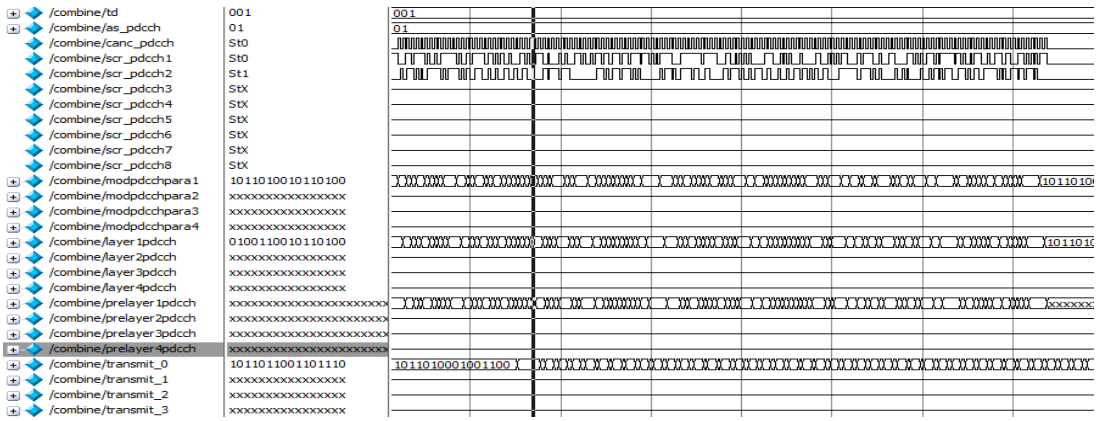

Figure 8 Simulation result for SISO (1X1) PDCCH

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5.2 Simulation output for MISO (2x1) transmitter

The simulation result for the transmitter using MISO (2x1) concept for PCFICH channel is shown in Figure 9. The variables clk, rst, td, and 'mod_pcfich' are the inputs given. For MISO (2x1) the process is similar to SISO (1x1).But in layer mapping same modulated data is layer mapped into two layers. The layer mapped output is given by 'layer1pcfich' and 'layer2pcfich'. Layer mapped output is given to the precoding module; the output is 'prelayer1_pcfich' and 'prelayer2_pcfich', which consists of two segments in two layers. The final transmitted output through the antenna is given by 'transmit_0' and 'transmit_1'. The above explained procedure is similar for all the other channels.

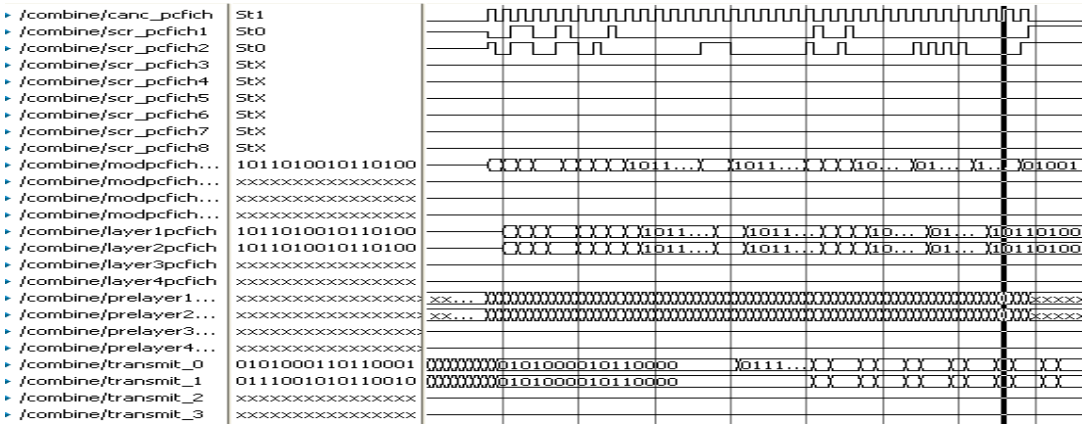

Figure 9 Simulation result for MISO (2X1) PCFICH

5.3 Simulation output for MISO (4x1) transmitter

The simulation result of MISO (4x1) transmitter for PMCH channel is shown in Figure 10. The variables clk, rst, td, and 'mod_pmch' are the inputs given. For MISO (4x1) the process is similar to SISO (1x1). For PMCH channel the modulated data is layer mapped into a single layer. The layer mapped output is given by 'singlepmch'. Layer mapped output is given to the precoding module, the output is 'single_prepmch'. The final transmitted output through the antenna is given by 'transmit_3'.

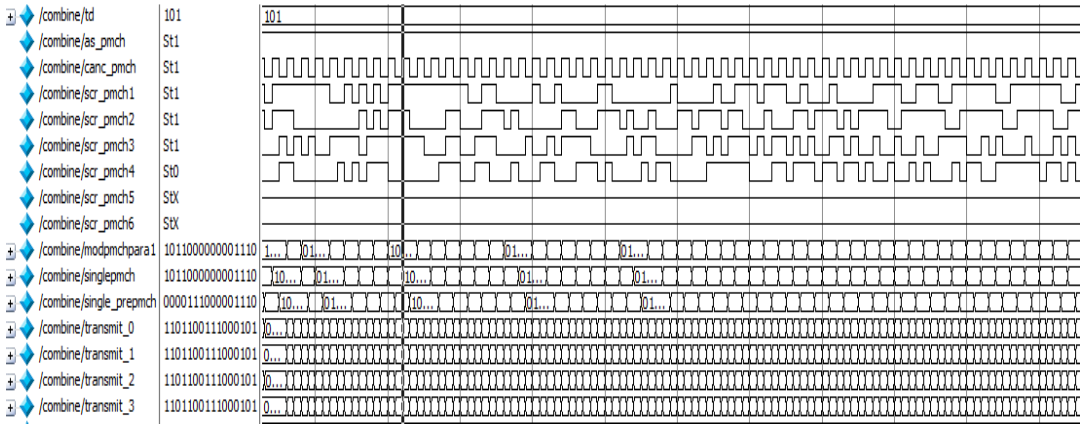

Figure 10 Simulation result for MISO (4X1) PMCH

5.4 Simulation output for MIMO (2x2) transmitter

The simulation result for the MIMO (2x2) transmitter for channel PDSCH is shown in Figure 11. For MIMO (2x2) the number of scrambling bits to be generated is 4/8/12bits for QPSK/16QAM/64QAM modulations. For 64QAM, the scrambler module outputs are 'scr_pdsch1','scr_pdsch2','scr_pdsch3','scr_pdsch4','scr_pdsch5','scr_pdsch6', 'scr_pdsch7', 'scr_pdsch8','scr_pdsch9','scr_pdsch10', 'scr_pdsch11','scr_pdsch12'. Variable 'canc_pdsch' is the clock generated from the scrambling module. Scrambling output is directly given as the input to modulation module. Variable 'modpdschpara1'and 'modpdschpara2' are the modulated output of the modulation module which shows two different data to be given directly to the layer mapping module. The layer mapped output is given by 'layer1pdsch' and 'layer2pdsch'. Layer mapped output is given to the precoding module; the output is 'prelayer1_pdsch' and 'prelayer2_pdsch', which is of two different segments in two layers. The final transmitted output through the antenna is given by 'transmit_0' and 'transmit_1'.These explanations are similar for PBCH, PCFICH and PDCCH channels also.

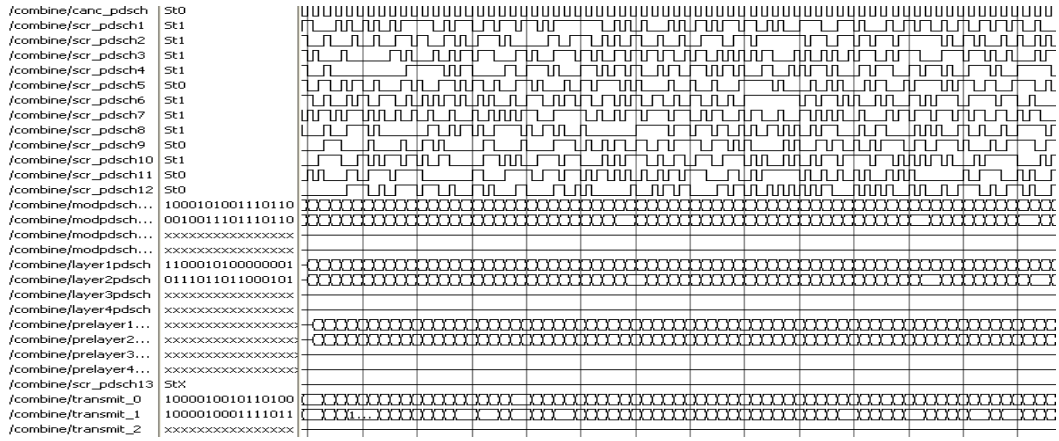

Figure 11 Simulation result for MIMO (2X1) PDSCH

5.5 Simulation output for MIMO (4x2) transmitter

The simulation result for the MIMO transmitter of PBCH channel is shown in Figure 12.For QPSK, the scrambler module outputs are 'scr_pbch1', 'scr_pbch2', 'scr_pbch3', 'scr_pbch4', 'scr_pbch5', 'scr_pbch4', 'scr_pbch7', 'scr_pbch8'.Variable 'canc_pbch' is the clock generated from the scrambling module. Scrambling output is directly given as the input to modulation module. Variable 'modpbchpara1', 'modpbchpara2', 'modpbchpara3' and 'modpbchpara4' are

the modulated output of the modulation module which shows four different data to be given directly to the layer mapping module. The layer mapped output is given by ‘layer1pbch’, ‘layer2pbch’, ‘layer3pbch’ and ‘layer4pbch’. Layer mapped output is given to the precoding module, the output is ‘prelayer1_pbch’, ‘prelayer2_pbch’, ‘prelayer3_pbch’ and ‘prelayer4_pbch’, which is of four segments in four layers. The final transmitted output through the antenna is given by ‘transmit_0’, ‘transmit_1’, ‘transmit_2’ and ‘transmit_3’.

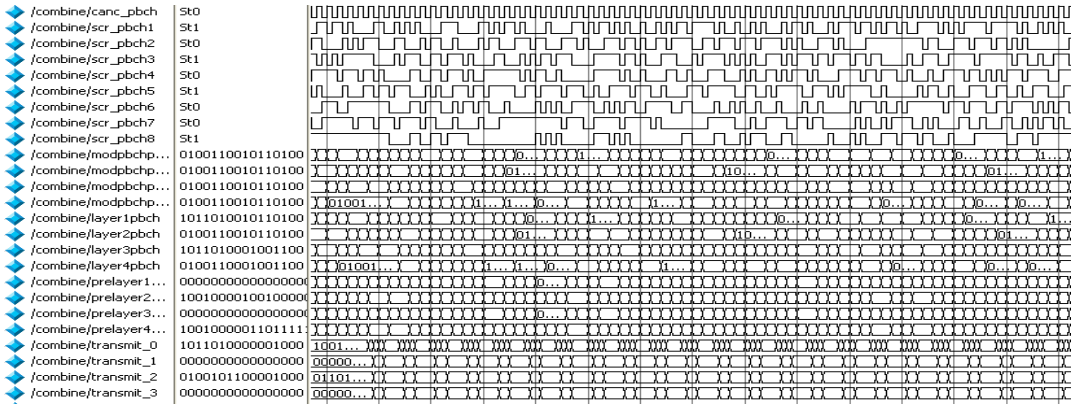

Figure 12 Simulation result for MIMO (4x2) PBCH

5.6 Simulation output for SISO (1x1), MISO (2x1) and MISO (4x1) Receiver

The Simulation output for the SISO (1x1), MISO (2x1) and MISO (4x1) receiver for PBCH channel is shown in Figure 13. The variables clk, rst, td, are the inputs given.The variables ‘as_pdsch’, ‘as_pbch’, ‘as_pdcch’, ‘as_pcfich’ and ‘as_phich’ are the antenna selection variables which has value 01 indicating single receiver antenna. The variable ‘prelayer1pbch’ is the output of the data demapping module, which exclusively demaps the received data from antenna. The variable ‘singlepbch’ is the decoded value for the PBCH channel. In detection module the variable ‘singlepbchqpsk’ is the output, which is of two bits for the PBCH channel. The variables ‘delayersinglepbch’ is the delayermapped value. The variables ‘descr_pbch1’ and ‘descr_pbch2’ are the variables indicating the descrambled bits for the channel PBCH. Similarly for PDCCH and PCFICH also. Since PDSCH employs QPSK, 16QAM and 64QAM modulations, the output of the detector module ‘singlepdsch_demod’ consists of 2 bits/4 bits/6 bits for QPSK/ 16QAM /64QAM modulations respectively. The variables ‘descr_pdsch1’, ‘descr_pdsch2’, ‘descr_pdsch3’, ‘descr_pdsch4’, ‘descr_pdsch5’, ‘descr_pdsch6’, are the variables indicating the descrambled bits for the channel PDSCH.

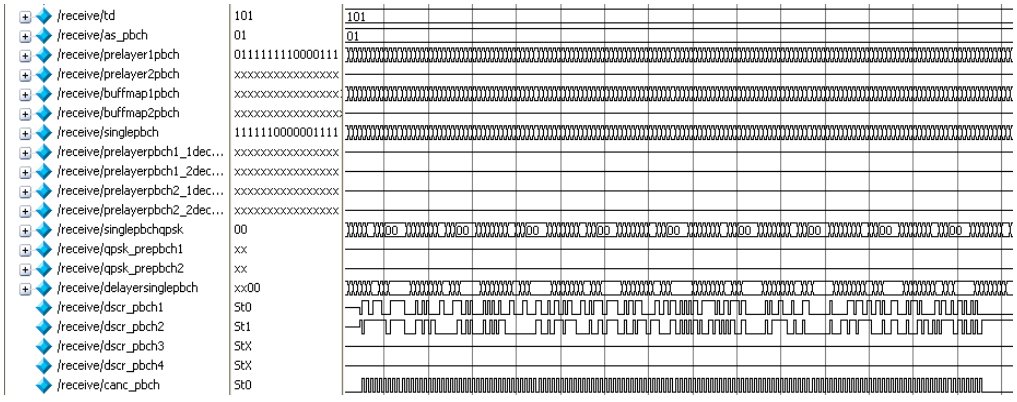

Figure 13 Simulation output for SISO (1x1), MISO (2x1) and MISO (4x1) Receiver-PBCH

5.7 Simulation output for MIMO (2x2) and MIMO (4x2)

The Simulation output for the MIMO (2x2) and MIMO (4x2) receiver for PBCH channel is shown in Figure 14.The variable 'as_pbch' is the antenna selection variable which has value 10 indicating two antenna receivers. The variables 'prelayer1pbch' and 'prelayer2pbch' are the output of the data demapping module, which exclusively demap the received data from antenna. The variables 'prelayerpbch1_1decode', 'prelayerpbch1_2decode', 'prelayerpbch2_1decode' and 'prelayerpbch2_2decode' are the decoded values for the PBCH channel. In detection module the variable 'qpsk_prepbch1' and 'qpsk_prepbch2' are the output, which is of two bits for the PBCH channel. The variables 'delayersinglepbch' is the delayermapped value. The variables 'descr_pbch1', 'descr_pbch2', 'descr_pbch3'and 'descr_pbch4' are the variables indicating the descrambled bits for the channel PBCH. Similarly for PDCCH and PCFICH also.

PDSCH employs QPSK, 16QAM and 64QAM modulations. Each of the two output variables 'twopdsch_demod1' and 'twopdsch_demod2' of the detector module consists of 2 bits/4bits/6bits for QPSK/16QAM/64QAM modulations respectively. The variables descr_pdsch1, descr_pdsch2, descr_pdsch3, descr_pdsch4, descr_pdsch5, descr_pdsch6, descr_pdsch7, descr_pdsch8, descr_pdsch9, descr_pdsch10, descr_pdsch11, descr_pdsch12, are the variables indicating the descrambled bits for the channel PDSCH shown in Figure 15.

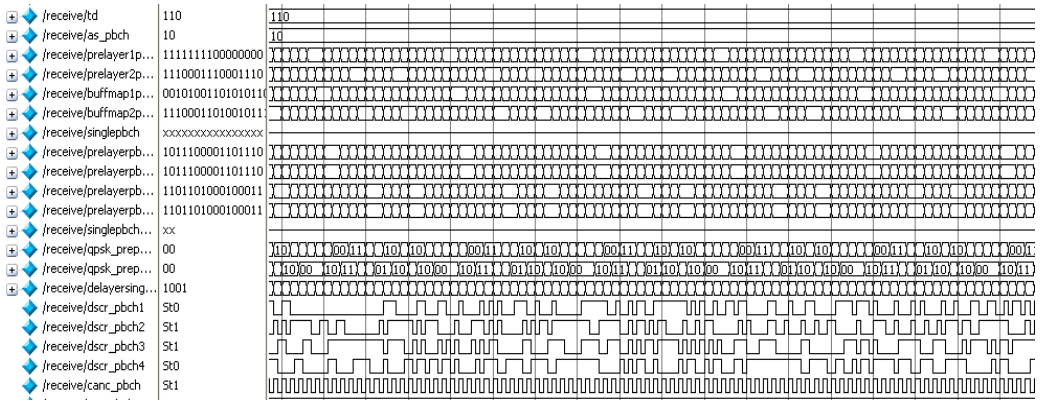

Figure 14 Simulation output for MIMO (2x2) and MIMO (4x2) Receiver –PBCH

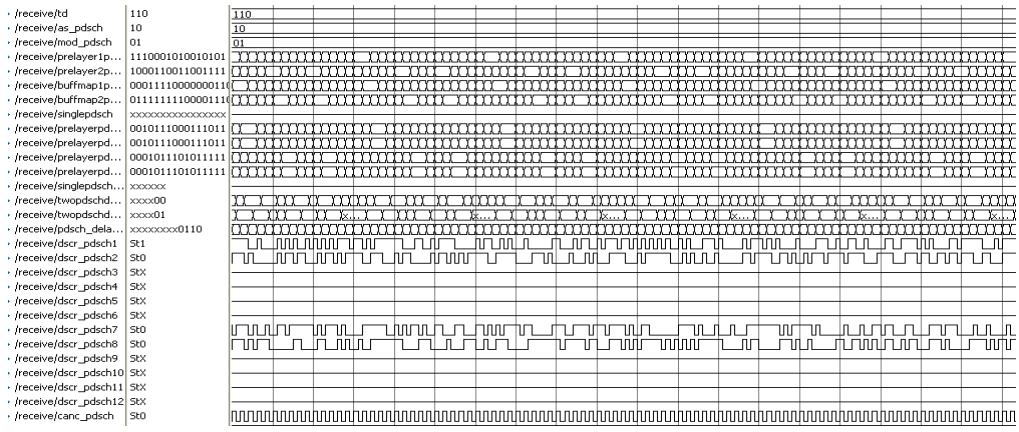

Figure 15 Simulation output for MIMO (2x2) and MIMO (4x2) Receiver - PDSCH (QPSK)

5.8 Implementation Results

Simulated programs are implemented on Plan Ahead 13.4 Virtex-5 board and the implemented results are discussed in terms of RTL Design, Power Estimation, Resource Estimation and FPGA Editor. Register-transfer-level abstraction is used in hardware description languages (HDLs) like Verilog and VHDL to create high-level representations of a circuit, from which lower-level representations and ultimately actual wiring can be derived. One of the peculiarities of the Plan Ahead tool is that it provides RTL elaboration capabilities to compile RTL source files in the project. The Figure 16 provides the RTL diagram of transmitter showing the different modules like scrambling, modulation, layer mapping, precoding and Resource element mapping. Inside various blocks we can see the Muxes, Look up tables, various interconnections and Gates. The Figure 17 provides the RTL diagram of receiver showing the different modules like descrambling, de modulation, delayer mapping, decoding and Demapping from the resource elements.

The resource estimation for the transmitter and receiver is shown in the Figure 18a and 18b. From the graphical representation it is clear that out of the total resources about 1% is used for registers, 6% for Look up tables, 10% for the slices, 15% for the IO, 21% for BUFG in transmitter side, 1% is used for registers, 25% for Look up tables, 36% for the slices, 7% for the IO, 15% for BUFG in receiver side .One of the peculiarities of the Plan Ahead software is that it performs power estimation to provide an early view of your design power distribution at the RTL level. The power estimation is a graphical representation of the total on chip power and its distribution to the device static, core dynamic, and I/O as shown in Figure 19a and 19b.The total on chip power of 1379 mw for the transmitter is distributed among I/O, core dynamic and Device static as 245mw, 459mw and 455 .The total on chip power of 1263 mw for the receiver is distributed among I/O, core dynamic and Device static as 33mw, 777mw and 454 mw. The FPGA editor shows the placing and routing in the device xc5vlx50tff1134. The utilization of the IC is shown in the Figure 20a and 20b.

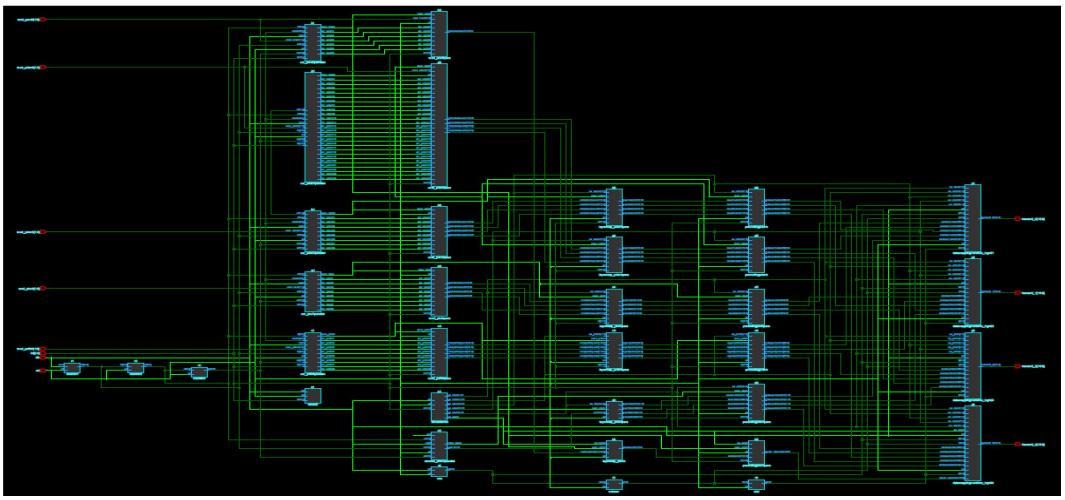

Figure 16 RTL Diagram of the Transmitter

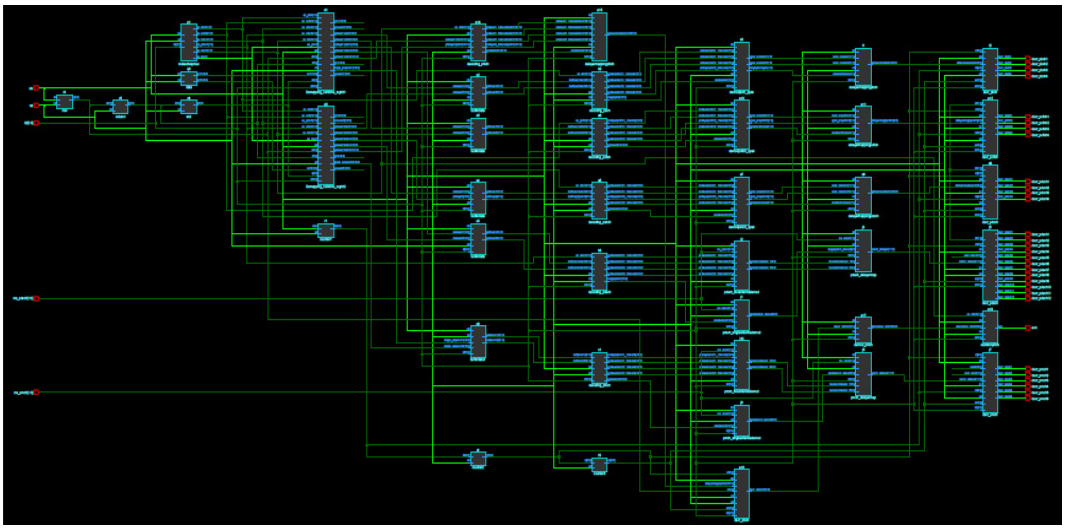

Figure 17 RTL Diagram of Receiver

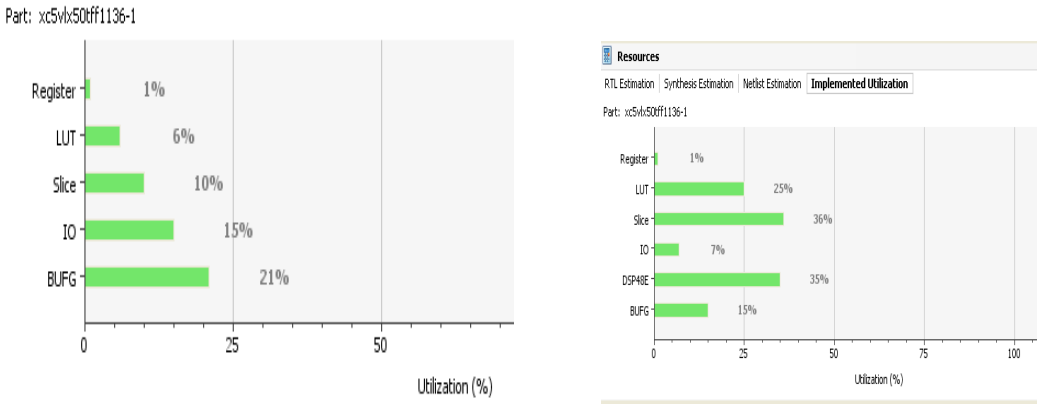

Figure 18a and 18b Resource utilization of the Transmitter and Receiver

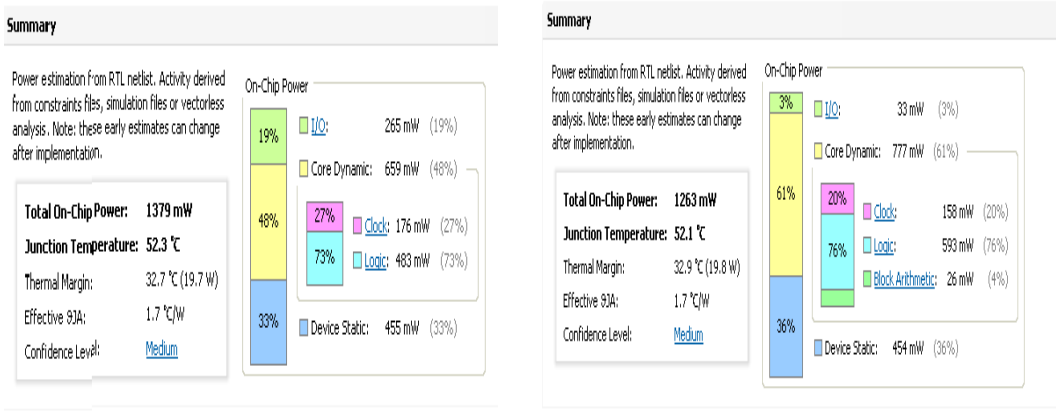

Figure 19a and 19b Power estimation of Transmitter and Receiver

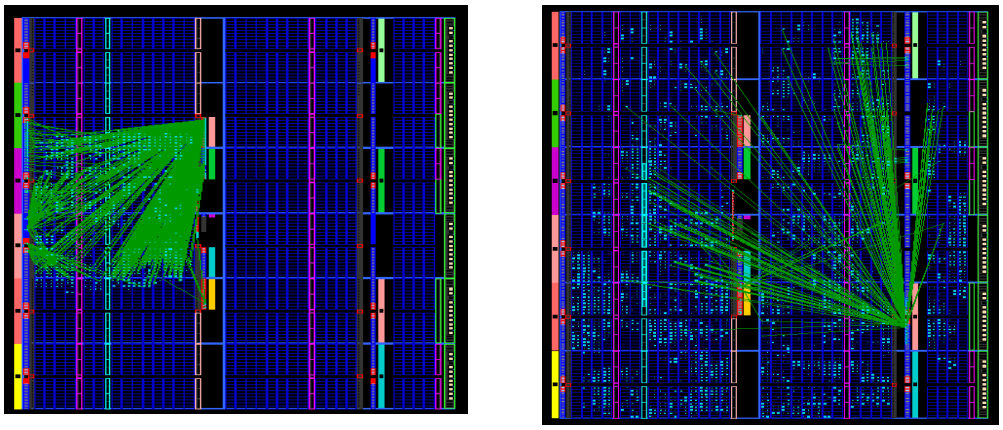

Figure 20a and 20b FPGA editor of the Transmitter and Receiver

6. CONCLUSIONS

The transmitter architecture of LTE Physical Downlink channels consists of five steps namely Scrambling, Modulation, Layer Mapping, Precoding and Mapping to Resource Elements. Initially the single codeword say 32 bits is taken and is scrambled using gold sequence. The scrambled output is modulated by any one of the modulation scheme according to the information obtained from the higher layers. The modulated stream of bits is layer mapped according to the number of antenna ports present. The layer mapped output is precoded. Then precoded output is mapped to resource elements at the respective positions of each channel leaving space for reference and synchronization signals. The receiver architecture of LTE Downlink Physical channels consists of five steps namely Demapping from Resource Elements, Decoding, Detection, Delayer mapping and Descrambling. At receiver, the data is received from the grid and the reverse process demapping, decoding, detection, delayer mapping, for respective channels and finally descrambled to get the original transmitted codeword at all channel. The implementation of the transmitter and receiver architectures of all channels are carried by Verilog HDL programming and synthesized in Plan Ahead 13.4 with Virtex-5 specification. Simulation results and implementation results (RTL design, power estimation, resource estimation and FPGA editor) for transmitter and receiver of LTE downlink channels are discussed.

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