FGMOS BASED LOW-VOLTAGE LOW-POWER HIGH OUTPUT IMPEDANCE REGULATED CASCODE CURRENT MIRROR

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ABSTRACT

Floating Gate MOS (FGMOS) transistors can be very well implemented in lieu of conventional MOSFET for design of a low-voltage, low-power current mirror. Incredible features of flexibility, controllability and tunability of FGMOS yields better results with respect to power, supply voltage and output swing. This paper presents a new current mirror designed with FGMOS which exhibit high output impedance, higher current range, very low power dissipation and higher matching accuracy. It achieves current range of up to 1500 μA, high output impedance of 1.125 TΩ, bandwidth of 4.1 MHz and dissipates power as low as 10.56 μW. The proposed design has been simulated using Cadence Design Environment in 180 nm CMOS process technology with +1.0 Volt single power supply.

KEYWORDS

Floating Gate MOSFET, Current Mirror, Regulated Cascode, Low-Voltage & Low-Power

1. INTRODUCTION

A current mirror (CM) is a circuit designed to copy a current through one active device by controlling the current in another active device of circuit, keeping the output current constant regardless of loading. The responsibilities of current mirror circuit are current amplification and to provide proper biasing to analog circuits. Due to very wide application of current mirror in low voltage low-power analog circuits, accuracy, output impedance and power consumption play key role in determining CM performance [6]. Their utilization in analog signal processing extends the advantages of low-voltage operations, derivation of resistorless topologies and electronic adjustment capability of their frequency characteristics [13].

With the increasing demand for smaller and faster products, there is an ongoing trend in fabrication process towards smaller transistors. Reducing feature size arises potential problem like power dissipation and dielectric breakdown due to high electric field across the feature. These potential problems can be compensated by reducing the voltage and hence low-voltage power supply is beneficial. In addition to this battery lifetime is crucial factor in various applications and hence low-power device is also a compulsory requirement as per current market trend. In the quest to achieve low-voltage and low-power, various techniques have evolved in due course of time and Floating Gate MOS (FGMOS) technique is one amongst them.

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FGMOS is proven technology in digital circuits but has also gained pace when it comes to its application in the area of low-voltage, low-power analog design. FGMOS is a device in which the second gate generally called floating gate is electrically isolated but capacitively coupled to input gates. A control voltage present at one of the multi-input FGMOS and facility to additional weighted inputs provides wide range of tunability to the circuit [1]. Implementation of FGMOS allows threshold voltage (V_{th}) controllability without reducing the feature size, thus operates at power supply voltage levels which are well below the intended operational limit. Also, it consumes less power than the minimum required power for a circuit designed with conventional MOSFET. Using regulated cascode configuration achieves high output impedance of the order of $g_m^2 r_{out}^3$ where g_m is device trans-conductance and r_{out} is output resistance [5], [10]-[11].

Various FGMOS based current mirror designs have been presented in [4], [7] and [8]-[9]. FGMOS based current mirror design presented in [4] and [8] suffers from higher power dissipation and lower current range. On the other hand [7] and [9] both presents FGMOS based design having better results with respect to input impedance, bandwidth and supply voltage but exhibits very low output impedance. Current mirror suggested in [12] has ultra low power dissipation but at a very low biasing current of the order of atto ampere.

In this paper a new low-voltage, low-power regulated cascode current mirror has been proposed. At input side of the proposed design a 3-input FGMOS device has been introduced to control the input characteristics of CM by varying the input bias voltage at one of the floating gate. The design has been supported by the simulated results.

The rest of the paper is organised as follows: Brief introduction of FGMOS and regulated cascode current mirror (RCCM) is given in section 2. Section 3 describes the proposed low-voltage, low-Power CM (LV-LPCM). Simulation results are discussed in section 4. Finally, some conclusions are drawn in section 5.

2. FGMOS AND REGULATED CASCODE CURRENT MIRROR

In this section floating gate MOSFET (FGMOS) and regulated cascode CM (RCCM) have been briefly introduced with their diagrammatic representation. This section also justifies the implementation of FGMOS and RCCM into the final design.

2.1. Floating Gate MOSFET (FGMOS)

Floating Gate MOS transistors are widely used in digital world as EPROM, EEPROM, flash memories, and neuronal computational element in neural network, digital potentiometers and single transistor DAC's. But, it is also gaining its popularity in analog design and has found application in low-voltage low-power analog design and analog storage elements. A typical multi input floating gate transistor is shown in Figure 1. It is a conventional MOSFET in which the gate is capacitively coupled to the input using another poly-silicon layer. The equation that models the behaviour of floating gate voltage (V_{FG}) of FGMOS is given by equation (1) [1], [3].

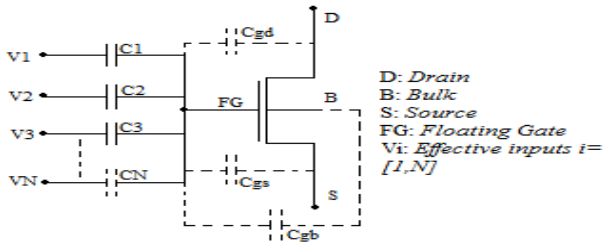

Figure 1. Equivalent schematic of N-input n-channel FGMOS

$$V_{FG} - \sum_{i=1}^{N} \frac{C_i}{C_T} V_i + \frac{C_{gs}}{C_T} V_S + \frac{C_{gd}}{C_T} V_D + \frac{Q_{FG}}{C_T} \quad (1)$$

Where $C_T - C_{gs} + C_{gd} + C_{gb} + \sum_{i=1}^{N} C_i$ and Q_{FG} accounts for the amount of charges that is being trapped in FG during fabrication.

FGMOS device provides impressive features relevant to low-voltage, low-power context. It shows flexibility in implementing both linear as well as non-linear functions. Independent control of threshold voltage (V_{th}) accounts for controllability of the device. Also, since it is a multi-input device, FGMOS allows addition of extra inputs as per designer's requirement and hence provide tunability to the circuit.

In order to simulate FGMOS in Cadence design environment, a simulation model is needed which is shown in Figure 2 [1], [3]. In the model, the voltages V_1, V_2, ..., V_n are the input voltages which are coupled to gate by resistor-capacitor parallel combination. V_F and V_0 are floating gate voltage and substrate voltage respectively. M is a conventional MOSFET.

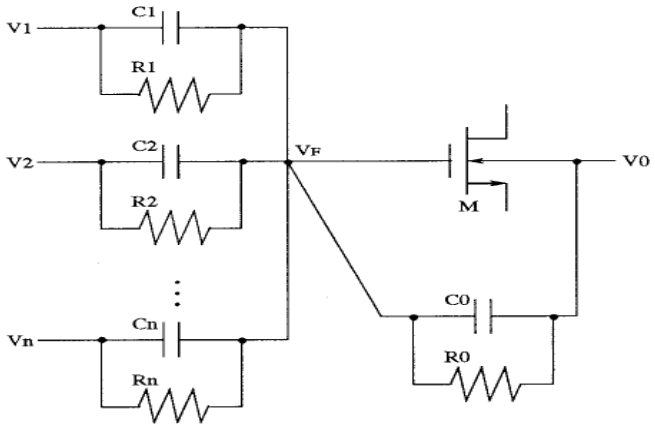

Figure 2. Simulation Model for N-input n-channel FGMOS

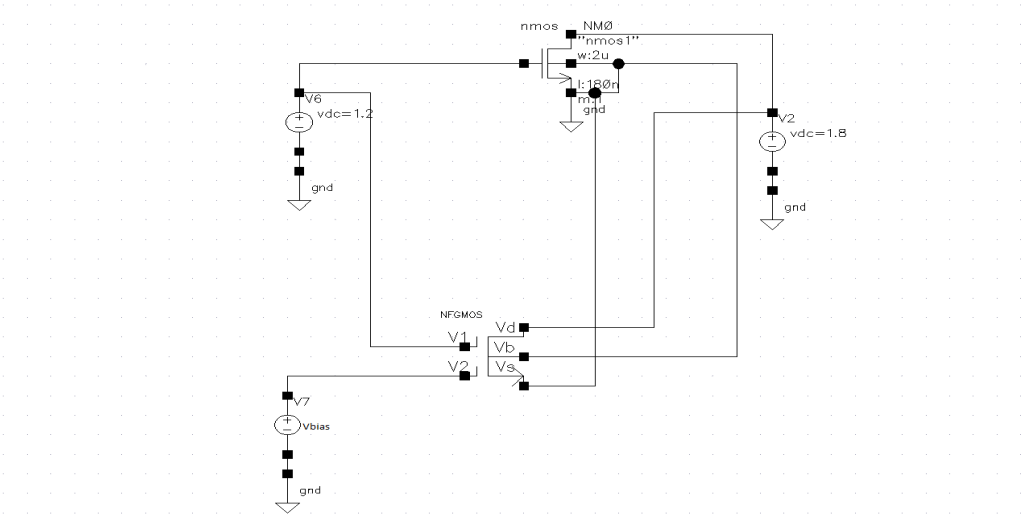

Figure 3. Test circuit for comparison between N-type FGMOS and NMOS

Figure 3 shows the test circuit for comparison between 2-input N-type FGMOS and a conventional NMOS. The simulated output characteristics and power dissipation on comparative basis is shown in Figure 4 and Figure 5 respectively.

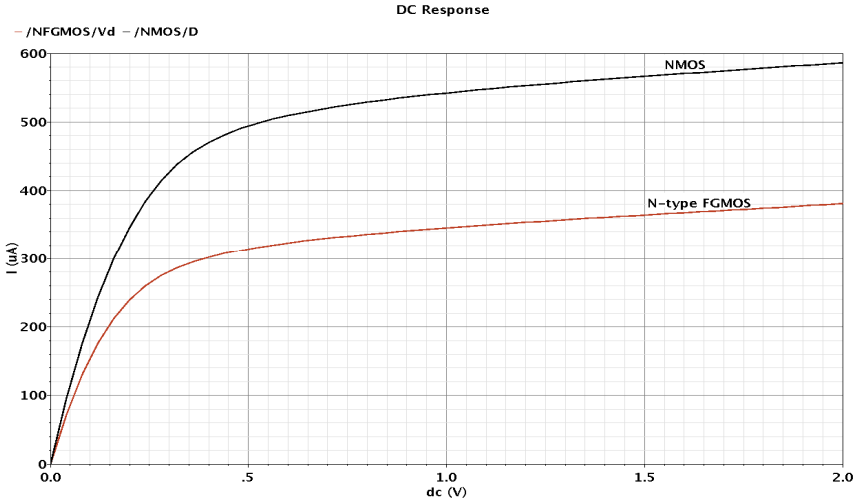

Figure 4. DC response of N-type FGMOS and conventional NMOS

Power dissipation of 2-input N-type FGMOS is 673.9 µW for the test circuit, which is nearly 40% less than that of conventional NMOS transistor. This suffices for one of the reason why FGMOS device is used in low-voltage, low-power design.

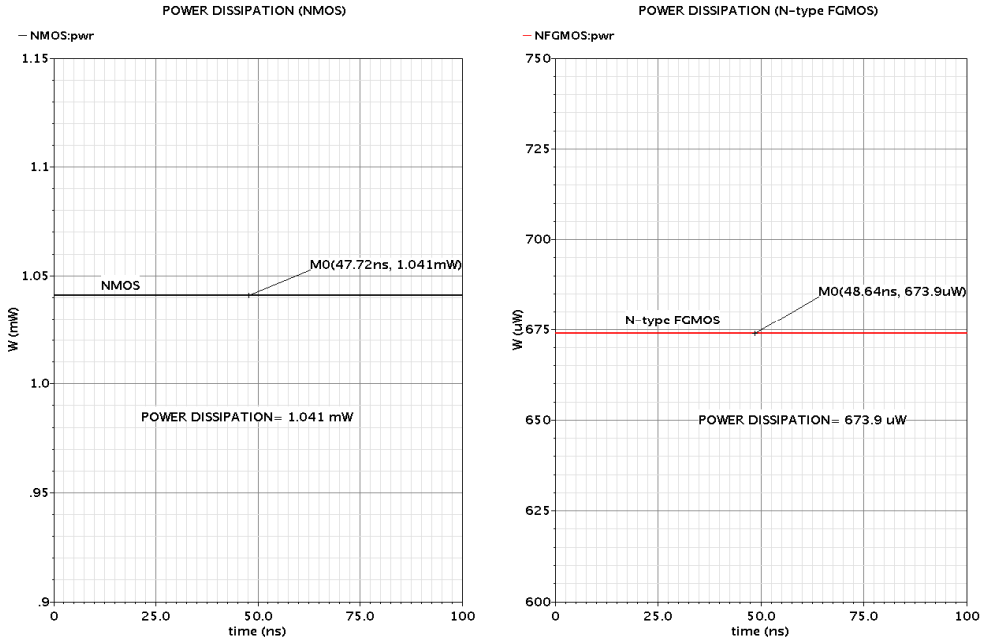

Figure 5. Power Dissipation of N-type FGMOS and conventional NMOS

2.2. Regulated Cascode Current Mirror (RCCM)

Regulated cascode CM is improved version of simple CM and it uses negative feedback concept for output current stabilization [2]. A typical regulated cascode configuration is shown in Figure 6. The primary reason behind considering RCCM configuration as a basis for the proposed design is its high output impedance of the order of $g_m^2 r_{out}^3$. Also, current gain matching for regulated cascode configuration is good as long as primary transistors are properly biased.

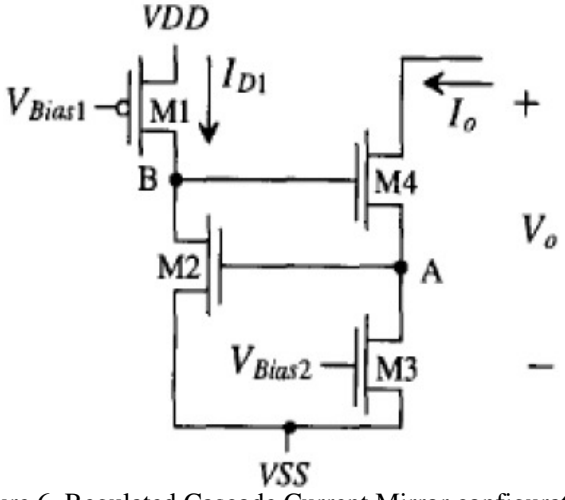

Figure 6. Regulated Cascode Current Mirror configuration

3. PROPOSED FGMOS BASED LV-LPCM

The proposed LV-LP RCCM is based on FGMOS technique and is shown in Figure 7. It allows the design to work at a voltage as low as +0.8 Volts but works best at a single supply voltage of +1.0 Volts. It exhibits good matching accuracy and high output impedance of the order of 1.125 TΩ.

Table 1. Transistor Sizes of the Proposed CM

Transistors	W(µm)	L(nm)	W/L
3-input N-Type FGMOS	18	180	100
NM0	36	180	200
NM1	18	180	100
NM2	5.4	180	30
NM3	18	180	100
NM4	18	180	100
PM0	18	180	100
PM1	18	180	100

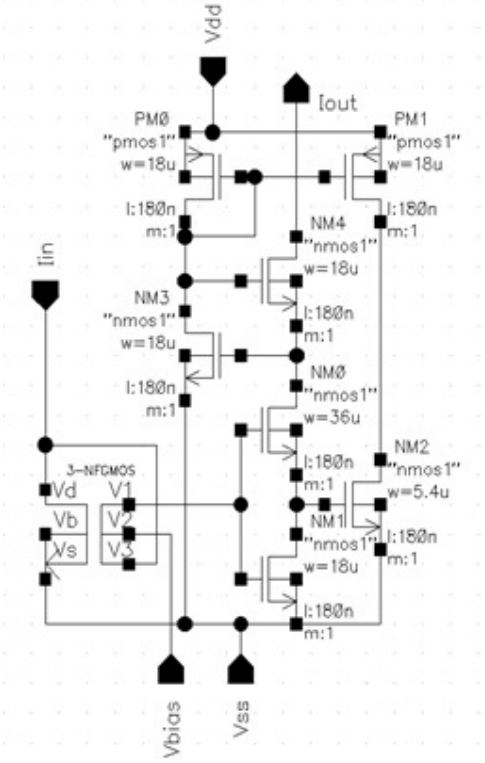

Figure 7. Proposed LV-LP Regulated Cascode CM

Power dissipation of the circuit has been reduced to a value as low as 10.56 µW. It achieves higher current range of up to 1500 µA. The aspect ratios for various transistors have been summarized in Table1.

Transistors NM1, 3-input N-type FGMOS, NM4 and NM3 accounts for conventional regulated cascode CM. Transistors PM0 and PM1 are biasing transistors and provides accurate matching at the output. Transistor NM2 is connected in negative feedback to increase the output resistance and stabilize the output current. NM0 is specifically introduced in common gate configuration to achieve higher output resistance up to TΩ range. The circuit however suffers from low bandwidth which is overshadowed by other satisfactory results viz. high output resistance, large current range and very low power dissipation.

3. SIMULATION RESULTS

The proposed circuit is simulated with Cadence Spectre simulator in Virtuoso ADEL environment. Various simulated results corresponding to its respective analysis viz. transient, DC or AC analysis with appropriate test circuits has been done. DC analysis is carried out to obtain current range. Figure 8 shows that the design achieves a current range of upto 1500 µA. Input and output characteristics are shown in Figure 9 and Figure 10 respectively.

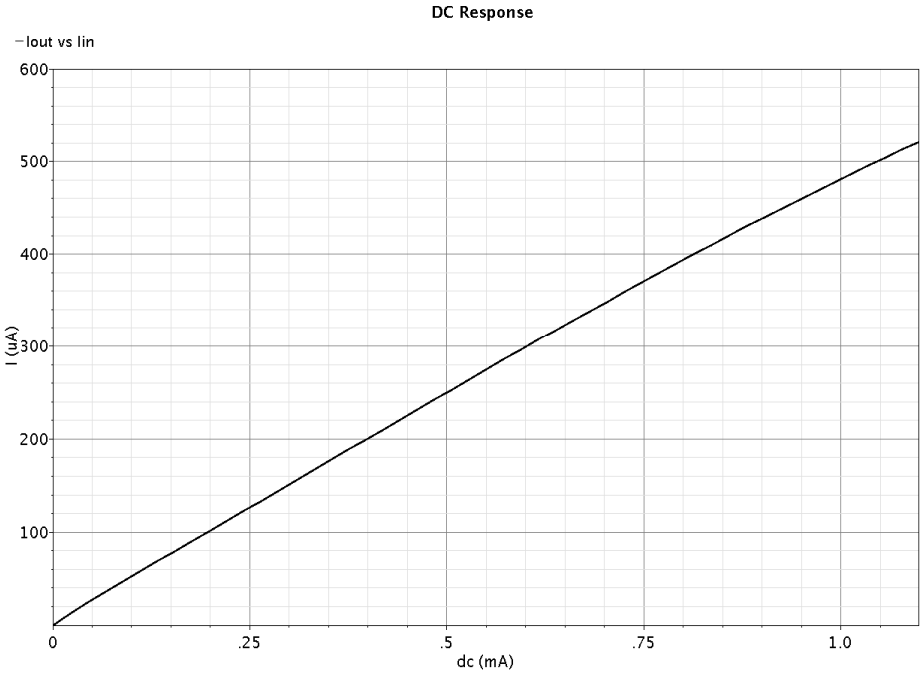

Figure 8. Transfer Characteristics

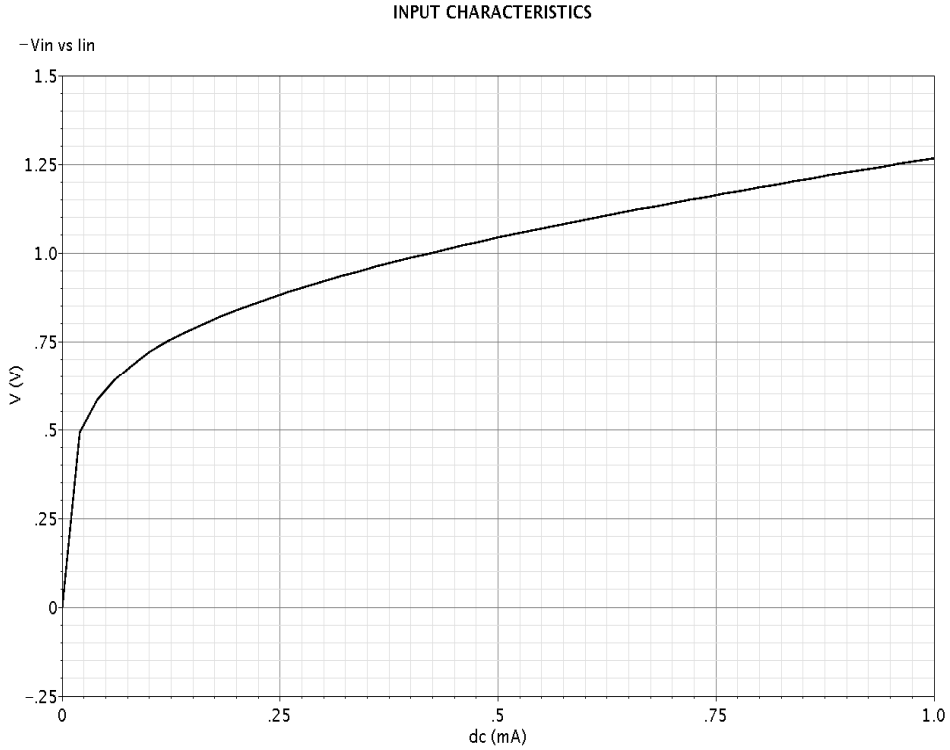

Figure 9. Input Characteristics

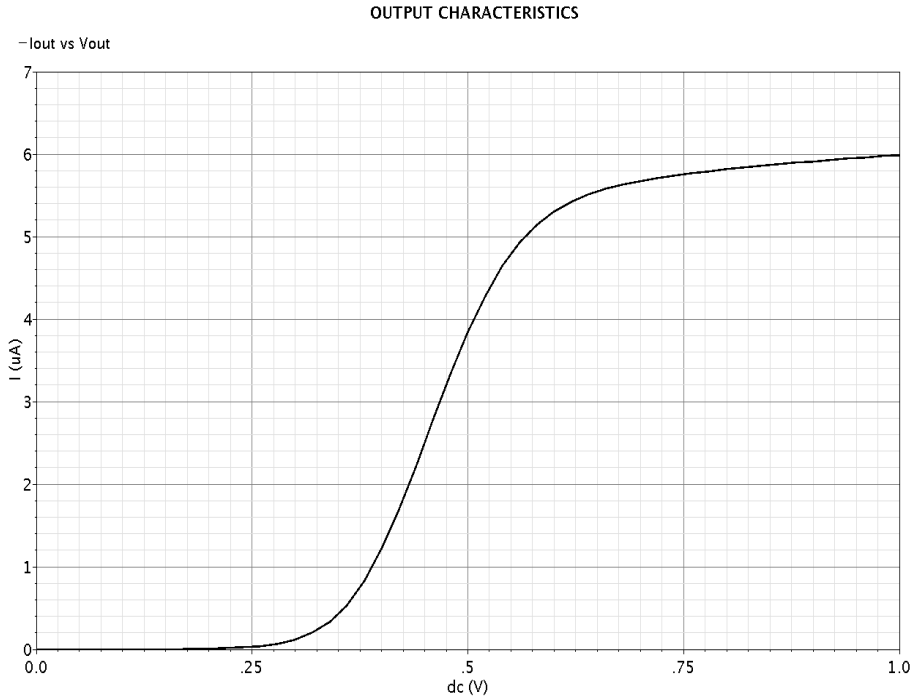

Figure 10. Output Characteristics

Figure 11 illustrates the variation in input resistances with input biasing current. It can be observed from the graph that input impedance of the circuit is 24.5 KΩ for biasing current of 20 µA and as low as 540 Ω for a input biasing current of 500 µA.

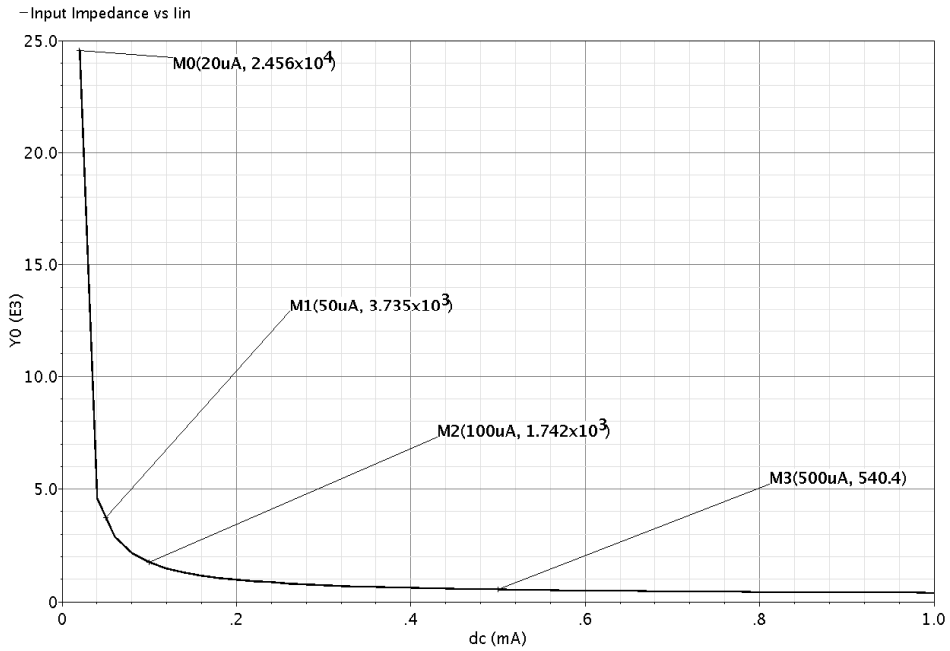

Figure 11. Input Impedance versus Input biasing current

Transient analysis is carried out to evaluate power dissipation of the circuit. It is observed to be 10.56 µW as shown in Figure 12, which makes the circuit a low power design.

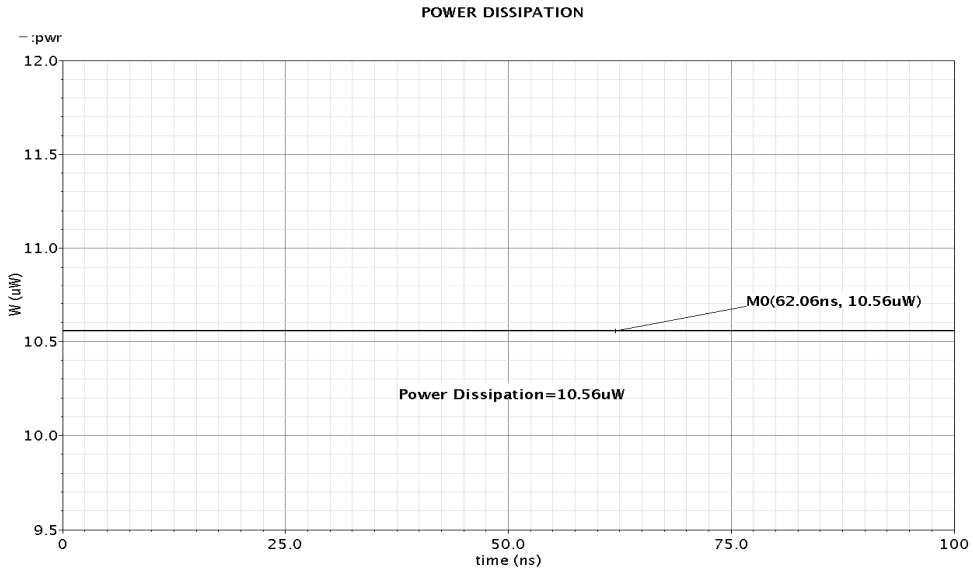

Figure 12. Power dissipation

AC analysis is performed to obtain the output impedance and bandwidth of the proposed FGMOS based LV-LP RCCM. The output impedance comes out to be 1.125 TΩ and bandwidth of 4.1 MHz at a biasing current of 10 µA and is shown in Figure 13 and Figure 14 respectively.

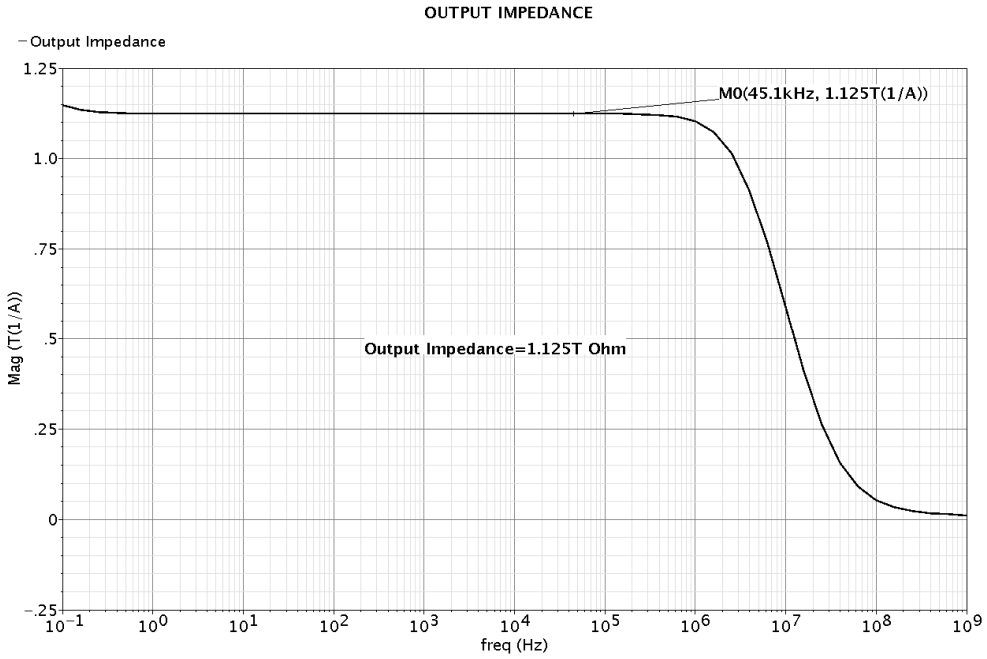

Figure 13. Output Impedance

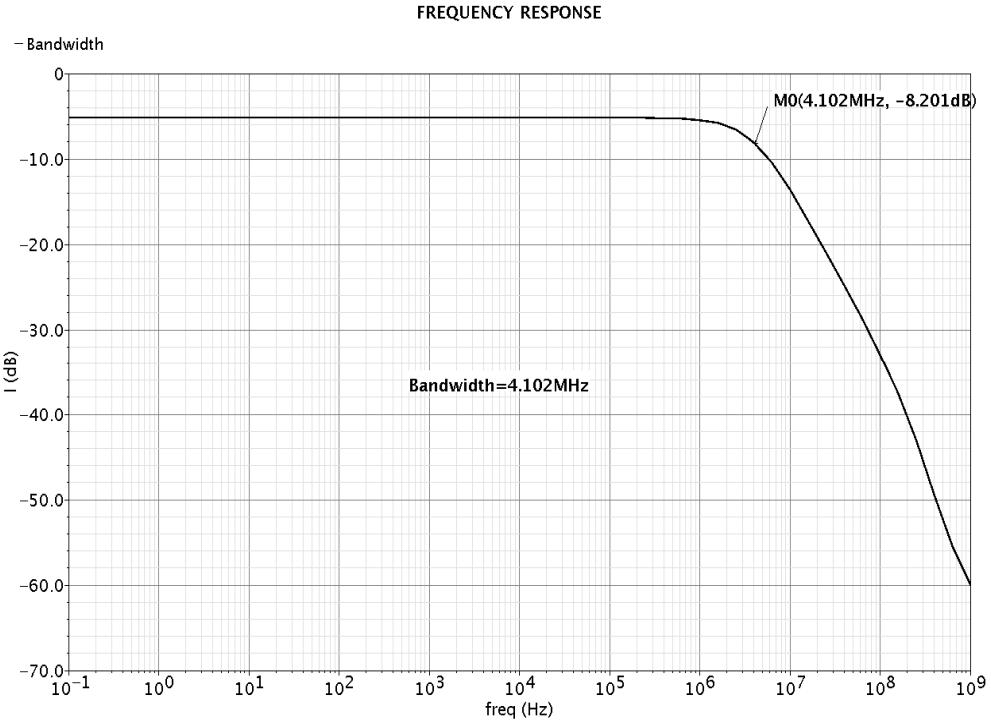

Figure 14. Frequency Response

The performance of the proposed design has been compared with previous works and is being presented in Table 2.

Table 2. Comparison with previous works

Parameters	Proposed Work	REF[12]	REF[7]	REF[9]	REF[8]	REF[4]
Process Technology (µm)	0.18	0.18	0.50	0.25	0.50	0.50
Supply Voltage (Volts)	+1.0(single supply)	±1.8	±0.75	±0.45	±0.75	±0.75
Current Range(µA)	0-1500	-	0.1-500	0-150	0-500	~2-500
Output Impedance(TΩ)	1.125	0.045	0.00135	0.0153	0.00167	0.7854
Input Impedance(KΩ)	3.73 (I_{bias}= 50 µA)	20000	0.2	1.99	0.48	-
Power Dissipation(µW)	10.56	1.5	-	96.5	1500	250
Bandwidth(MHz)	4.1	15.8	500	-	640	631

4. CONCLUSION

This paper demonstrates a floating gate MOSFET (FGMOS) based low-voltage, low-power regulated cascode current mirror which exhibits a very high output impedance of 1.125 TΩ and dissipates power as low as 10.56 µW at an input biasing current of 10 µA. The current range for the circuit is also at par with respect to other design. The proposed design can work well with low-power, low-voltage analog signal processing & bio-medical application. Measured performance of proposed current mirror is comparable with other proposals reported to date, as shown in Table 2. The simulation is done in Cadence design environment for 180 nm CMOS technology with a single power supply of +1.0 Volts.

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