THE DESIGN OF A LOW POWER FLOATING GATE BASED PHASE FREQUENCY DETECTOR AND CHARGE PUMP IMPLEMENTATION

Md Monirul Islam[1] and Ankit Shivhare[2]

[1]Department of Electronics Engineering, KIIT University, Bhubaneswar, India
imoniofficial@gmail.com
[2]Department of Electronics Engineering, KIIT University, Bhubaneswar, India
ankitshivharenitdgr@gmail.com

ABSTRACT

A simple new architecture of phase frequency detector with low power and low phase noise is presented in this paper. The proposed phase frequency detector is based on floating gate, consist of 4 transistors including one floating gate pMOS and one floating gate nMOS constructed with two GDI (gate diffusion input) cells and maintain main characteristics of conventional phase frequency detector in 180 nm technology. Floating gate based methodology reduced the power of phase frequency detector about 51%. Introduction of floating gate based phased frequency detector also reduces the number of transistor as compared with conventional phase frequency detector.

KEYWORDS

Phase frequency detector, floating gate MOSFET, Voltage controlled oscillator, Gate diffusion cell, Charge pump.

1. INTRODUCTION

The recent development of communication system has brought an increase demand for low power and low noise system in phase-locked loop (PLL) design. Phase frequency detector is the most key element in PLL design. The two non linear components present in PLL are phase frequency detector (PFD) and voltage controlled oscillator (VCO). The main concept of phase frequency detector or PFD is comparing two input frequencies in terms of both phase and frequency. In a PLL the two frequencies are reference frequency (clk_ref) and voltage controlled oscillator (VCO) output after division by N (clk_vco). The output is a pulse proportional to the phase difference between the inputs and it drives the charge pump to either increase the control voltage of the VCO or decrease it or keep it without changing. A PFD is usually built using by state machine with memory element such as D flip-flop. There are many methodologies to simplify the circuit. This paper presents a novel architecture of PFD design that floating gate based PFD improves the power dissipation as compared with conventional PFD. As Floating gate based circuit can operate at power supply voltage levels which are well below the intended operational limits for a particular technology and consume less power than the minimum required power of a circuit designed with only MOS devices in the same technology with the same performance.

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2. PHASE FREQUENCY DETECTORS

Figure1 illustrates a common linear PFD architecture using two D flip flop implemented using CMOS logic and a AND gate in the reset path. The PFD generates an UP and a DOWN signal that passed through the charge pump followed by a loop filter and VCO. When clk_ref goes high it will charge the upper D flip flop and results in UP signal to high and when clk_vco signal goes high it will result DOWN signal to high. This will result both the inputs of AND gate high and make the reset signal high to make both outputs low. It is known as the lock condition for the PFD when both the outputs of PFD – UP signal and DOWN signal are low. When clk_ref is leading it will result UP signal high and when lagging result DOWN signal high. The width of the UP signal or DOWN signal is the measure of error. With the use of this error the control voltage is generated and then that will correct out the frequency difference between input CLK and the clock coming from the VCO from feedback path of the PFD [2].

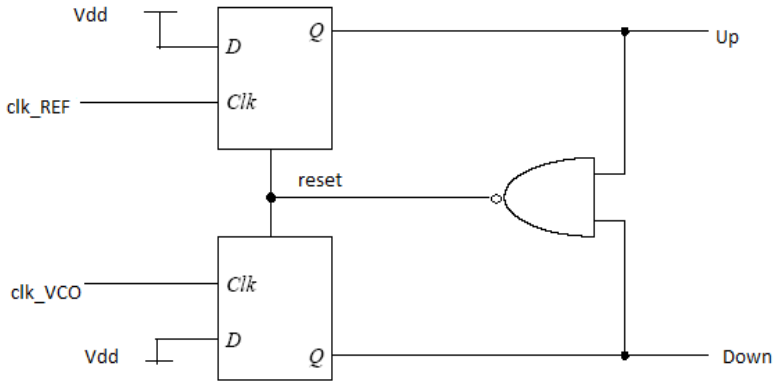

Figure 1.Linear PFD detector

2.1. GDI BASIC CELL METHODLOGY

GATE DIFFUSION INPUT (GDI) technique has been used for the simultaneous generation of digital logic functions**.**The GDI method is based on the use of a simple cell as shown in Figure 2. At a first glance the basic cell resembles the standard CMOS inverter, but there are some important differences: GDI cell contains three inputs–G (the common gate input of the nMOS and pMOS transistors), P (input to the outer diffusion node of the pMOS transistor) and N (input to the outer diffusion node of the nMOS transistor).The Out node (the common diffusion of both transistors) maybe used as input or output port, depending on the circuit structure[3].the most advantages of GDI cell over CMOS technology are low power circuit design, allows reducing power consumption, reducing propagation delay and area, it also maintains low complexity of logic design.

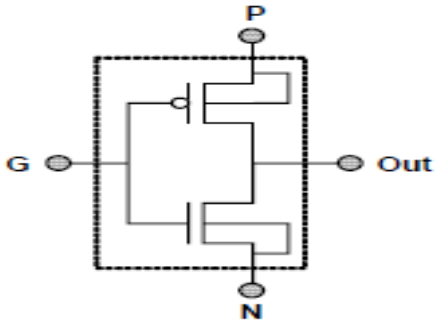

Figure 2.GDI basic cell

N	P	G	Out	Function
'0'	B	A	$\bar{A}B$	F1
B	1	A	$\bar{A}+B$	F2
1	B	A	A+B	OR
B	'0'	A	AB	AND
C	B	A	$\bar{A}B+AC$	MUX
'0'	1	A	$\bar{A}$	NOT

Table 1. Logic function of GDI cell

2.2. GDI BASED PHASE FREQUENCY DETECTOR

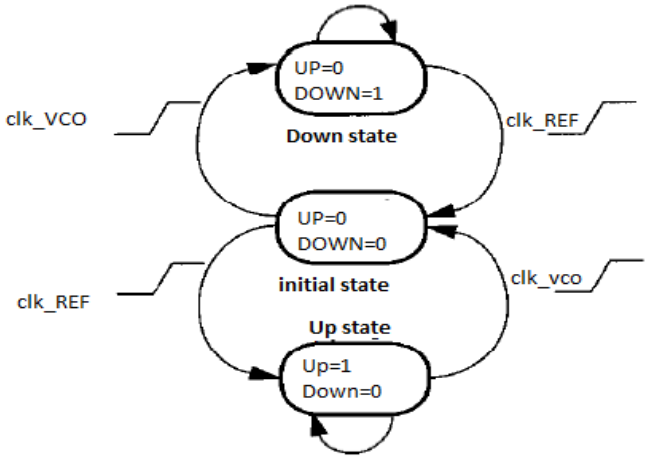

Figure 3.PFD state diagram

Figure 3 illustrates the finite state machine (FSM) of phase frequency detector. Initially both UP and DOWN both signal are low. When one of the PFD input rises then corresponding output becomes high. This state remains same until second input goes high which resets the circuit and returns the FSM to the initial state [2].

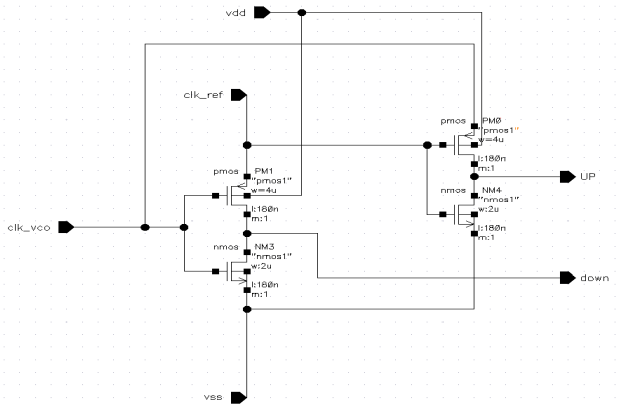

Figure 4.GDI based phase frequency detector.

From basic GDI cell view table 1 when the supply voltage B is applied to PMOS and nMOS is grounded and given input voltage in gate terminal is A then it gives output in the common drain is $\bar{A}B$.In figure 4, DOWN signal comes from the common drain terminal of pMOS PM1 and nMOS NM3 and UP signal comes from the common drain of pMOS PM0 and nMOS NM4. The UP signal of this circuit is $\bar{clk}\_ref \times clk\_vco$ and the DOWN signal is $\bar{clk}\_vco \times clk\_ref$. So we take output from common drain of this inverter configured on GDI cell.In this congiguration there are only four transistors are use [1].the body bias substrate of pMOS is connected with VDD and nMOS is connected with VSS ground.

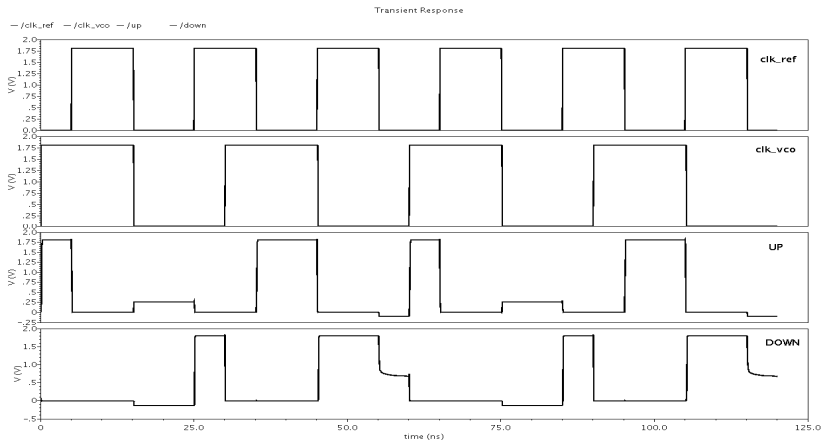

Figure 5. Simulation of GDI based phase frequency detector

2.3. CHARGE PUMP

A charge pump is a three position electronic switch which is controlled by the three states of PFD. When switch is set in UP or DOWN position, it delivers a pump voltage $\pm V_P$ or a pump current $\pm I_P$ to the loop filter. When both UP and DOWN of PFD are off, the switch is open, thus isolating the loop filter from the charge pump and PFD.

The charge pump coupled is a vital building block in the design topology, it helps provide an effective controlling mechanism for the charging and discharging of the low pass filter.Also it is

used to manipulate the amount of charge on the loop filter capacitor depending on the UP and DOWN signals from phase frequency detector [4]

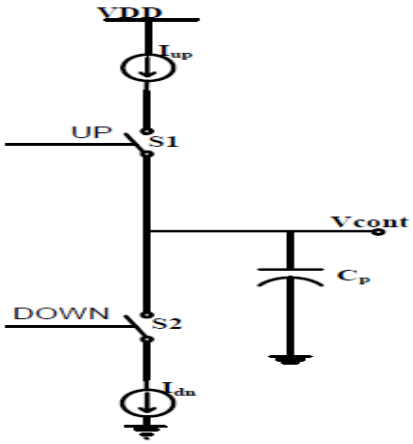

Figure 6. Concept illustrating charge pump circuit

3.1. FLOATING GATE MOSFET

An FGMOS can be fabricated by electrically isolating the gate of a standard MOS transistor, so that there are no resistive connections to its gate. A number of secondary gates or inputs are then deposited above the floating gate (FG) and are electrically isolated from it. These inputs are capacitive connected to the FG, since the FG is completely surrounded by highly resistive material. So, in terms of its DC operating point, the FG is a floating node. [5]

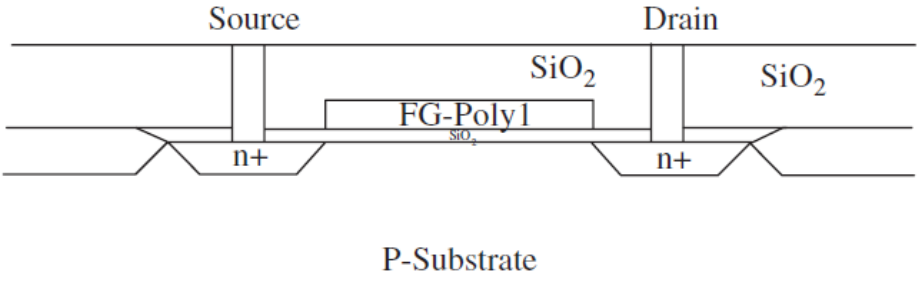

Figure 7. Cross Sectional view of n channel FGMOS

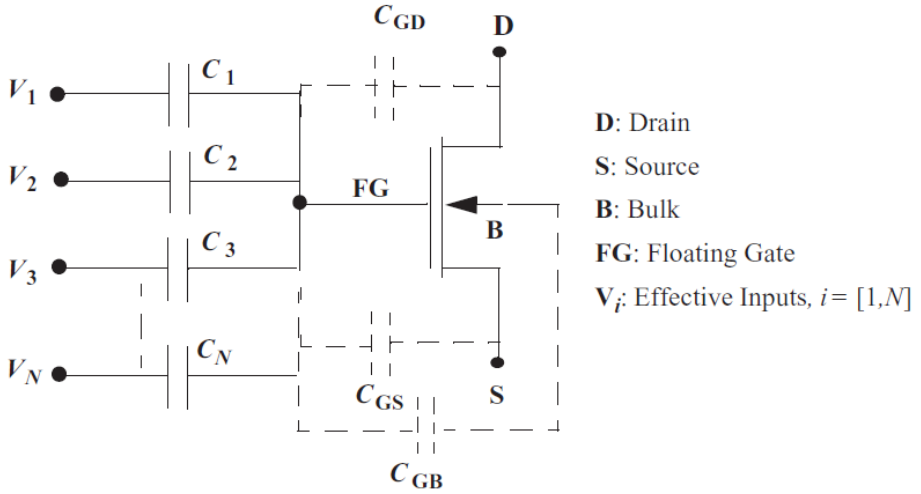

Figure 8.Equilvalent Schematic of n channel N input FGMOS transistor

The distinctive feature of the FGMOS device is the set of input capacitors, denoted Ci where i = [1, N] in Figure 8, between the effective inputs and the FG. The parasitic capacitances, C_{GD} and C_{GS}, represented using dotted lines, are the same parasitic capacitances that would be present in an MOS transistor fabricated using the same technology with the same active area. The relationship between the DC drain to source current and the FG voltage, V_{FG}, of an FGMOS is not affected by parasitic capacitances. However, C_{GD}, C_{GS} and C_{GB} do affect the relationship between V_{FG} and the effective input voltages V_i.

The value of V_{FG} can be obtained by applying the charge conservation law to the floating node (FG) shown in Fig.8. If there is an infinite resistance between the FG and all the surrounding layers, there will be no leakage current between them, and so, the FG will be perfectly isolated. So the voltage at the FG is given by [5]

$$V_{FG} = \sum_{i=1}^{N} \frac{C_i}{C_T} V_i + \frac{C_{GS}}{C_T} V_S + \frac{C_{GD}}{C_T} V_D + \frac{Q_{FG}}{C_T} - - - \; - - - - \; (1) without\ body\ bias$$

$$V_{FG} = \sum_{i=1}^{N} \frac{C_i}{C_T} V_{iS} + \frac{C_{GB}}{C_T} V_{BS} + \frac{C_{GD}}{C_T} V_{DS} + \frac{Q_{FG}}{C_T} + V_S - - - \; (2) with\ body\ bias$$

where N is the number of effective inputs.

The term QFG refers to a certain amount of charge that has been trapped in the FG during fabrication. As this term is constant, it can be interpreted as a voltage offset at the FG, or alternatively, as an offset in the threshold voltage of the device. The term CT refers to the total capacitance seen by the FG and is given by [5]

$$C_T = C_{GD} + C_{GS} + C_{GB} + \sum_{i=1}^{N} C_i - - - \; (3)$$

The equations modelling the large signal behaviour of the FGMOS can now be obtained by replacing VGS in the equations describing the large signal behaviour of the MOS transistor, with the expression describing the voltage between the FG and source which can be obtained by referring VFG to the source terminal rather than the bulk.

4. PROPOSED PHASE FREQUENCY DETECTOR USING FGMOS

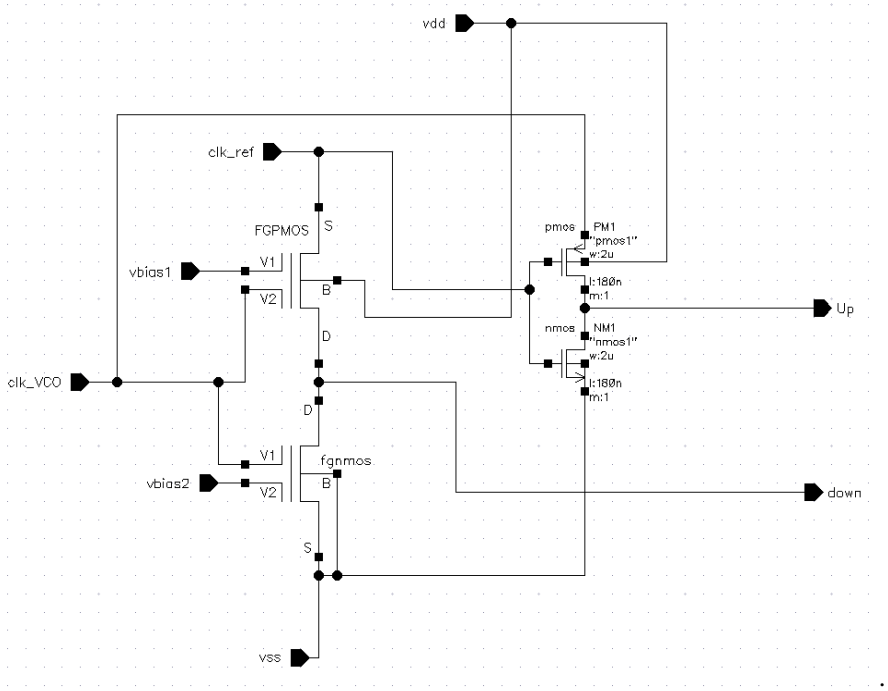

Figure 9.Circuit diagram of the proposed PFD

The proposed phase frequency detector consist of 4 transistor including both FGMOS of n type and p type.V1 of the FGPMOS is connected with bias voltage Vbias1 and V2 of FGNMOS of is connected with Vbias2 voltage. Common gate of both FGMOS are given clk_vco input. The source of the FGPMOS is given clk_ref as reference signal. The output DOWN signal is drawn from common drain of two FGMOS. UP signal is drawn from common drain of PM1 and NM1.When REF signal leads the feedback VCO signal the PFD detects a rising edge on the REF signal and it will produce the UP signal and when feedback clk_vco signal leads reference signal clk_ref it will produce the DOWN signal.

5. SIMULATION RESULT

The proposed phase frequency detector is given two pulse sequences clk_ref and clk_vco. For simulation we apply clk_ref at 50MHz and clk_vco at 33.33MHz.

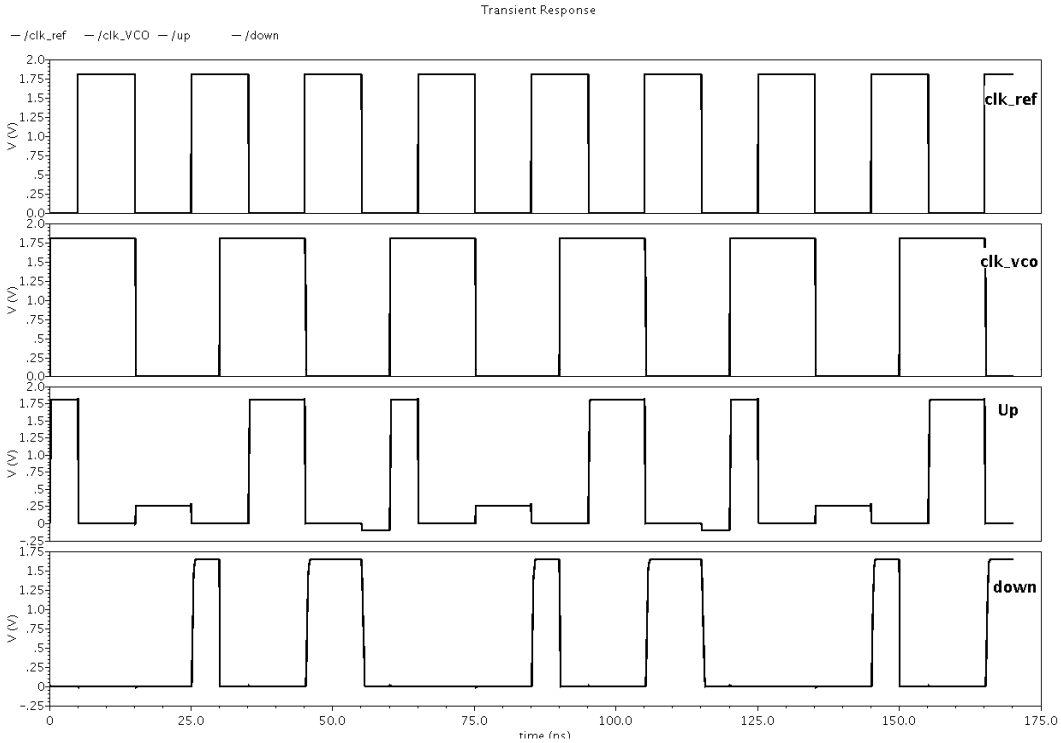

Figure 10.Input and Output waveform of proposed PFD

The output of the proposed PFD is given to the VCO after passing through charge pump and loop filter. Charge pump provide an effective controlling mechanism for the charging and discharging of the low pass loop filter. It is used to manipulate the amount of charge on the loop filter's capacitors depending on the UP and DOWN signal generated from phase frequency detector. When UP signal goes up, the charge pump drives current into the loop filter which change the VCO control voltage in such a way that frequency is increased and when DOWN signal goes up, charge pump draw current from the loop filter to change the control voltage and slowdown the VCO output frequency. Loop filter also removes jitter from charge pump to smoothen the control voltage.

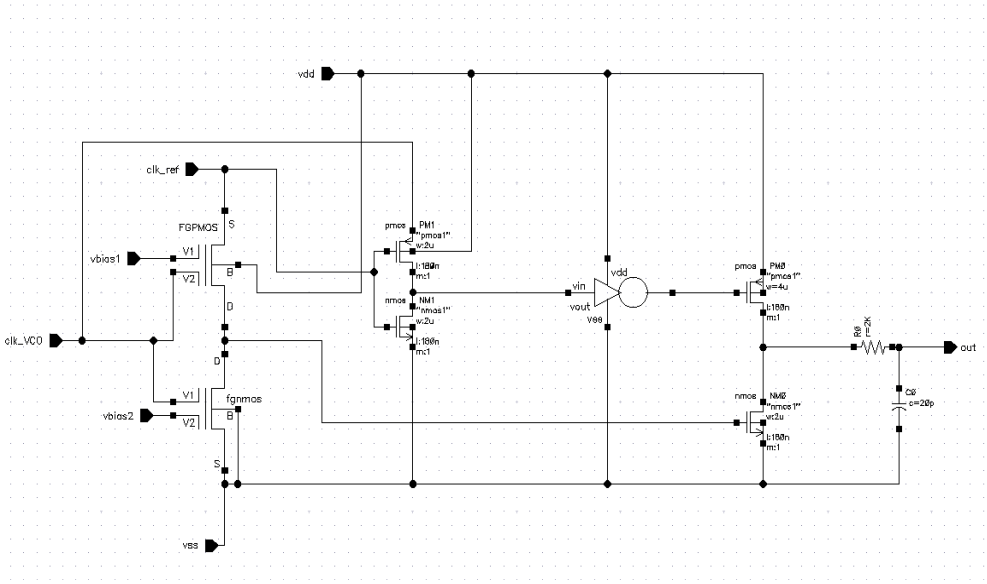

Figure11. Proposed PFD and Charge pump

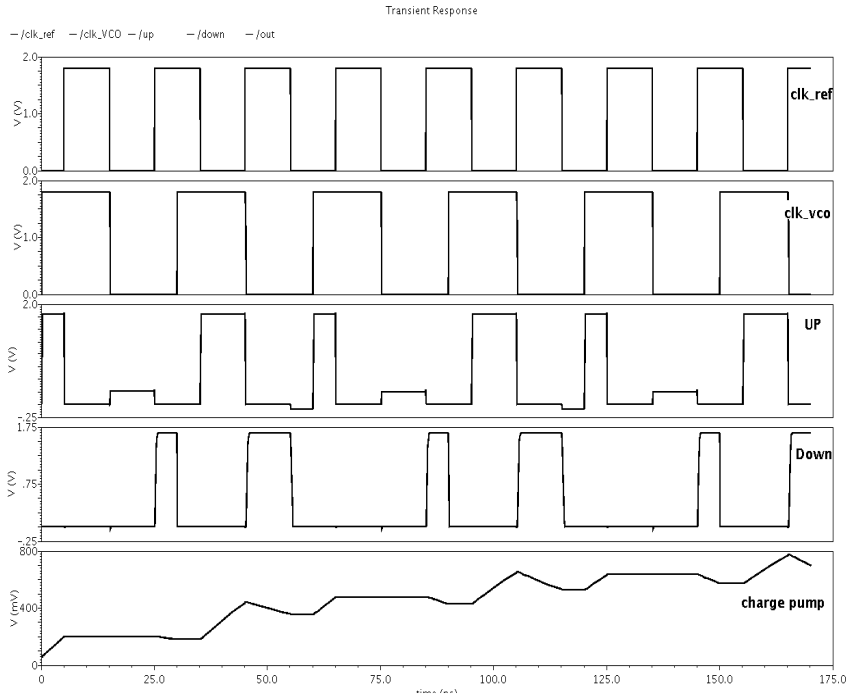

Figure 12.Input output waveform of PFD and charge pump

5.1. PHASE NOISE ANALYSIS

The phase noise in Up and Down translates to random modulation of the time during which noise is injected into the loop filter. There are three possible cases. The phase noise may modulate the widths of Up and Down by the same amount, in which case the CP produces no net output. The phase noise modulates only the position of Up with respect to Down. This effect is negligible. Lastly, the phase noise may modulate the widths of Up and Down pulses differently and it is this

case that matters most [6]. The power supply 1.8V.the phase analysis is simulated cadence virtuoso 180nm technology where the clk_vco in 25MHz and clk_ref 50MHz.

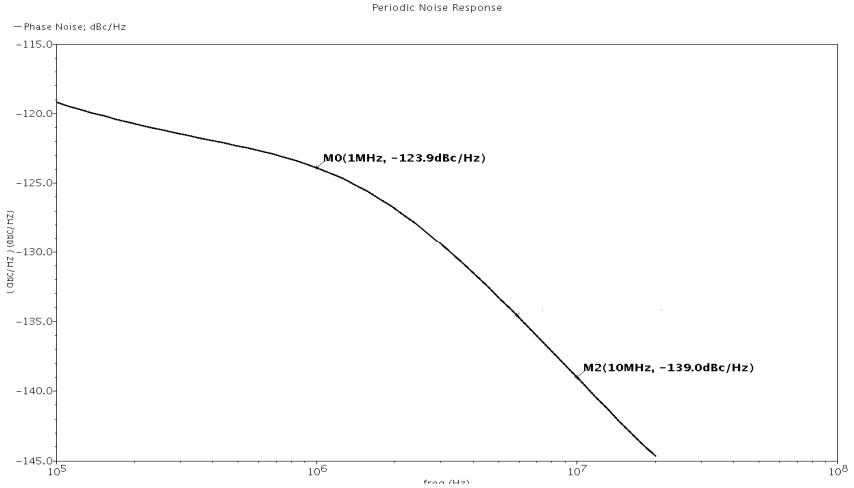

Figure 13.GDI based PFD phase noise

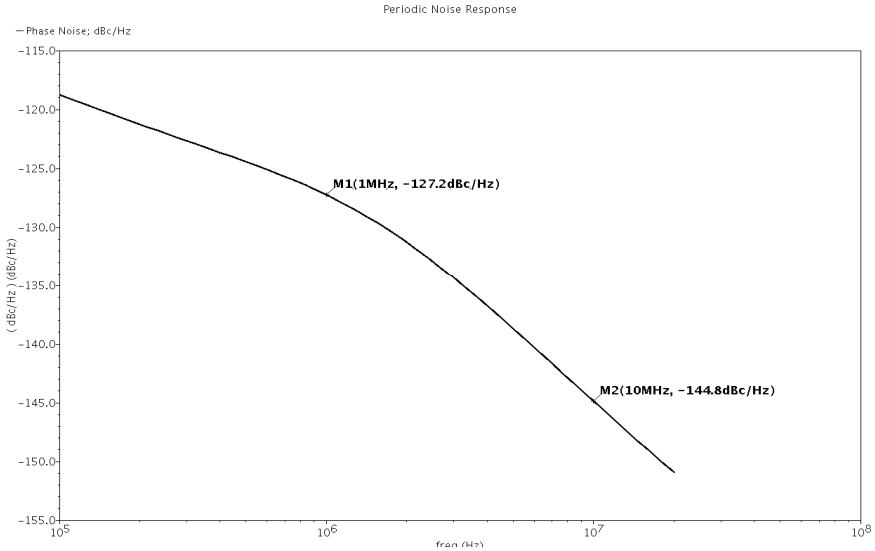

Figure 14. Proposed PFD phase noise

SI no PFD_S	Number of transistor	Power consumption	Types of transistor
Conventional	48	33µ	nMOS, pMOS
Proposed PFD	4	16.1µ	FGPMOS, FGNMOS, nMOS, pMOS

Table 2: Performance comparison between different PFD topologies

SI no PFD_S	Phase noise	Offset frequency at
Conventional	-112dbc/Hz	1 MH_Z
GDI based PFD	-123.9dbc/Hz	
Proposed PFD	-127.2dbc/Hz	

Table 3: Performance comparison between different PFD topologies

6. CONCLUSIONS

This paper presents a new phase frequency detector or PFD architecture and charge pump implementation using cadence 180nm 1.8V CMOS process technology. Most important advantage of using floating gate reduce the power consumption. Use of floating gate reduces the power 51% in proposed circuit, which is dominant factor in low power application This paper also presents the minimum number of transistor for implementing PFD which becomes a crucial factor in deep submicron as space is very important factor for complex circuit. The proposed phase frequency detector maintain all functionality of a conventional PFD. Implementation of charge pump circuit in the PFD circuit for phase lock loop application is also verified to present the accuracy of proposed circuit. The presented circuit also very much noise free as its investigation result shows -127dbc/Hz phase noise at 1 MHz frequency offset which is less than the both conventional and simple GDI based phase frequency detector circuit. So the presented circuit confirms its applicable identity for charge pump operation within a high performance PLL application.

REFERENCES

[1] S.Siva, S.Yellampalli, Design of phase frequency detector and charge pump for high frequency PLL,international journal of soft computing and engineering.vol-2,issue-2,May 2012.

[2] M.Mansuri, DeanLie, Ken yang Fast frequency acquisition phase-frequency detector for Gsample/sphase locked loops.IEEE journal of solid state circuits.vol.37,no 10,oct 2002.

.[3] A.Morgenshtein, M.Moreinis, R.Ginosar,Asynchronous gate-diffusion input(GDI) circuits,Electrical engg.dept,Isreal Institute of technology,Isreal.

[4] A.Mann,A.Karalkar,Lili He,M.Jones, department of electrical engineering,San Jose State Univrsity,CA,USA

[5] Esther Rodriguez-Villegas ,Low Power and Low Voltage Circuit Design with the FGMOS Transistor, Published by The Institution of Engineering and Technology, London, UK.

[6] A.Homayoun,B.Razavi, Analysis of Phase Noise in Phase/Frequency Detectors, IEEE transactions on circuit and system regular paper,vol .60,no-3,March 2013

Authors

Md Monirul Islam : He received his B.E degree in electronics and communication from The University of Burdwan, West Bengal, India in 2011.He is currently perusing his M.tech course in VLSI and Embedded System from KIIT University, Bhubaneswar, India. His area of research topic in digital VLSI design, logic design verification, Low power VLSI.

Ankit Shivhare : He is currently working as Assistant Professor in School Of Electronics Engineering, Kalinga Institute of Industrial Technology (KIIT University), Bhubaneswar, Odisha. He has completed his BE in 2010 field of Electronics and Communication from Government Engineering College, Jabalpur, Madhya Pradesh and MTech in 2012 specialization in Microelectronics and VLSI from National Institute Of Technology Durgapur, West Bengal. He has lecture subjects including Electromagnetic Theory, Semiconductor Device, Control System, Analog Electronic Circuits, Digital Electronic Circuits, MOSFET Device Modelling, VLSI Design, Communication System- Analog and Digital, Basic Electrical Theory etc. His current interest includes Analog, Digital, Mixed Signal IC Design.