SMART MULTICROSSBAR ROUTER DESIGN IN NOC

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ABSTRACT

This paper gives the innovative idea of designing a router using multicrossbar switch in Network on Chip(NoC) . In Network-on-Chip architectures the input buffer can consume a large portion of the total power. Eliminating all input buffer would result in increased power consumption at high load, while reducing the size of input buffer degrades the performance. In this paper we have proposed a muticrossbar router design using elastic buffer by combining the advantage of both buffered and buffer less network. In the proposed design Power Delay Product is reduced by around 37 .91% as compared to baseline router.

KEYWORDS
Network on chip, Virtual Channel, Virtual Allocator, Elastic Buffer, Power Delay Product (PDP).

1. INTRODUCTION

As the technology increases in order to improve the performance of future multi-cores the researcher reduce the wire delay[1] .Insertion of buffer reduce wire delay as a result power consumption increases. In order to solve these wire delay and scalability issues, researchers suggested the use of a packet based communication network which is known as Network-on-Chip (NoC)[2,3]. One of the major research challenges currently faced by NoC designers is that of power dissipation, Power is dissipated by the NoCs in communicating data across the links as well as in the storage and switching functions within the routers [4,5]. Researchers have shown that almost 46% of the router power was consumed by the input buffers. Here elastic buffer (EB) flow control utilizes existing pipeline flip-flops in the channels to implement distributed FIFOs, eliminating the need for input buffers at the routers[6]. In the proposed design the in place of single crossbar ,muticrossbar switch is used. The multi-crossbar configuration provides the lower area due to split crossbars, reduces delay due to shorter path lengths and higher throughput due to selective merging of different output ports.Here performance is evaluated on the basis of power and delay product.

2. RELATED WORK

Different techniques have been proposed to reduce or eliminate the size of input buffers. Initially iDEAL, a low-power area-efficient NoC ia achive by reducing the number of buffers within the router[9]. Other designs targeting power saving with router design have different approaches. A dynamic buffering resources allocation design named ViChaR (Virtual Channel Regulator) focuses on efficiently allocating buffers to all virtual channels, by deploying a unified buffering unit instead of a series of separated buffers, and minimizing the required size[10]. Another approach utilizing channel buffering is the Elastic Channel Buffers (ECB), which replaces the repeaters with flip-flops, and eliminates the router buffers altogether [6]. Other bufferless

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networks such as FlitBLESS [7] and SCARAB [8] adopt either deflecting or dropping conflicting packets, thereby reducing the latency and power, while sustaining throughput at low network loads while at higher network loads, these networks suffer deflection/dropping leading to an increase in power consumption. The crossbar within the NoC has also received a lot of attention due to area overhead and power consumption.Reasearcher have proposed crossbar optimizations that reduced the power consumption and area overhead and channel buffer organization. In the proposed design elastic buffer multicrossbar router is implemented in which elastic buffer is used for storage , single channel ,and muticrossbar configuration is defined.

3. ARCHITECTURE OF BASELINE ROUTER

A router in NoCs consists of buffers, switches, and control units which are required to store and forward flits from the input ports to the desired output ports. The architecture is actually similar to that of modern routers, but with smaller area and buffer size .Figure :1 shows a NoC 16 buffer slots per input port. The buffer slots are divided into four queues, and each queue is called a virtual channel (VC) [11,14]. There are four cardinal input ports and output ports connected from and to +x, -x,+y and- y directions. The last pair of input/output ports are connected from and to the processing element (PE). The four VCs are sandwiched between the de-multiplexer connected to the input port, and the multiplexer connected to the crossbar. Each input unit can communicate with router, virtual-channel allocator, and switch allocator[13], which are responsible for Routing Computation (RC), Virtual-Channel Allocation (VA), and Switch Allocation (SA), respectively. The crossbar is controlled by the switch allocator for correctly connecting input ports to output ports [12].

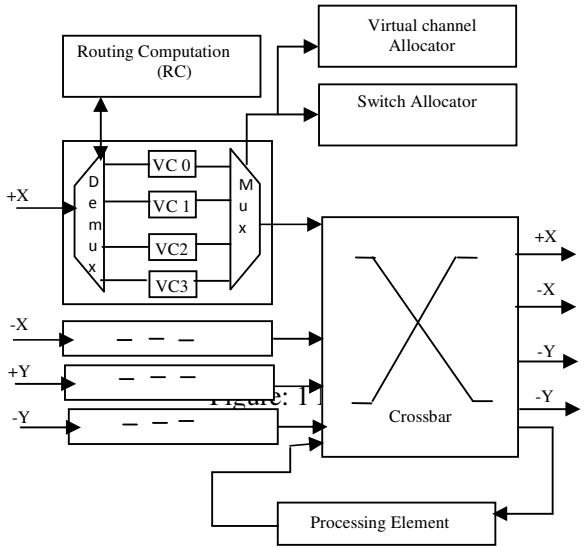

Figure: 1 Base Line Router

4. PROPOSED ELASTIC BUFFER MULTICROSSBAR DESIGN

In the proposed multicrossbar router shown in Figure: 2 single cross bar is split into four smaller crossbars to reduce area and delay. The division of the 4 crossbars are along the 4 quadrants: (+x, +y) [North-East], (-x, -y) [South-West], (-x, +y) [North-West] and (+x, -y) [South-East].The packet arrives from +x direction into I_0, indicating that the quadrant is (x+, y+). This packet can be routed to either O_0 (+x direction) or O_2 (+y direction) using the North-East crossbar. Similarly, if the packet arrives from +x direction from I_0 direction into the South-East crossbar, then the possible outgoing directions will be O_0 and O_3, indicating that the destination quadrant is (x+, y-).

Therefore, by limiting the crossbar connections and combining select crossbar outputs, we adaptively provide more opportunities for the output ports to be occupied than a conventional crossbar. The multi-crossbar configuration provides lower area due to split crossbars, reduce delay due to shorter path lengths and higher throughput due to selective merging of different output ports.

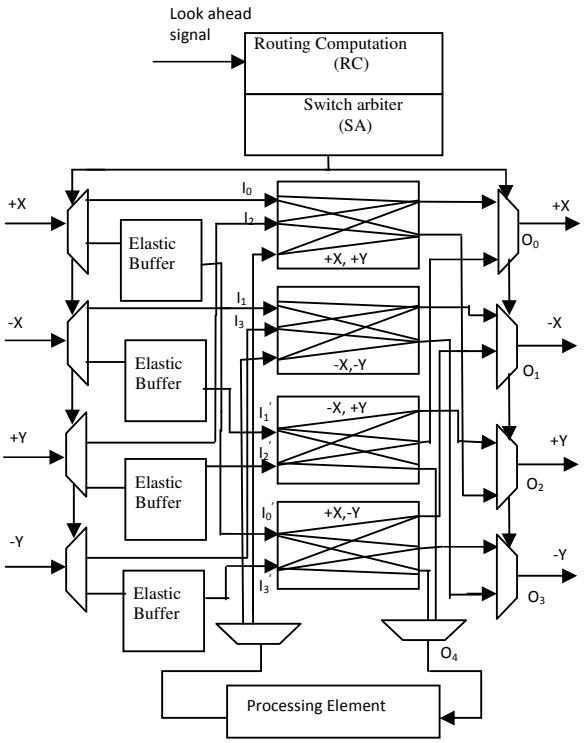

Figure: 2 Proposed Elastic Buffer Router Using Multicrossbar

The function of processing element is to give feedback from output to input to show whether the flit is valid or not. Buffers are in which the data moves serially as the virtual channel is eliminated so the virtual allocator stage is eliminated. Switch arbiter (SA) is modified to make control over the Demux and Mux to maintain the correct packet flow in the crossbars.

4.1. Elastic buffer

Elastic buffers (EBs) is an efficient flow-control scheme that uses the storage already present in pipelined channels instead of input virtual-channel buffers(VCBs). Removing VCBs reduces the area and power consumed by routers, but prevents the use of virtual-channel.

4.1.1 Elastic Buffer Channel

Here elastic buffer channel is discussed. EB channel is implemented by using Dflip-flop (DFF) and control logic. Dflip-flop (DFF) shown in Figure: 3(a) is implemented using master slave flip flop. EBs shown in Figure: 3(b) use a ready-valid handshake to advance a flit (flow-control digit).An upstream *ready* (R) signal indicates that the downstream EB has at least one empty storage location and can store an additional flit. A downstream *valid* (V) signal indicates that the flit currently being driven is valid. A flit advances when both the ready and valid signals between two EBs are asserted at the rising clock edge.

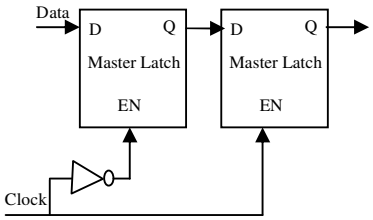

Figure: 3(a) DFF (D-flip flop) using master slave FF

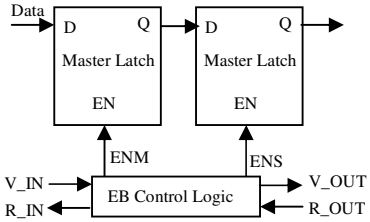

Figure: 3(b) Elastic buffer

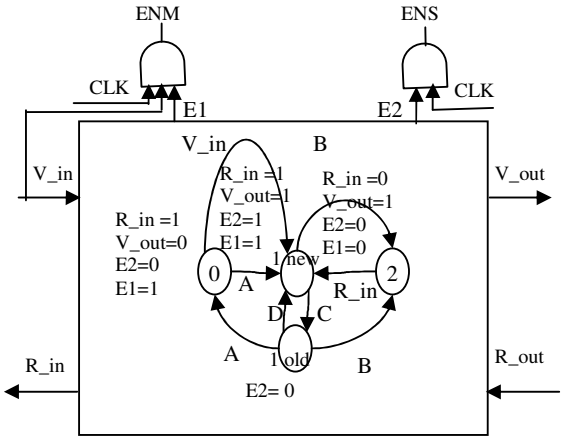

Figure: 3(c) FSM of EB Control Logic

Figure: 3(c) shows the expanded view of the EB control logic as a FSM for two-slot EBs.Elastic buffer works on the phenomenon of handshaking. EB channels feature provides multiple EBs to form a distributed FIFO.

4.1. Comparative Analysis

The comparison between the two routers is compared on the basis of parameters. The comparative table shown below in Table: 1

Table: 1 Comparison table between the baseline router and proposed router.

Parameters	Baseline Router	Proposed multicrossbar Router
Buffered	Buffered	Both buffered and buffer less
Number of crossbar used	One	Four
Type of Buffer	Virtual Channel	Elastic buffer
Handshaking	No	Yes
Probability of data lost	High	Negligible
Speed	Slow	Fast

5. SIMULATION AND RESULTS

Implementation is done in cadence virtuoso at 180nm.All the parameters are set at the time of simulation .The delay and average power is calculation is done. Delay of proposed router as compare to base line router is reduced to 51.37% % at the cost minimal increase in power as shown in Table 2 .This minimal increase in power is due to multicrossbar switches. The overall performance gets increases due to the reduction of PDP by 37. 91%.

Table 2 shows the comparison based on the delay and total average power and PDP.

Router Design	Delay(nsec)	Total average power(μW)	Power delay product(Femto watt sec)
Baseline Router	4.117	194.6	801.16
Proposed elastic buffer multicrossbar router	2.002	290.2	580.98

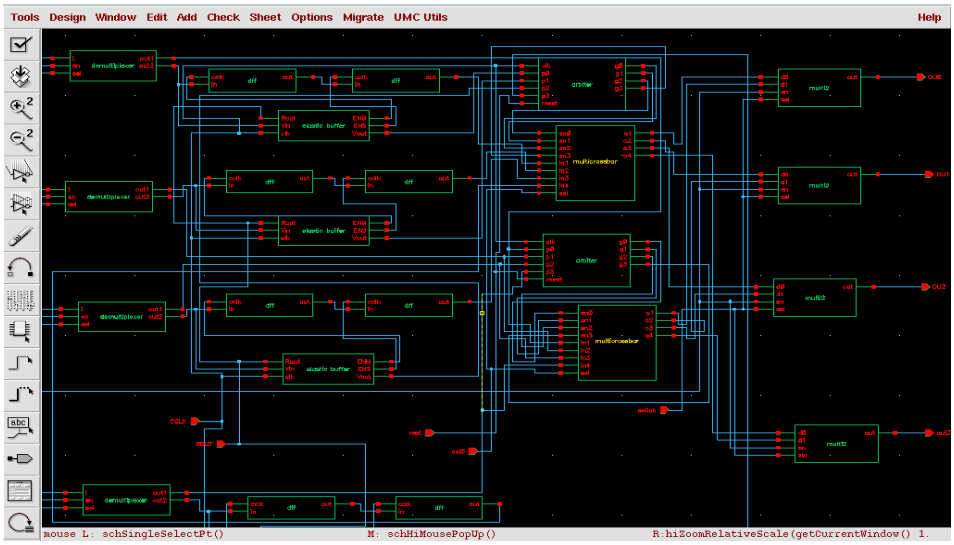

Figure: 4 Implemented Circuit of Proposed Router in Cadence

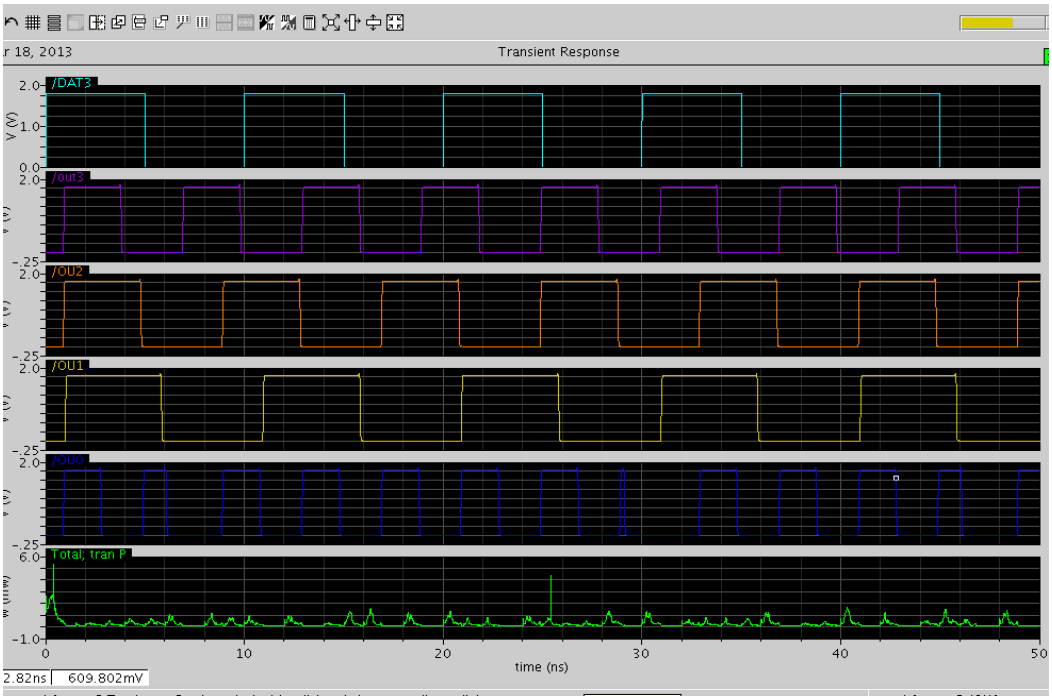

Figure: 5 Simulation of Proposed Router

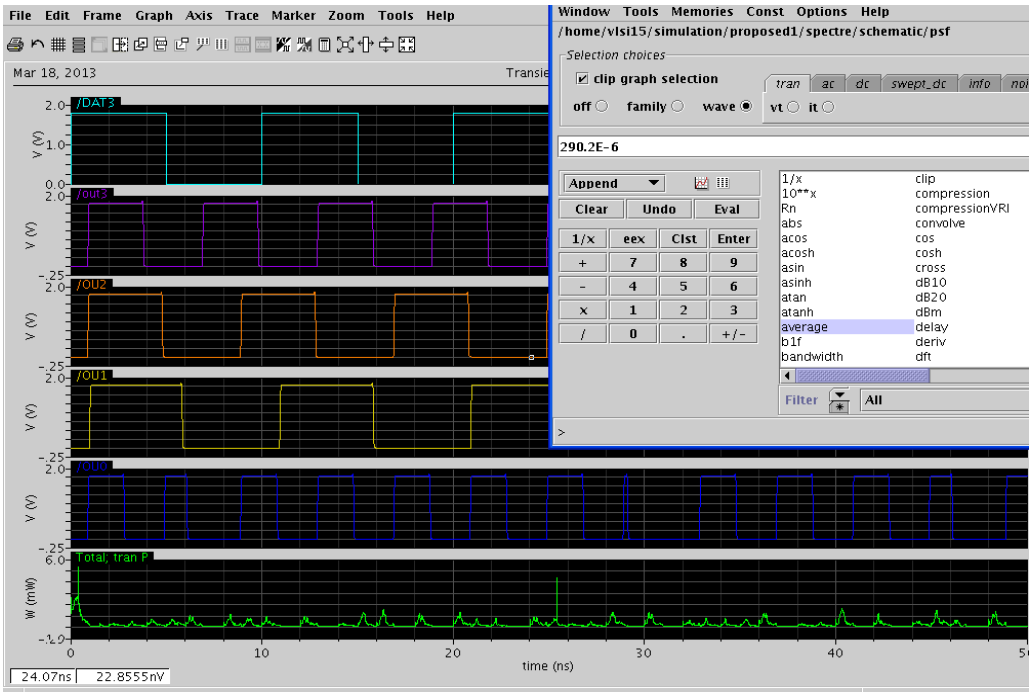

Figure: 6 Total power calculation of Proposed Router

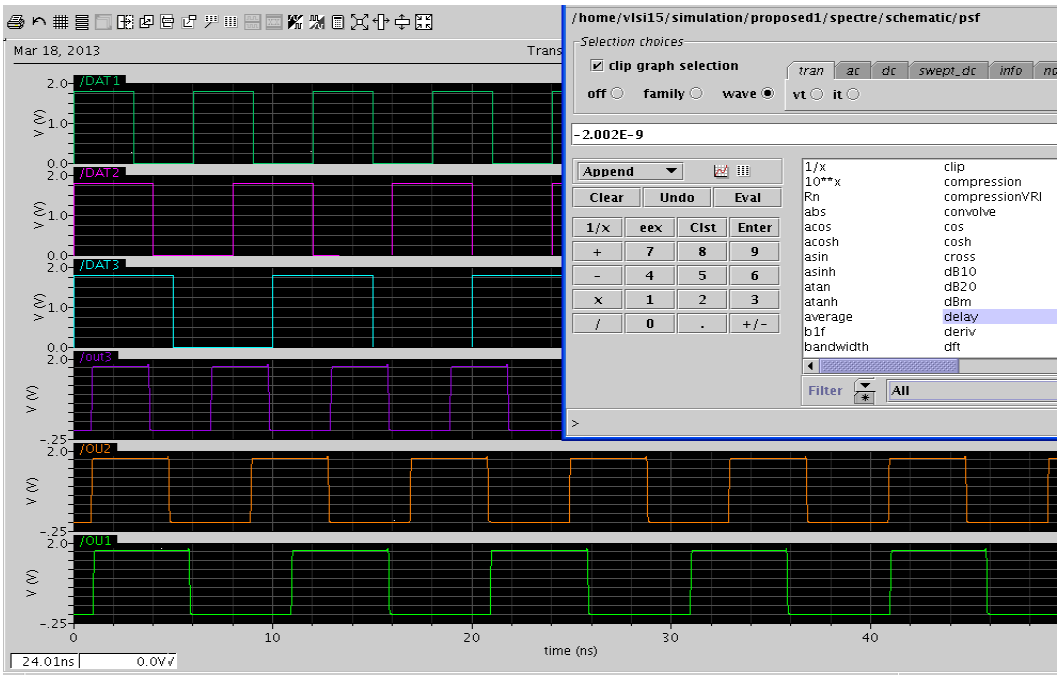

Figure: 7 Delay calculation of Proposed Router

6. CONCLUSION

In this paper we evaluate the performance of crossbar organization using multi cross bar router design using elastic buffer with an objective of reducing delay. The proposed design shows the power delay product reduction by 37.91% and delay reduction of 51.37% compare to baseline router design result in increase in performance. With the proposed design we conclude that the advantage of both buffered and buffer less is achieved. At low traffic flit traverse from the first multicrossbar and at high traffic flit traverse using elastic buffer via secondary multi-crossbar .In multi-crossbar configuration due to split of crossbars ,delay is reduced. Higher throughput is achieved due to selective merging of different output ports. Elastic buffer is enough to store a number of flit on each port with accuracy as it works on handshaking principle. It is concluded from the above discussion that proposed router design using multicrossbar provide better performance as compared to baseline router design.

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