DESIGN OF THREE BIT ANALOG-TO-DIGITAL CONVERTER (ADC) USING SPATIAL WAVE-FUNCTION SWITCHED (SWS) FETS

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ABSTRACT

The spatial wave-function switched field effect transistor (SWSFET) has two or three low band-gap quantum well channels inside the substrate of the semiconductor. Applied voltage at the gate region of the SWSFET, switches the charge carrier concentration in different channels from source to drain region. The switching of electron wave function in different channels can be explained by the device model of the SWSFET. A circuit model of SWSFET is developed in BSIM 4.0.0. The design of three bit analog-to-digital converter (ADC) using one three wells SWSFET is explained in this work. Analog-to-digital converter (ADC) circuit design using less number of SWSFET will reduce the device count in future analog and digital circuit design.

KEYWORDS

Spatial wave-function switched FET, Integrated circuit, VLSI, analog-to-digital converter (ADC), digital-to-analog Converter (DAC)

1. INTRODUCTION

Basic building block of any integrated circuit is metal-oxide-semiconductor field effect transistor (MOSFET) which acts as a switch based on the applied voltage in its gate terminal. The cross sectional schematic of a conventional MOSFET is shown in Fig. 1. The charge flow between the source and drain region of the MOSFET is controlled by the applied voltage in its gate terminal. The applied voltage in the gate terminal either enhances the channel formation or depletes the channel formation between the source and drain region of the MOSFET. The density and the performance of the MOSFET can be increased by decreasing it different parameters such as channel length, channel width, gate oxide thickness and other dimensions. Research is ongoing to improve MOSFET performance by controlling the different parameters like device structures [1-3], gate dielectric materials [4-6], substrate doping, and source-drain doping profile of the device.

But when the feature sizes approach towards nm range, one of the major challenge is the gate dielectric thickness which needs to be decreased to increase the gate capacitance and thereby the drive current and the device performance.

The gate dielectric thickness below 2 nm, increases the leakage currents due to the direct tunnelling of charge carriers which increases the power consumption and reduces device reliability [7-9]. Other major scaling issues besides the gate dielectric thickness are gate-channel interface states and surface charge doping fluctuations in the source and drain region, different kinds of short channel effects such channel length modulation, quantum confinement in the inversion layer etc. which deviates the transistor characteristics in the sub-nm range.

DOI : 10.5121/vlsic.2013.4301

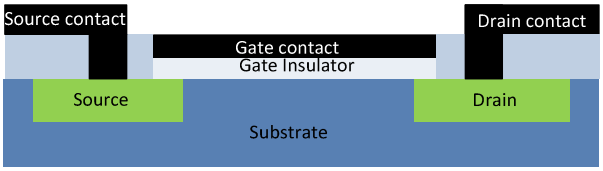
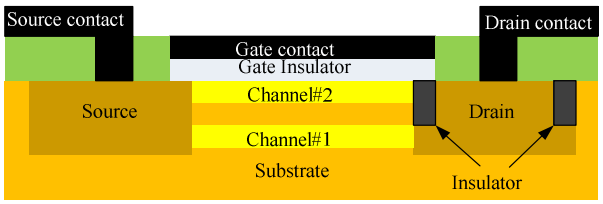
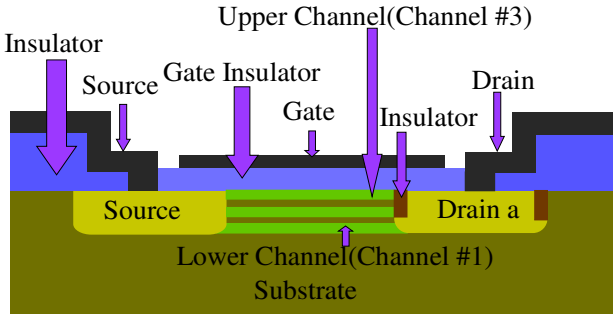


Figure 1: Cross-sectional schematic of conventional FET

The performance of integrated circuit can also be increased by only single polar based transistor circuit operation because of the high electron mobility of the charge carriers. In SWSFET, the charge population in the different channels depends on the applied voltage in its gate terminal [10]. In this work we have shown the design of three bit analog-to-digital converter (ADC) based on SWSFET. Before discussing the analog-to-digital converter (ADC), the SWSFET will be introduced in section II. The fabrication and theory of operation of SWSFET is discussed in brief in section III. The circuit model of SWSFET is discussed in section IV. The architecture of membership function using SWSFET is discussed in section V which is followed by conclusion in section VI.



(a)



(b)

Figure 2: Cross-sectional schematic of SWSFET (a) Two well (b) Three well

2. SPATIAL WAVE-FUNCTION SWITCHED FIELD EFFECT TRANSISTOR (SWSFET)

Spatial wave-function switched (SWS) FET is a field effect transistor where two or three separate low band gap channels are separated by a high band gap material between them. The cross sectional schematic of a two-channel SWSFET and a three-channel SWSFET are shown in Fig. 2. The applied gate voltage of a SWSFET switches the charge carrier concentration between the channels. Different channels are connected to two different drain terminals. Current flows through different drain terminals based on the applied voltage in its gate terminal. Three bit

analog-to-digital converter (ADC) can be designed by using one three well SWSFET which is the minimum number of circuit elements than the existing any other architecture. The high electron mobility of SWSFET also makes this circuit faster than the CMOS based conventional circuit architecture.

3. FABRICATION AND THEORY OF OPERATION

Metalorganic chemical vapor deposition (MOCVD) growth of the InGaAs-AlInAs three quantum- well structure on a p-InGaAs/p-InP wafer was the first step for substrate formation of the SWSFET structure, which was followed by the selective regrowth of an n+- InGaAs layer to form the source and drain regions.

The formation of source and drain regions was followed by the opening of the gate region. This is followed by epitaxial growth of II–VI gate insulators. on the InGaAs top well layer using photo-assisted metalorganic chemical vapor deposition (MOCVD).

Multiple-layer stack of ZnSe-ZnSZnMgS using ultraviolet (UV) radiation was deposited to form the gate insulator. The first layer (serving as the buffer) was a ZnSe layer. This layer was grown for 30 s with dimethylzinc (DMZn) and dimethylselenide (DMSe) growing a buffer layer of ZnSe (as thin as possible).

This was followed by the formation of another stack layer of ZnS/ZnMgS/ZnS/ZnSe using MOCVD technique.

The source - drain contact was formed using Gold-Arsenic following annealing in N_2 environment at 300^oC. Finally aluminum metal gate was formed on top of the gate region of the transistor.

The energy band-diagram of a two well SWSFET is schematically shown in Fig. 3. The charge flows in a SWSFET through different channels based on the applied gate voltage. When the gate voltage is low but above the threshold voltage (V_{TH1}) of the device, charge carriers are confined in the lower quantum well channel and flows from source to drain region. As the gate voltage is increased (V_{TH2}), charge carriers transfer from the lower channel to the upper quantum well channel and current flows through the upper channel of the device. Based on the applied gate voltage, the electron concentration as well as the electron wave function switches from one channel to the other and current flows through different drain terminals. Fig. 4 shows the electron wave-function switching between different quantum well channels in the SWSFET when the gate voltage increases gradually from (a) to (b). Fig. 5 shows the charge density variations in different channels with respect to gate voltage.

Fig. 6 shows the capacitance-voltage (C-V) characteristics of a fabricated two quantum well channel InGaAs-AlInAs SWSFET [10-13]. The C-V curves show distinct peak before the accumulation regime (gate voltage less than -2V) where the capacitance becomes constant. The capacitance of the SWS device reaches to first maximum value at a gate voltage ~ -1 V. This occurs when electrons are in the lower quantum well channel (channel#1). When the gate voltage is increased further, electrons are transferred from the first quantum well layer (channel#1) to the second quantum well layer (channel #2). The capacitance decreases as the carriers are in the proximity of gate until total inversion is reached. The detailed device operation is already published elsewhere [10-13].

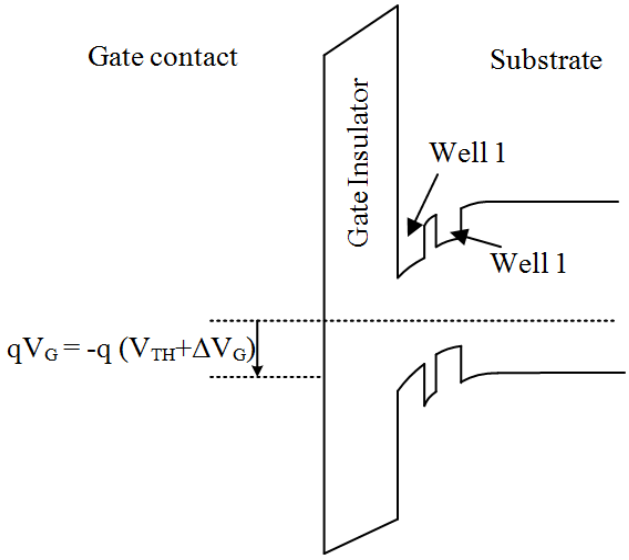
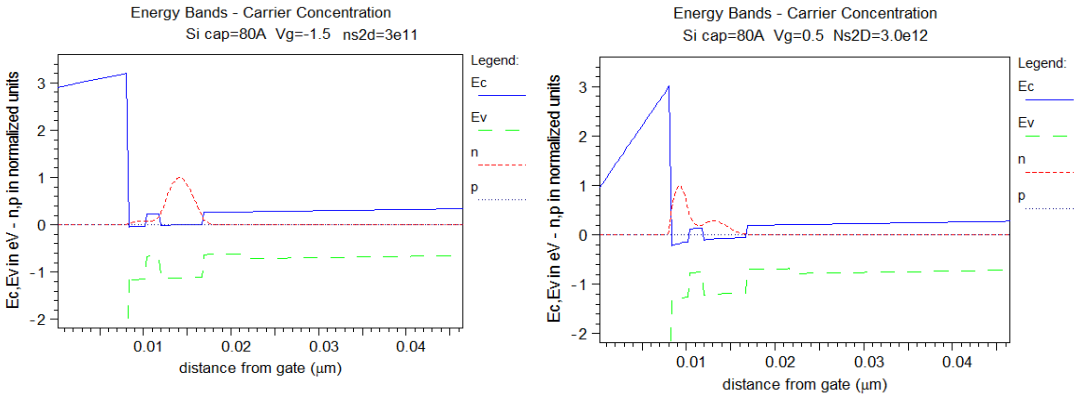


Figure 3: Energy band diagram of SWSFET



(a) (b)

Figure 4: Device simulation for two well SWSFET [13]

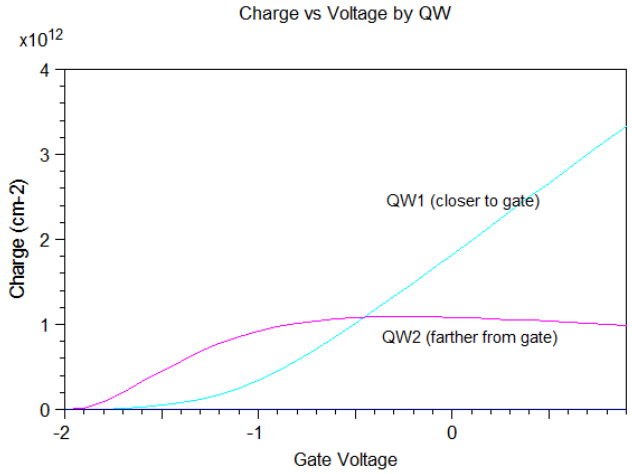


Figure 5: Transfer characteristics from device simulation [13]

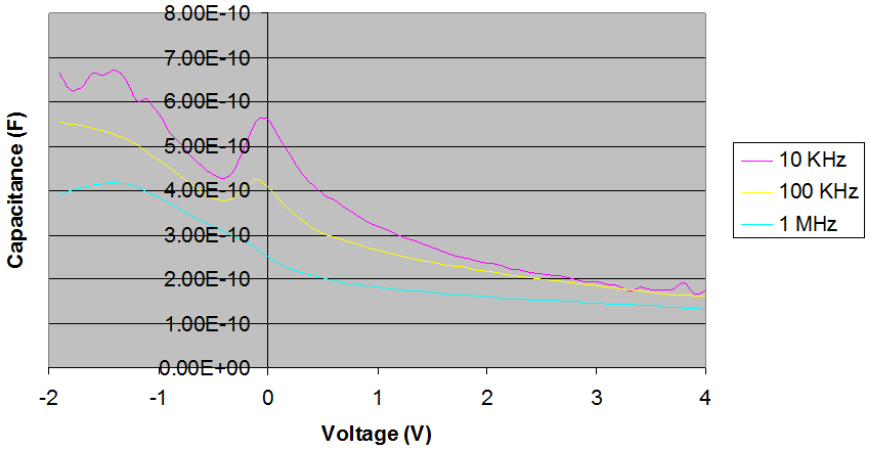


Figure 6: C-V characteristics of SWSFET [13]

Figure 7 shows the transfer of electron wave function in a three well SWSFET based on the applied gate voltage. Based on the applied gate voltage, the electron wave function switches between different channels and the drain current flows through different drai terminals. The transfer characteristics of a three well SWSFET is shown in Fig.8.

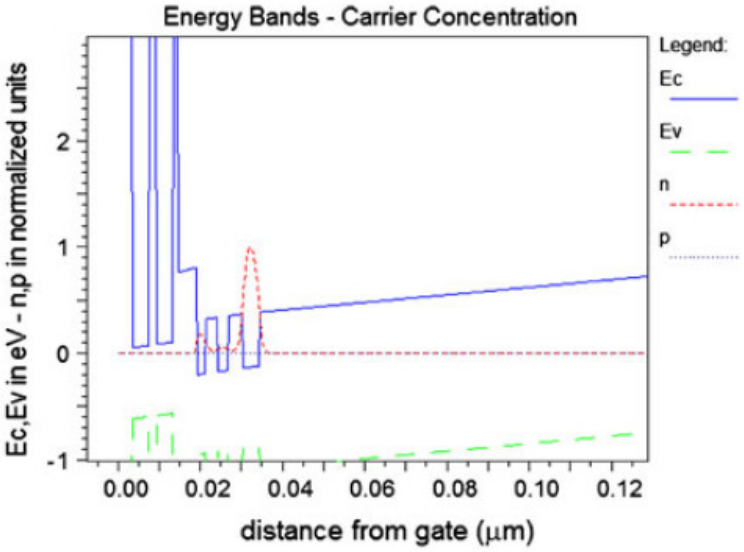


Figure 7: Device simulation for three well SWSFET [10]

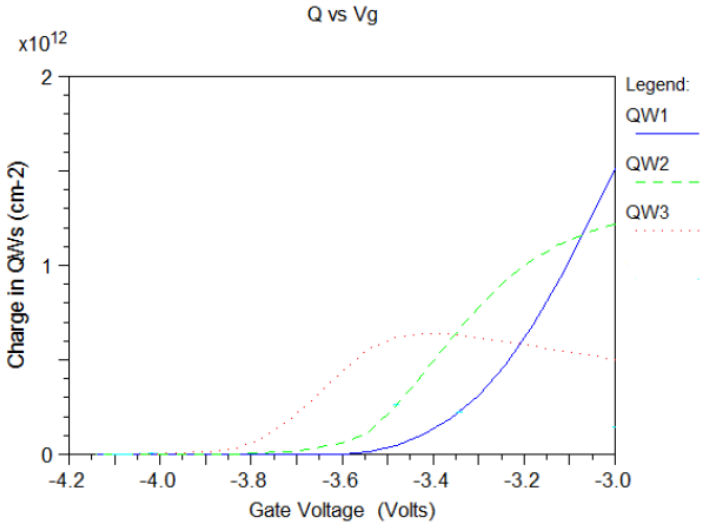


Figure 8: Transfer characteristics of a three well SWSFET from device simulation

4. SWSFET CIRCUIT MODEL

In this model the amount of charge in the different channels of the SWSFET is represented with the current level in through different channels. In three well SWSFET, we consider channel#3 as the channel which is further from the gate, and channel#1, which is closest to the gate. Channel#2 is in between these two.

Figure 9 shows the I_{DS}-V_{GS} characteristics of a three well SWSFET. Channel #3 turn on first, then Channel#2 and Channel#1 respectively. The charge transfer occurs from bulk semiconductor to the channel#3 first, then from channel#3 to channel#2 and channel#2 to channel#1. So initially in channel#3, current increases after threshold voltage corresponding to that channel, and then it reaches maximum value. Channel#2 turn on based on two mechanism: one based on its threshold

voltage, accumulation of charge in this channel and tunnelling of carriers from channel #3 to channel#2. The maximum value on current in channel#3 is the mutual effect of charge population in channel#3 because of charge accumulation from bulk semiconductor and tunnelling to channel#2.

Similar explanation is true for channel#2. Here charge population is corresponding to three effects: tunnelling from channel#3, accumulation of charge from bulk semiconductor and tunnelling to channel#1. Channel#1 behaves like a inversion channel in conventional FET, only difference is charge accumulation effect. Here additional charge accumulation is due to charge tunnelling form channel#2.

Different circuit model parameters are shown in Table 1.

The threshold voltage in channel 'a' can be expressed as

$V_{tha} = V_{tha}$ when $V_{GSeff} < V_{qL}$ (a)

$V_{tha} = V_{tha} + \alpha(V_{GSeff} - V_{qL})$ when $V_{GSeff} > V_{qL}$ (b)

where α is a matching parameter and

$$\alpha = \frac{\left(V_{GSeff} - V_{qL}\right)}{\left(V_{q1} - V_{qL}\right)} \quad \text{(c)}$$

Simmilarly the threshold voltage in channel 'b' can be expressed as

$V_{thb} = V_{thb}$ when $V_{GSeff} < V_{q2}$ (d) (1)

$V_{thb} = V_{thb} + \beta(V_{GSeff} - V_{q2})$ when $V_{GSeff} > V_{q2}$ (e)

where β is a matching parameter and

$$\beta = \frac{\left(V_{GSeff} - V_{q2}\right)}{\left(V_{qH} - V_{q2}\right)} \quad \text{(f)}$$

The threshold voltage in channel 'c' can be expressed as

$V_{thc} = V_{thc}$ when $V_{GSeff} < V_{qH}$ (g)

Voltage across the polysilicon gate can be expressed as

$$V_{Poly} = \frac{q\varepsilon_s n_{gate} C_{OX}^2 10^6}{2}\left[\sqrt{1 + \frac{2\left(V_{GS} - V_{FB} - 2\varphi_f\right)}{q\varepsilon_s n_{gate} C_{OX}^2 10^6}} - 1\right]^2 \quad \text{(h)}$$

Since the voltage across the poly-silicon gate does not exceed the silicon bandgap voltage, the effective voltage across the poly-silicon gate is

$$V_{PolyEff} = 1.12 - 0.5\left(1.12 - V_{Poly} - \delta + \sqrt{\left(1.12 - V_{Poly} - \delta\right)^2 + 4.\delta.(1.12)}\right) \quad \text{(i)}$$

The effective gate voltage can be expressed as

$$V_{GSeff} = V_{GS} - V_{PolyEff} \quad \text{(j)}$$

where

n_{gate} is the poly silicon gate doping concentrations

V_{qL} is the transition voltage

V_{q1} is the voltage corresponding to peak current in channel 3.

V_{q2} is the transition voltage
V_{qH} is the voltage corresponding to peak current in channel 2
V_{tha} is the threshold voltage of the channel 3
V_{thb} is the threshold voltage of the upper channel 2
V_{thc} is the threshold voltage of the upper channel 1
α is a matching parameter
V_{GS} is the gate-source voltage
V_{GSeff} is the effective gate-source voltage
$V_{PolyEff}$ is the voltage drop in the Poly Si gate
C_{OX} is the gate capacitance
V_{FB} is the flat band voltage
Φ_f is the surface potential
q is the electron charge
$\delta = 0.01$ is the parameter for DC V_{DSeff}
ϵ_s is the permittivity

The drain current

$$I_{DS} = \left(\frac{W}{L}\right) C_{OX} \mu_n \left[(V_{GS} - V_{tha}) V_{DS} - \frac{V_{DS}^2}{2} \right] \quad (2)$$

Table 1

SWSFET parameters

Parameter	Value
Minimum L	5.0 µm
Minimum W	10 µm
V_{tha}	0.2 V
V_{thb}	0.7 V
V_{thc}	2.25 V
V_{qL}	0.6 V
V_{q1}	1.5 V
V_{q2}	2.0 V
V_{qH}	2.5 V
V_{DD}	3.0 V

5. ANALOG-TO-DIGITAL CONVERTER (ADC)

The threshold voltages of three channels of SWSFET are different. Based on the input voltages, different channels of the FET conduct for different input voltages.

Based on this charge transfer concept different channel has different amount of accumulated charge based of gate voltage. When gate voltage is below the threshold voltage of the channel#3(further from gate), no charge accumulation, the three well SWSFET is off, no current in output.

State assignment concept sequence is as (channel#1 channel#2 channel#3). In the OFF state of the FET, all channels are OFF and assignment of that state is (000) [0]. When some charge accumulated in channel#3 and channel#2 is off, that state is assigned as (001) [1]. When charge tunnelling starts from channel#3 to channel#2, channel#2 starts to conduct, get some current in

channel#2 as well as channel#3. Initially channel#3 charge is more, more current corresponding to this channel than channel#2, this state is assigned as (011^{+}) [2]. When gate voltage increases, charge carriers tunnel more from channel#3 to channel#2, sometimes, channel#3 current will be less than channel#2, that state is assigned as ($01^{+}1$) [3]. Gradually, channel#3 will be empty of charge, all charge will be in channel#2 at some point, and in this gate voltage range, only conducting channel is channel#2. This state is assigned as (010) [4]. For more gate voltage, tunnelling of charge carriers from channel#2 to channel#1 will start and channel#1 will start to conduct. Based on the same concept between channel#3 and channel#2, different states are assigned as ($11^{+}0$) [5], ($1^{+}10$) [6] and (100) [7].

Figure 9 shows the transfer characteristics from the model of three state SWSFET and assignment of different states with the current levels of different channels of the FET.

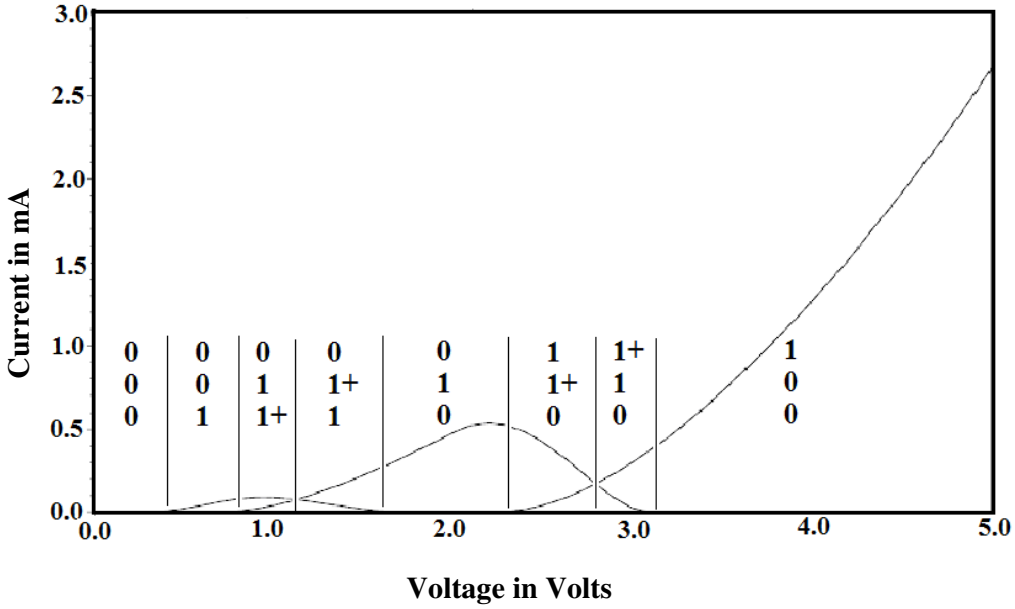


Figure 9: Assignment of different states I_{DS}-V_{GS} (Transfer) Characteristics of triple FET

To identify the current levels in different channels, MOS inverter is used in the output of each channel. Each channel is connected to the input of two comparator circuits of different threshold voltages. The high threshold voltage comparator represents 1^{+} state, because it turns on at higher reference voltage (for higher current level). Low threshold voltage comparator represents 1 state.

This step is equivalent to quantization of analog signal for analog-to-digital conversion. The block diagram of the ADC circuit based on three well SWSFET is shown in Fig. 10.

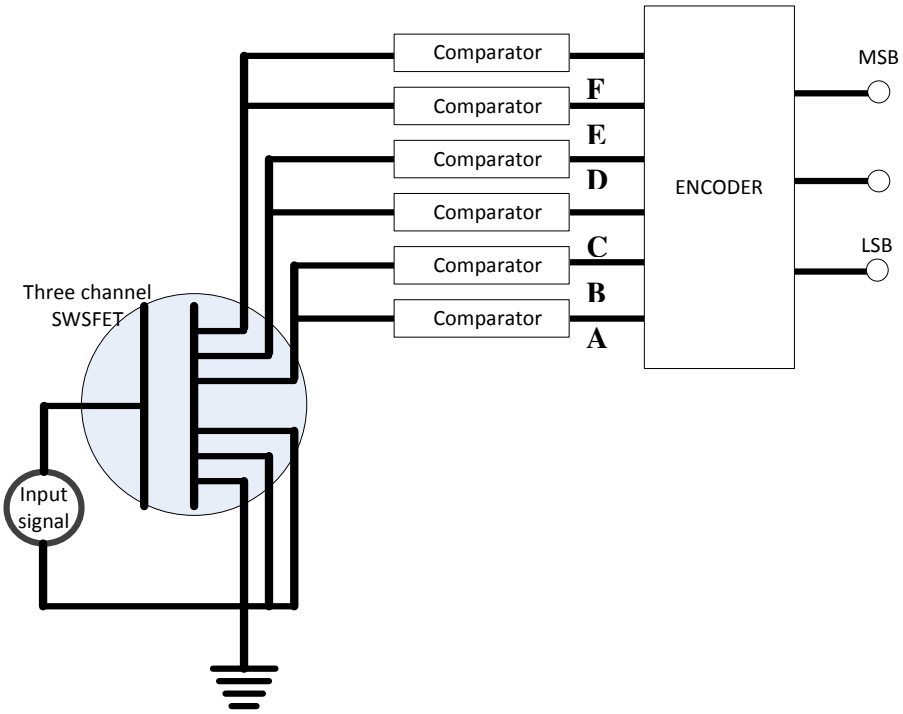


Figure 10: Circuit diagram of analog-to-digital converter (ADC)

The encoder circuit comprised of a code converter and encoder. The code converter converts different quantized input to different codes in three bit logic system.

The code converter activates anyone of 0-7 outputs at a time based on the A-F input waveforms combination. Table 2 and table 3 represent this design.

The outputs show that, at a time only one output active, which represent the combination of different channel charge status which depends on the input analog voltage applied in the gate of the device.

The code converter is followed by the encoder. The encoder is designed based on the table 4. The encoder design is shown in Fig. 11.

Table 2

A	B	C	D	E	F	Activated output
0	0	0	0	0	0	0
1	0	0	0	0	0	1
1	1	Don't care	0	0	0	2
0	0	1	Don't care	0	0	3
0	0	1	1	0	0	4
0	0	1	1	1	0	5
0	0	1	Don't care	1	1	6
0	0	0	0	1	1	7

Table 3

Activated output	Input Combination based on Table#1
0	$\overline{A}.\overline{B}.\overline{C}.\overline{D}.\overline{E}.\overline{F}$
1	$A.\overline{B}.\overline{C}.\overline{D}.\overline{E}.\overline{F}$
2	$A.B.(C+\overline{C}).\overline{D}.\overline{E}.\overline{F}$
3	$A.\overline{B}.C.(D+\overline{D}).\overline{E}.\overline{F}$
4	$\overline{A}.\overline{B}.C.D.\overline{E}.\overline{F}$
5	$\overline{A}.\overline{B}.C.D.E.\overline{F}$
6	$\overline{A}.\overline{B}.C.(D+\overline{D}).E.F$
7	$\overline{A}.\overline{B}.\overline{C}.\overline{D}.E.F$

Table 4

Input to encoder	**MSB**	**Central**	**LSB**
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

So MSB = 4 + 5 + 6 +7
Central = 2 + 3 + 6 +7
LSB = 1 + 3 + 5 + 7

Figure 11 shows the corresponding circuit implementation.

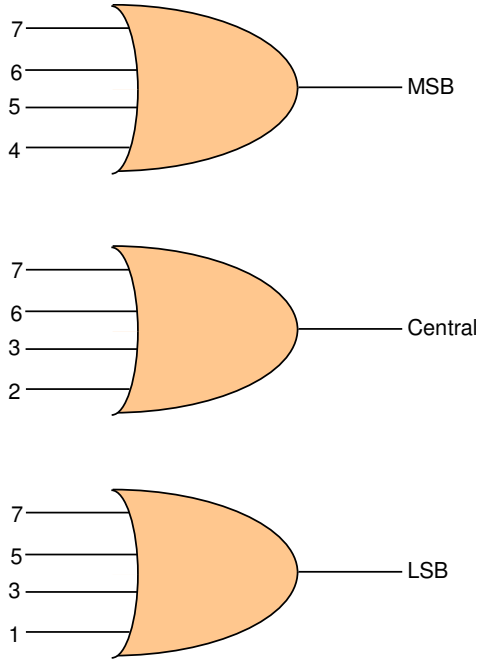


Figure 11: Encoder Circuit diagram

The final Analog-to-Digital (ADC) output and input combination is shown in Figure 12. The tabular form of ADC output is shown in Table 5.

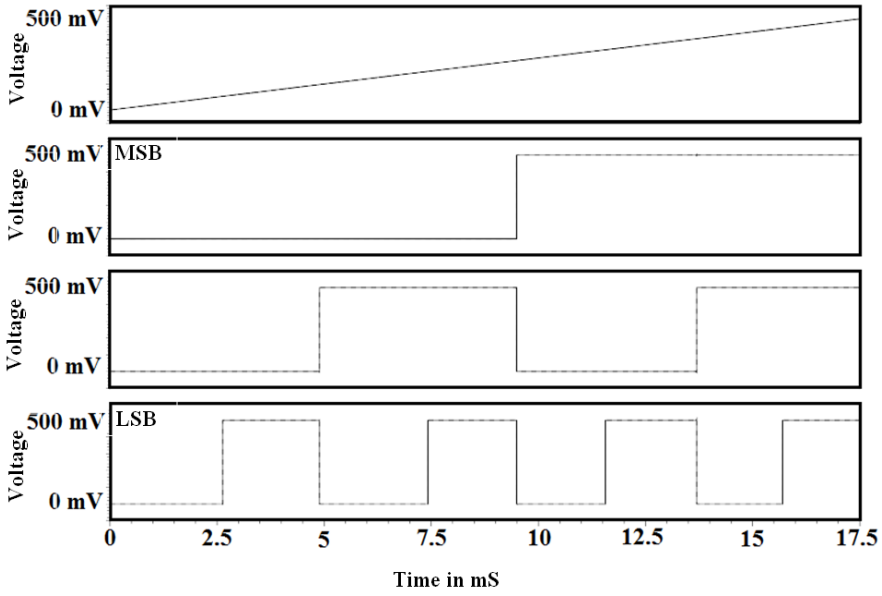


Figure 12: Input and output waveform of the designed Analog-to-Digital converter

Table 5

Analog input voltage (mV)	MSB	Central	LSB
0 – 62.5	0	0	0
62.5 – 135.0	0	0	1
135.0 – 197.5	0	1	0
197.5 – 260.0	0	1	1
260.0 – 312.5	1	0	0
312.5 – 375.0	1	0	1
375.0 – 437.5	1	1	0
437.5 – 500.0	1	1	1

6. CONCLUSION

In this paper the design of analog-to-digital converter based on spatial wave function switched field effect transistor (SWSFET) is shown. The SWSFET can be fabricated using conventional CMOS process. The basic advantage of using SWSFET is the number of circuit elements. Single SWSFET based three bit ADC will give minimum device count for this circuit design. The number of circuit element to design ADC circuit is reduced a lot compared to conventional CMOS architecture. The SWSFET generally fabricated in InGaAs material systems. Because of their higher electron mobility SWSFET based circuits are faster than other. The implementation of three bit ADC using less number of circuit elements will make SWSFET a promising circuit element in future communication circuit design.

ACKNOWLEDGEMENTS

Discussions with Prof. Faquir C. Jain and Dr. John A. Chandy, Dept. of Electrical and Computer Engineering, University of Connecticut, Storrs, CT, are gratefully acknowledged.

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