

CROSSTALK MINIMIZATION FOR COUPLED RLC INTERCONNECTS USING BIDIRECTIONAL BUFFER AND SHIELD INSERTION

Damanpreet Kaur and V.Sulochana

Centre for Development of Advanced Computing (C-DAC) Mohali, India
damannrng@gmail.com, vemus@cdac.in

ABSTRACT

Crosstalk noise is often induced in long interconnects running parallel to each other. There is a need to minimize the effect of these crosstalk noise so as to maintain the signal integrity in interconnects. In this paper crosstalk noise is minimized using various techniques such as repeater (bidirectional buffer) insertion along with shielding, skewing and shielding & skewing simultaneously. With the help of these techniques crosstalk noise is controlled to a great extent in long interconnects. Pre-layout and Post-layout simulations for crosstalk are carried out for these techniques at 180nm technology node using Cadence EDA tools. The influences of these techniques are analyzed and it is found that crosstalk is reduced up to 32 % with repeater insertion, 47% with skewing, 58% with shielding and 81% with skewing & shielding simultaneously.

KEYWORDS

Crosstalk, Bidirectional Buffer, Shielding, Skewing.

1. INTRODUCTION

The feature size of integrated circuits has been reduced in the search of enhanced speed, power, silicon area and cost characteristics [1]. Semiconductor technologies with feature sizes of several tens of nanometers are currently in progress. As per, International Technology Roadmap for Semiconductors (ITRS), the future nanometer scale circuits will contain large number of transistors on single chip and operate at clock speeds well over high frequencies. Distributing robust and reliable power, ground and other control signals through interconnects in such a high-speed, high-complexity.

Environment is quite a challenging task. The performance of a high-speed chip is dependent on interconnects, which connect different cells within a VLSI chip. With ever-growing length of interconnects and frequency in a chip, the effects of interconnects cannot be constrained to RC models alone. The importance of on-chip inductance is continuously increasing and the introduction of new materials for low resistance interconnects is in progress. Now a days interconnect delay dominates gate delay in current deep sub micrometer VLSI circuits [2]. With the continuous scaling of technology and increased die area, this behavior is expected to continue. Wide wires are frequently found in global and semi-global interconnects in upper metallic layers. These wires are low resistive lines that can have significant inductive effects. Owing to presence

of these inductive effects, the new generation VLSI designers have been forced to model interconnects as distributed RLC models [3]. These RLC line when running parallel to each other have capacitive coupling, which makes the design of interconnects even more important in terms of crosstalk. Many of the research work have been aimed at reducing delay and power dissipation only [4]. Crosstalk noise effects have not been given generally much concern. In a modern interconnect design, interconnects in an adjacent metal layers are tried to keep orthogonal to each other. This is done to reduce crosstalk as much as possible. But with growing interconnect density and reduced chip size, even the non-adjacent interconnects exhibit significant coupling effects.

The impact of this has made on chip's performance of concern in today's design era. The effect of crosstalk induced overshoot generated at a noise-site. The peak overshoot generated at a noise-site can wear out the thin gate oxide layer resulting in permanent failure of the chip [5]. This problem will be noteworthy as the feature size of transistor reduces with advancement of technology. Drawing out exact values of capacitance and inductance induced noise for an interconnect is a very challenging task. For an on-chip interconnect, the different performance of capacitive noise must be taken into consideration. As we know electrostatic interaction between wires is of very short range, consideration of only nearest interconnects provides sufficient accuracy for capacitive coupled noise.

General methods for reducing the effects of crosstalk include bus encoding [6–9], wire spacing adjustments [10], buffer insertion [11], and shielding [12]. In this paper buffer insertion, skewing, shielding and skewing & shielding simultaneously has been considered for minimizing crosstalk.

1.1 Repeater Insertion

Uniform repeater insertion is an efficient technique for driving long interconnects. Uniform repeater insertion technique divides the interconnect into equal sections and make use of equal size repeaters to drive each section [5]. The primary objective of a uniform repeater insertion system is to minimize the time for a signal to propagate through a long interconnect. In this paper it is revealed that inserting repeaters, other than fulfilling its primary goal reduces crosstalk levels also.

1.2 Skewing

In this paper crosstalk is reduced using system resource that is time. Time or timing slack has been previously used in buses [13, 14], where the delay of a coupled bus was reduced by intentionally skewing the timing of adjacent wires. Skewing was applied to reduce the energy dissipation of a coupled bus [15] and was used to reduce bus peak power [16]. In this crosstalk voltage induced on quiet victim wires is reduced as proposed in [17].

1.3 Shielding

Shield insertion is an effective method to reduce crosstalk noise and signal delay uncertainty and has become common practice when routing critical signal and power lines [18]. Inserting shield lines can greatly reduce capacitive coupling [19] by providing a closer current return path for both the interconnect lines.

The remainder of the paper is organized as follows. Section II provides present work implementing crosstalk reduction techniques and discusses obtained results. Finally, conclusions are drawn.

2. RELATED WORK

Tianpei Zhang *et.al*[11] presents a method for incorporating crosstalk reduction criteria into global routing under a broad power supply network paradigm. This method utilizes power/ground wires as shields between signal wires to reduce capacitive coupling, while considering the constraints imposed by limited routing and buffering resources. An iterative procedure is employed to route signal wires, assign supply shields, and insert buffers so that both buffer/routing capacity and signal integrity goals are met. In each iteration, shield assignment and buffer insertion are considered simultaneously via a dynamic programming-like approach. Noise calculations are based on Devgan's metric, and the work demonstrates, for the first time, that this metric shows good fidelity on average. An effective noise margin inflation technique is also proposed to compensate for the pessimism of Devgan's metric. Experimental results on test cases with up to about 10 000 nets point towards an asymptotic runtime that increases linearly with the number of nets.

Gargi Khanna and Rajeevan Chandel[20] analyzes the effects of aggressor-line load variations (both active gate and passive capacitive loads) on the nonideal effects of a coupled VLSI-interconnect system. Signal delay, power dissipation and crosstalk noise in interconnect can be influenced by variation in load of another interconnect which is coupled to it. For active gate and passive capacitive load variations, such effects are studied through SPICE simulations of a coupled interconnect pair in a 0.13mm technology. Crosstalk between a coupled pair, is affected by transition time of the coupled signal, interconnect length, distance between interconnects, size of driver and receiver, pattern of input, direction of flow of signal and clock skew. In this work, influence of aggressor-line load variations (both active gate and passive capacitive loads) on the non-ideal effects of delay, power consumption and crosstalk in a victim-line of a coupled VLSI-interconnect system are determined through SPICE simulation. In this experiment, the victim line is terminated by a fixed capacitive load and the coupled to aggressor line has variable load, either passive capacitive or active gate. Distributed RLC transmission model of interconnect is considered for the SPICE simulations.

3. PRESENT WORK AND ANALYSIS

In this paper RLC interconnect model as in Figure 1. is used to study the effect of crosstalk. RLC parameter values are obtained from ptm models $R= 36.666\text{ohms}$, $L= 1.8358\text{nH}$ and $C=82.932\text{fF}$.

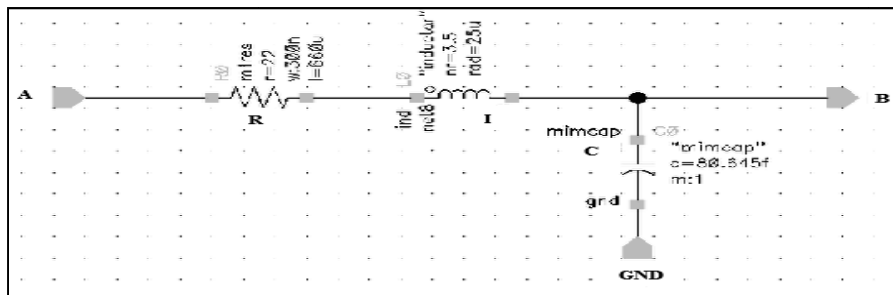


Figure1. RLC interconnect model

RLC interconnect model analysis has been done and simulation results at 1GHz are shown in Figure 2. It is observed that at 1GHz signal is distorted which may lead to degradation of signal. So there is a need to maintain the signal integrity which is done using repeater insertion.

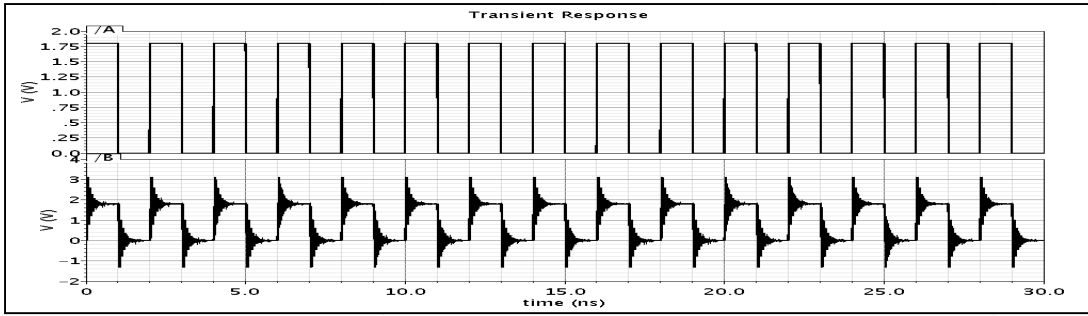


Figure 2 .RLC interconnect simulations at 180nm

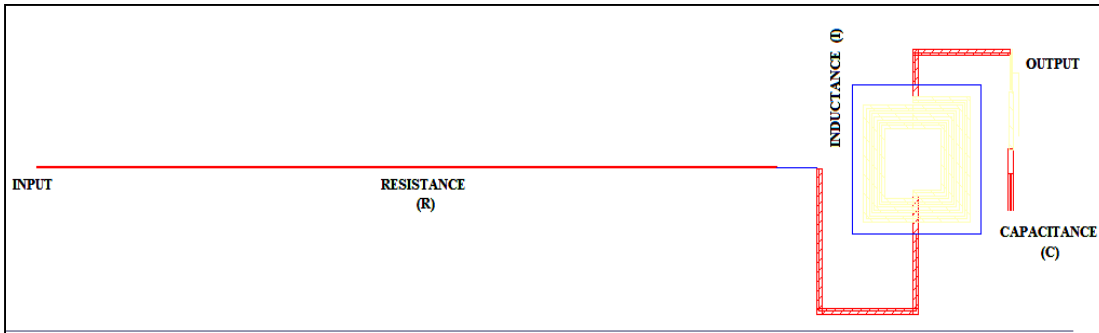


Figure 3. RLC interconnect model layout

Bidirectional buffers are used in programmable logic devices for amplifying a signal on a line wherein signal flow may be in either direction on line [20]. In this paper Bidirectional buffer is designed as a repeater in RLC interconnects. This bidirectional buffer is made up of tri-state buffers and invertors. Control input pin decides the direction of signal flow as in Table 1.

Table 1. Bidirectional Buffer direction

Control	Direction of bidirectional buffer
1	A to B
0	B to A

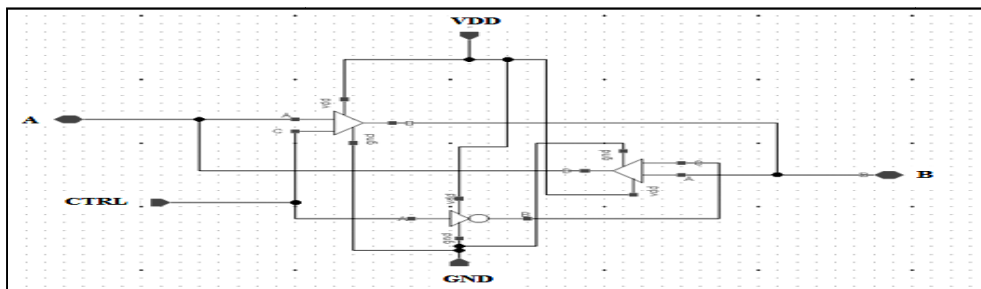


Figure 4. Bidirectional buffer using tristate buffers and invertors

In Figure 4. Bidirectional Buffer is designed as a repeater at 1GHz in both directions as per input to control signal. Figure 5. shows when control is high signal flows from A to B and Figure 6. shows when control is low signal flows from B to A in bidirectional buffer.

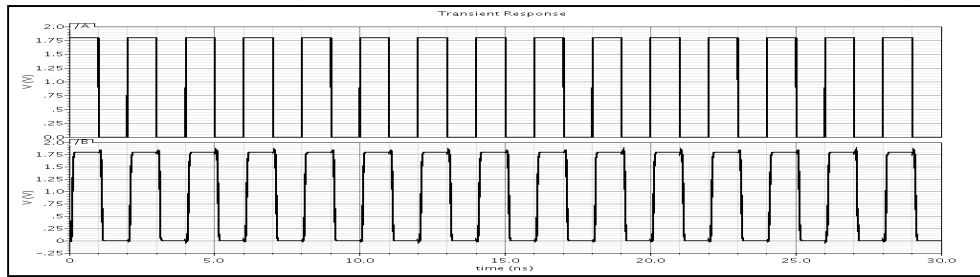


Figure 5. Bidirectional Buffer from A to B

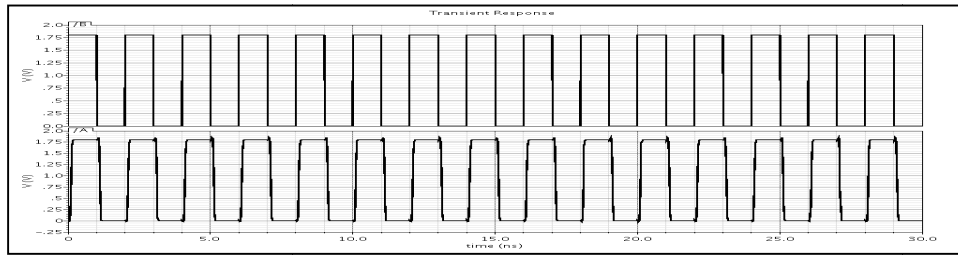


Figure 6. Bidirectional Buffer from B to A

In Figure 7, bidirectional buffer is designed and is inserted as repeater in RLC interconnect model. Ctrl pin determines the condition of signal flow either from A to B or vice versa.

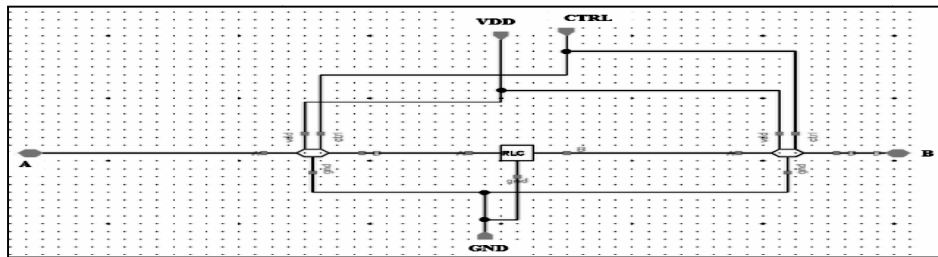


Figure 7. Bidirectional buffer insertion in interconnects

Figure 8. shows the layout of buffer insertion in interconnects at 180nm. Bidirectional buffer are placed at extreme ends with RLC in between them. VDD supply and GND pins are shown in layout.

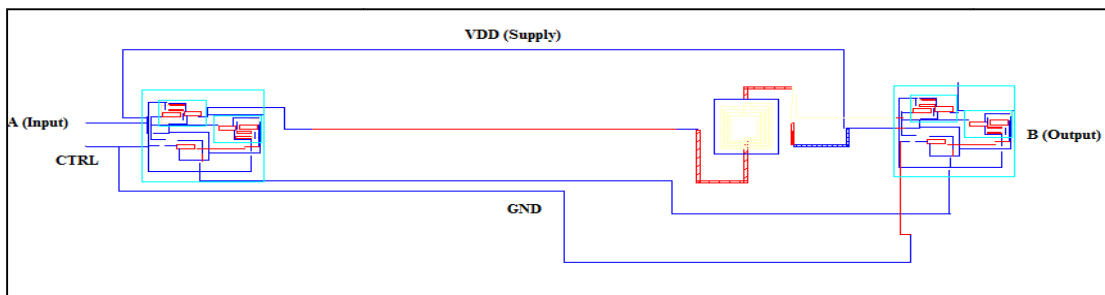


Figure 8. Layout of Bidirectional buffer insertion in interconnects

Transient analysis of this bidirectional buffer is inserted in RLC interconnect model obtained is as in Figure 9. It is observed in Figure 9. that with buffer insertion in RLC signal has restored to great extent.

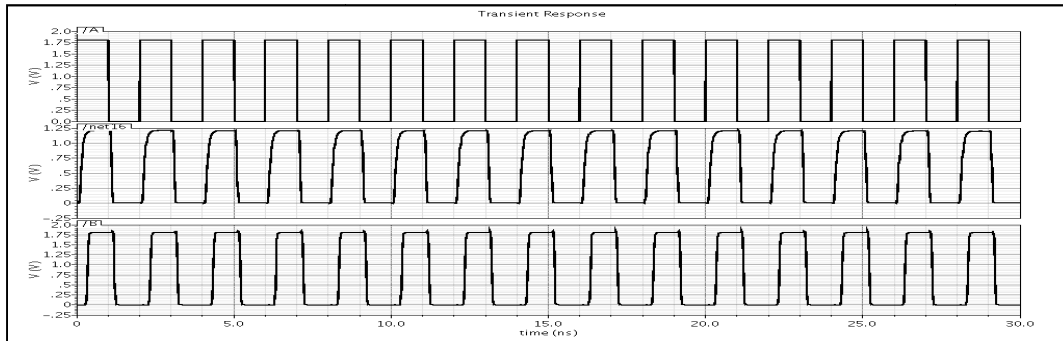


Figure 9 . Bidirectional Buffer insertion in interconnects

Two parallel interconnect lines are considered along with coupling capacitances to study the effect of crosstalk in interconnects as in Figure 10. Value of coupling capacitance as per ptm model is chosen to be 88.37fF. The crosstalk is measured with these circuits with voltage sources switching in same and in opposite directions at the receiving buffer input node being referred to as critical node in terms of crosstalk.

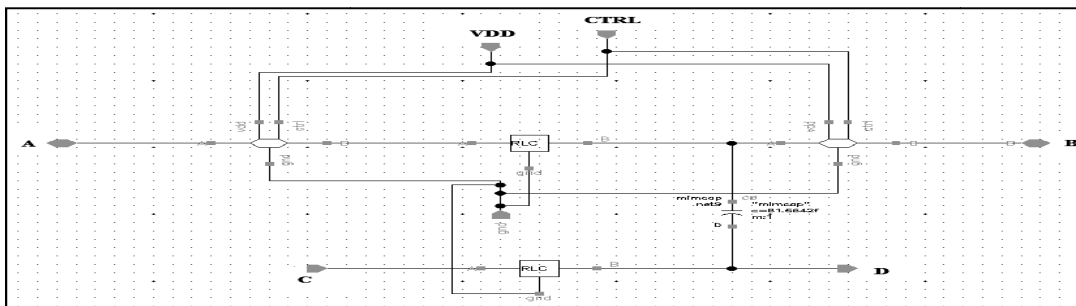


Figure 10. Coupling in interconnects

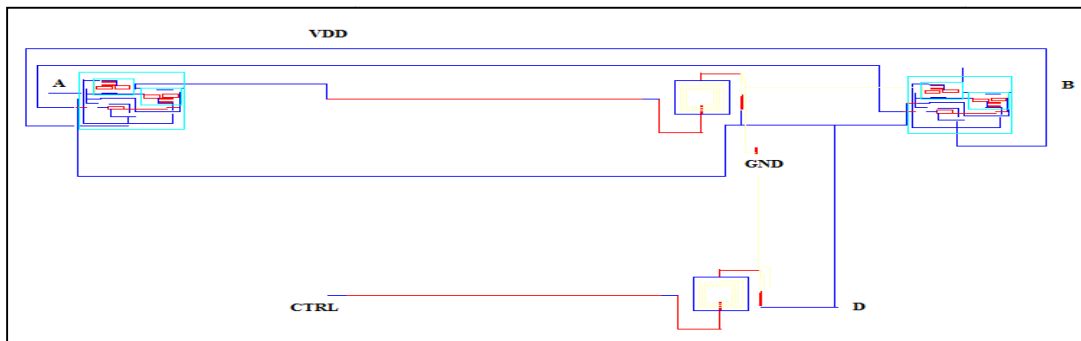


Figure 11. Layout depicting coupling in interconnects

Due to coupling capacitance crosstalk is observed at the input of receiver driver. It is found that when there is switching of voltage drivers in same direction crosstalk observed is less and when they are switching in opposite directions crosstalk observed is more.

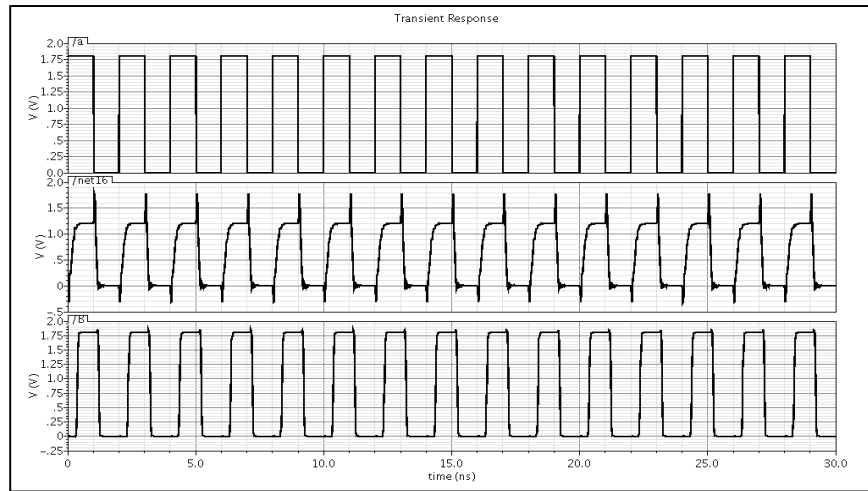


Figure 12. Coupling in interconnects

Crosstalk induced in circuits due to adjacent interconnects may distort the original signal so it is undesirable in circuits. To minimize this crosstalk minimization technique such as shielding is implemented in Figure 13. In this ground lines are placed around the victim lines so as to reduce the crosstalk by providing a closer current return path for both the interconnect lines.

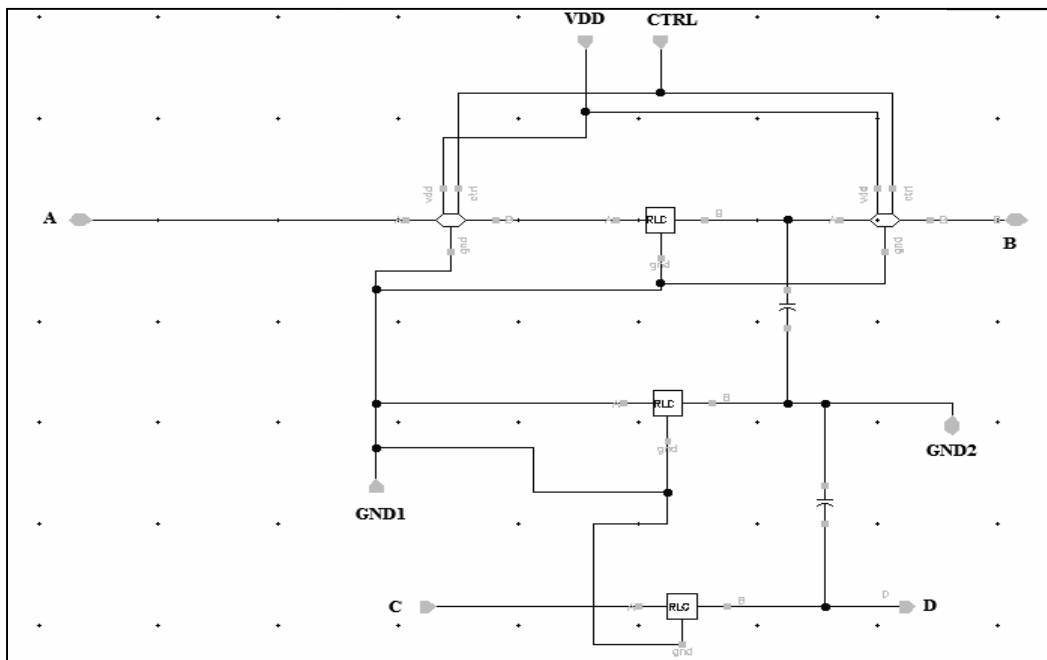


Figure 13. Shielding in interconnects

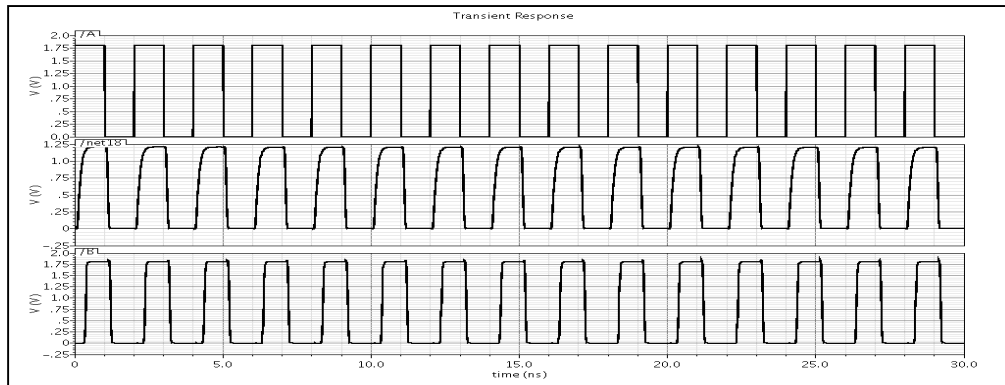


Figure 14. Shielding technique in interconnects

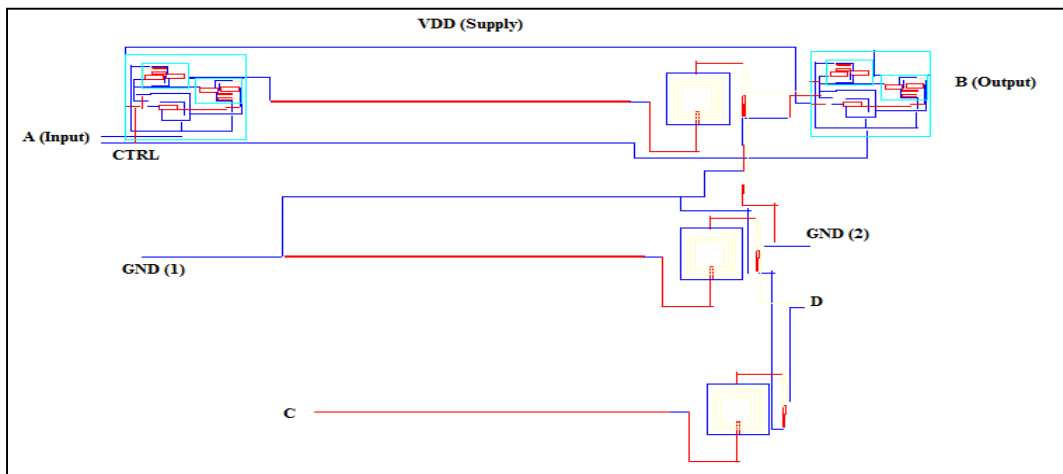


Figure 15. Shielding in interconnects layout

Skewing, one of the technique to reduce crosstalk is also implemented. In this delay time of 500ps is inserted, so that delay is introduced between the switching times of the drivers which may lead to reduction of crosstalk.

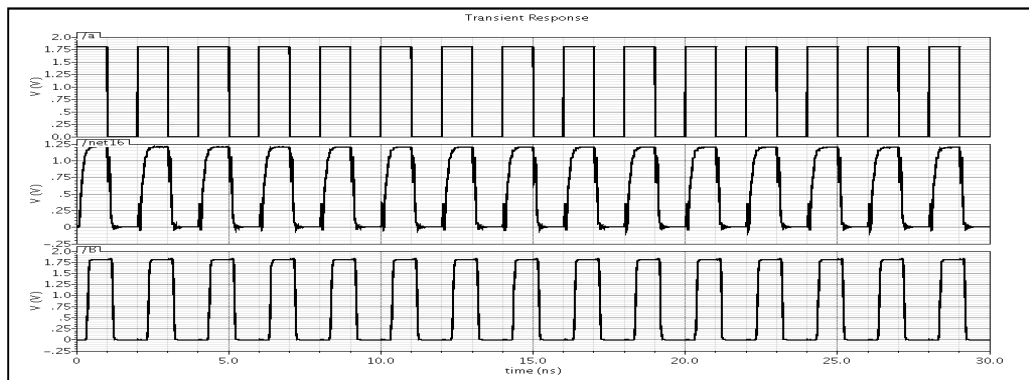


Figure 16. Skewing technique in interconnects

Further crosstalk reduction is implemented using both skewing and shielding techniques simultaneously in by inserting delay time of 500ps in Figure 13. It is observed that crosstalk is reduced maximum in this case.

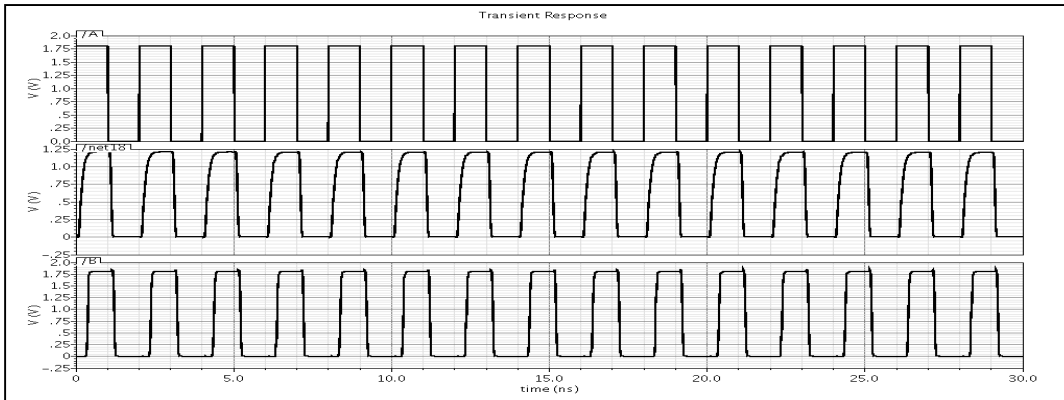


Figure 17. Shielding and skewing simultaneously technique in interconnects

Techniques such as skewing, shielding and skewing & shielding simultaneously reduces the crosstalk. The maxima of the signal is calculated at critical node and crosstalk values at prelayout and postlayout simulations are as shown in Table 2.

TABLE 2. Crosstalk values at different techniques

Direction of bidirectional buffer	Layout	Switching direction	RLC coupling	shielding	skewing	Skewing & shielding	
A to B	Pre-layout	same	1.270 V	1.210V	1.196V	1.166V	
		opposite	1.607V	1.212V	1.26V	1.169V	
B to A		Same	1.270V	1.210V	1.196V	1.164V	
		opposite	1.607V	1.212V	1.259V	1.169V	
A to B		Post-layout	Same	1.282 V	1.213V	1.201V	1.168V
			Opposite	1.794V	1.214V	1.214V	1.172V
B to A	Same		1.282V	1.213V	1.201V	1.168V	
	opposite		1.794V	1.214V	1.214V	1.172V.	

4. CONCLUSIONS

In order to reduce crosstalk noise, bidirectional buffer operating at 1 GHz frequency is proposed along with buffer insertion and various techniques such as shielding, skewing so as to reduce the crosstalk noise. The proposed buffer also helped to reduce delay. It was observed that crosstalk noise is effectively reduced with these techniques and delay is reduced by 34% with buffer insertion. Thus through the various results obtained using cadence at 180 nm technology node crosstalk is analyzed and reduced through different techniques up to 32% with repeater insertion, 47% with skewing, 58% with shielding and 81% with skewing & shielding simultaneously.

5. FUTURE DEVELOPMENT OF THIS WORK AND APPLICATION AREAS

Crosstalk minimization techniques can be implemented in SOC (system on chip) circuits. Crosstalk degrades the signal integrity which is not desirable for reliable VLSI circuits. Since logic of the signal must be maintained for functionality of various analog and digital circuits so its necessary to reduce the effect of crosstalks due to interconnects on ICs.

ACKNOWLEDGEMENTS

We would like to extend a special thanks to C-DAC Mohali for providing us means to carry out our research work in meticulous way. We are also grateful to MHRD, Govt of india for providing us a platform to do our research work.

REFERENCES

- [1] Rabaey, J.M. (1996), *Digital Integrated Circuits, A Design Perspective*, Prentice-Hall, Englewood Cliffs, NJ
- [2] Sakurai, T. (1983), "Approximation of wiring delay in MOSFET LSI", *IEEE J. Solid-State Circuits*, Vol. SC-18, pp. 418-26
- [3] Ismail, Y.I., Friedman, E.G. and Neves, J.L. (1999), "Figures of merit to characterize the importance of on-chip inductance", *IEEE Trans. on VLSI Sys.*, Vol. 7, pp. 442-9
- [4] Bakoglu, H.B. and Meindl, J.D. (1985), "Optimal interconnection circuits for VLSI", *IEEE Trans Electron Devices*, Vol. ED-32, pp. 903-9.
- [5] Banerjee, K. and Mehrotra, A. (2001), "Accurate analysis of on-chip inductance effects and implications for optimal repeater insertion and technology scaling", *Proc. IEEE Symp. VLSI Circuits*, Kyoto, Japan, pp. 195-8.
- [6] Victor, B., Keutzer, K.: 'Bus encoding to prevent crosstalk delay'. *Proc. IEEE Int. Conf. on Computer-Aided Design*, 2001, pp. 57-63
- [7] Lyuh, C.-G., Kim, T.: 'Low-power bus encoding with crosstalk delay elimination', *IEE Proc. Comput. Digit. Tech.*, 2006, 153, (2), pp. 93-100
- [8] Khan, Z., Arslan, T., Erdogan, A.T.: 'Low power system on chip bus encoding scheme with crosstalk noise reduction capability', *IEE Proc. Comput. Digit. Tech.*, 2006, 153, (2), pp. 101-108

- [9] Lampropoulos, M., Al-Hashimi, B.M., Rosinger, P.: 'Minimization of crosstalk noise, delay and power using a modified bus invert technique'. Proc. Design, Automation and Test in Europe, 2004, pp. 1372–1373
- [10] Macii, E., Poncino, M., Salerno, S.: 'Combining wire swapping and spacing for low-power deep-submicron buses'. Proc. ACM GLSVLSI, April 2003, pp. 198–202
- [11] Zhang, T., Sapatnekar, S.S.: 'Simultaneous shield and buffer insertion for crosstalk noise reduction in global routing', IEEE Trans. Very Large Scale Integr. (VLSI) Syst., 2007, 15, (6), pp. 624–636
- [12] Zhang, J., Friedman, E.G.: 'Effect of shield insertion on reducing crosstalk noise between coupled interconnects'. Proc. Int. Symp. On Circuits and Systems, 2004, pp. 529–532
- [13] Hirose, K., Yasuura, H.: 'A bus delay reduction technique considering crosstalk'. Proc. Design, Automation and Test in Europe, 2000, pp. 441–445
- [14] Ghoneima, M., Ismail, Y.I., Khellah, M.M., Tschanz, J.W., De, V. 'Reducing the effective coupling capacitance in buses using threshold voltage adjustment techniques', IEEE Trans. Circuits Syst. I, Regul. Pap., 2006, 53, (9), pp. 1928–1933
- [15] Ghoneima, M., Ismail, Y.I.: 'Utilizing the effect of relative delay on energy dissipation in low-power on-chip buses', IEEE Trans. Very Large Scale Integr. (VLSI) Syst., 2004, 12, (12), pp. 1348–1359
- [16] Lee, Y.M., Park, K.H.: 'Mesochronous bus for reducing peak I/O power dissipation', IEE Electron. Lett., 2001, 37, (5), pp. 278–279
- [17] Liljeberg, P., Tuominen, J., Tuuna, S., Plosila, J., Isoaho, J.: 'Self-timed approach for noise reduction in NoC. In Interconnect-centric design for advanced SoC and NoC' (Kluwer Academic Publishers, 2004), pp. 285–313.
- [18] P. Saxena and S. Gupta, "On integrating power and signal routing for shield count minimization in congested regions," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 22, no. 2, pp. 437–445, Apr. 2003.
- [19] J. Zhang and E. G. Friedman, "Crosstalk noise model for shielded interconnects in VLSI-based circuits," in Proc. IEEE Int. SOC Conf., 2003, pp. 243–244
- [20] Gargi Khanna and Rajeevan Chandel "Analysis of non ideal effects in coupled VLSI interconnects with active and passive load variations" Microelectronics international 26/1(2009).
- [21] Sridhar Krishnamurthy, Shekhar Bapat, "Programmably bidirectional buffered interconnect circuit", United States patent, Patent no. 5,844,424, January 1998

Authors

Damanpreet Kaur is pursuing Masters of Technology at C-DAC Mohali in VLSI Design. She has obtained her Bachelor of Engineering degree in Electronics & Communication Engineering from Punjab technical University, Jalandhar in 2011. Her research interests include Digital & Analog VLSI Design. Her email-id is damannrng@gmail.com.



Vemu Sulochana has obtained her Bachelor of Technology degree from JNTU Kakinada and Master of Technology degree from NIT, Hamirpur in 2004 and 2009 respectively. In 2011, she joined C-DAC, Mohali to conduct innovative research in the area of VLSI design, where she is now a Project Engineer - II. Her research is concerned with low power VLSI design, Design of high speed VLSI interconnects. She is conducting research in IC interconnect characterization, modeling and simulation for the high speed VLSI circuit design. Her email-id is vemus@cdac.in

