DESIGN OF A PROGRAMMABLE LOW POWER LOW DROP-OUT REGULATOR

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ABSTRACT

A low power programmable low drop-out regulator capable of providing 1V output has been proposed. The regulator requires a supply voltage of 1.2V and works in the temperature range of -40 to 125 °C in nominal corner (i.e, normal doping for PMOS and NMOS Field Effect Transistors), yielding a load regulation of 3%. The output voltage level is controlled externally by means of 2 1-bit control signals. The circuit provides a DC gain of 30 dB and a maximum DC Power Supply Rejection Ratio of -35 dB and a worst case PSRR of -20 dB. Power dissipation in the load is nearly 100 μ W.

Keywords

Low Drop-Out, Voltage Regulator, Low Power, Low quiescent current.

1. INTRODUCTION

With the advent of low power battery-operated circuits, demanding special emphasis on compactness and portability, it has become imperative to optimize existing low drop-out regulator structures for greater all-round performance. Low drop-out regulators are circuits designed to provide a specified, stable DC voltage, with a low input-to-output voltage difference. The drop-out voltage of a regulator is defined as that value of differential voltage at which regulation provided by the control loop stops. Typically, an LDO is characterized by performance metrics such as drop-out voltage, line regulation, load regulation, power supply rejection ratio, tolerance over temperature, ESR(equivalent series resistance) range, output capacitance, variation in voltage due to transient current set up and quiescent and maximum load currents.[1] LDOs today have become ubiquitous as mobile battery operated products ranging from cellular phones to laptops require them. Today's LDO's must meet demands of low operating voltages and low quiescent currents as a consequence of the higher packing densities that process technology demands.

Perhaps the biggest challenge incumbent on the engineer with regards to design lies in the tradeoff between loop gain, a necessary parameter to accomplish optimal load and line regulation, and bringing the dominant pole (which in this case, is the pole at the output node) below the unity gain frequency to achieve a desirable phase margin that satisfies the stability condition. For polezero cancellation to occur at low frequencies, an output capacitor with high ESR(equivalent series resistance) must be used, which poses the danger of degraded transient response Also, leakage currents significantly increase when operating voltages are substantially increased, and rise in temperatures have a hindering effect on loop gain due to thermal leakages. Minimization of dropout voltages is essential for maximizing dynamic range within a given power supply voltage,

owing to the fact that signal to noise ratio decreases with decrease in power supply voltages as noise is typically a constant phenomenon.

To combat these effects, an LDO design has been proposed that utilises a pole-zero cancellation scheme for compensation, and a cascode current amplifier together with a large, high threshold PMOS operated in the sub-threshold region, which is responsible for boosting the gain and yielding the desired output voltage. The LDO is programmable and offers a range of four different voltages, by means of the two binary-input control signals at its input. The entire circuit has been designed in a 65 nm process and simulated using Cadence Tool.

2. ANALYSIS OF CONVENTIONAL LDO

Low-drop out regulators are one of the most conventional applications of operational amplifiers. Figure1 shows the basic topology. A voltage reference is used with the op-amp to generate a regulated voltage, V_{reg} . If the voltage reference is stable with temperature, the fact that the Vreg is a function of a ratio of resistors (so process or temperature changes in the resistance value don't affect the ratio) and the variation in the op-amp's open loop gain is desensitized using feedback makes the regulated voltage stable with process and temperature changes. The ideal (meaning that the op-amp has infinite open-loop gain) regulated voltage is [2]



Figure 1: Conventional Low Drop-Out Regulator

$$Vreg = Vref \cdot \left(1 + \frac{R_1}{R_2}\right) \tag{1}$$

If the op-amp's open-loop gain is finite, then we can write [2]

$$Vreg = Ao1. (vp - vm)$$
 (2)

$$vm = Vreg. \frac{R2}{R1 + R2}$$
 and $vp = Vref$ (3)

Solving for the actual regulated voltage, gives

$$Vreg = Vref. \frac{1}{\frac{1}{Ao1} + \frac{R2}{R1 + R2}}$$
 (4)

which implies that the equation simplifies to equation 1 for very large values of A_{o1} .

The drop out voltage of a regulator depends on the switch ON resistance (Ron) and is given by the formula [1]

$$V \, drop - out = I \, load \, \times R \, on \tag{5}$$

Typical drop-out voltages range from a minimum of 100mV to as high as a volt. This variation in the output voltage with change in input voltage is termed as line regulation. Load regulation is defined as variation in the output voltage due to the presence of a load. It is expressed as [1]

$$Ro = \frac{\Delta Vreg}{\Delta Iout} = \frac{Ro - pass}{1 + Av\beta}$$
(6)

where Ro is the output impedance of the circuit, ΔV reg and ΔI out are the changes in regulated output voltage and the load current respectively. R_{o-pass} is the output resistance of the pass transistor. Av is the open-loop gain of the system and β is the feedback factor. As can be seen from this equation, a high-open loop gain and low output impedance are influential factors in determining the transient response of an LDO. In addition, a high (W/L) ratio of the pass element, which results in a low output resistance, is required.

The temperature dependence of the output voltage is a function of the input offset voltage of the error amplifier and the drift in the voltage reference with changes in temperature. Accuracy of the system, may hence be defined as [1]

$$Accuracy = \frac{Vo, max - Vo, min}{Vo}$$
(7)

where Vo is the input offset voltage of the error amplifier. Offset voltage of the error amplifier can be minimized by increasing the open-loop gain of the system, which translates to a higher transconductance of the differential pair.

The efficiency of an LDO is limited by the quiescent current in the system, and may be expressed as [1],

$$Efficiency = \frac{IoutVreg}{(Iout + Iquiscent)Vin}$$
(8)

where Vin is the input voltage.

The open loop gain of the system is given by the equation [1]

$$\frac{Vfb}{Vref} = |Av| = \frac{gma \times Roa \times gmp \times Z}{1 + sRoaCpar} \cdot \frac{R1}{R1 + R2}$$
(9)

where g_{ma} and g_{mp} are the transconductances of the amplifier and the pass element respectively, R_{oa} is the output resistance of the amplifier, C_{par} is the parasitic capacitance due to the pass element and Z is the output impedance seen when looking into the output node, V_{fb} is the feedback voltage to the error amplifier.

3. PROPOSED REGULATOR ARCHITECTURE

In the conventional architecture of an LDO, it is assumed that the error amplifier, by virtue of its large gain and resistive feedback, desensitizes variations in the gain so that a stable regulated voltage output is obtained. In our architecture, a current-sourcing PMOS in the output stage has been introduced. It is required that the PMOS be pulled all the way to ground so as to be biased further into saturation region. For this reason, the existing topology is modified and a Common-Source Stage is added, with the amplifying device being large enough so as to be a strong pull-down device. The Common-Source stage is responsible for enhancing signal swing and boosting

the gain at the op-amp output, subsequently pulling the gate of the large PMOS low enough to increase its gate-to-source voltage.

Programmability has been added to the LDO by means of two external control signals which appear at the gate inputs of two NMOS transistors. The binary input that appears at the gate is responsible for bringing in that resistance into the circuit, by biasing the transistor in saturation or triode region, thereby controlling the output voltage.

Binary Input	Output Voltage
00	1.025
01	1
10	0.975
11	0.95

Table 1: Range of Output Voltages



Figure 2: Schematic of proposed regulator

The proposed architecture consists of the following stages:

- 1. Error Amplifier
- 2. Common Source Amplifier
- 3. Current-sourcing PMOS

3.1. Error Amplifier

A high gain operational amplifier is used as the error amplifier [5], with a stable voltage reference fed to one of its inputs. The voltage reference is usually derived from a bandgap reference circuit. The differential pair of the operational amplifier consists of a current mirror NMOS load and a PMOS tail current source, with the gate-drain connected load being driven by a 2.5 uA ideal current source. A current mirror load has the advantage of providing high output impedance, and consequently, high gain. An operational amplifier connected with this sort of load is termed an open-transconductance amplifier, where all nodes are low impedance nodes with the exception of

the differential pair[2]. The resistive feedback provided to the negative input of the error amplifier works in a way as to balance the amplifier, minimizing op-amp offset.

3.2. Common-Source Amplifier

In general, a source follower is used as the buffer stage in most LDO's. The gain of a source follower is given by the formula [2],

$$\frac{Vout}{Vin} = \frac{resistance connected to the source}{resistance connected to the source + resistance looking into the source}$$
(10)

i.e,

$$\frac{Vout}{Vin} = \frac{gm1}{gm2} \tag{11}$$

where gm1 and gm2 are the transconductances of the amplifying device and load, respectively.

which implies that the source follower has asymmetric current driving capability, and gain less than one. Hence a common-source amplifier is used, which has a small signal gain equal to

$$Av = gm(ro1 || ro2) \tag{12}$$

where g_m is the transconductance of the amplifying device, r_{o1} and r_{o2} are the output resistances of the load and the amplifying device.

The equation implies that when the amplifying device (in our case, the NMOS) is made large enough, the gain at the second stage is improved. Proper sizing of the NMOS also ensures that it acts as a strong pull down, yielding rail-to-rail swing.

3.3. Current-Sourcing PMOS

The sizing of the current-sourcing PMOS is the most vital part of the entire design. PFETs are known to have poor current driving capability, as a result of which a large-size PMOS is required. In our design, a PMOS with high voltage threshold (of upto 540 mV in slow corner) has been used. The question arises as to why a lower voltage threshold PMOS was not chosen, which might have provided the advantage of lesser area. Low-voltage threshold FETs are known to contribute to leakage currents, increasing power dissipation in the device. The PMOS is responsible for quick charging and discharging of the output node, thereby increasing slew rate to obtain faster settling times.

4. COMPENSATION METHOD

The load is driven by an external capacitor, which is made large enough so that it can quickly charge the load during fast transients. However, the size of the capacitor is limited by the following constraints: the charging capability, the slew rate and the phase margin. Unlike most architectures where the dominant pole lies at the first node, here the dominant pole occurs at the output node as a result of which the external capacitor must be used as the compensation capacitor. Hence there is a lower limit on the size of the capacitor. However, for effective charging of the output node a large capacitor is necessary, but not too large that the output response becomes sluggish and the load transient is very slow. A large capacitor can also lead to poor load regulation.

The three poles can be characterized by the equations below[6]:

$$p1 = \frac{1}{CextResr}$$
 (13),

$$p2 = \frac{1}{Ceff1Reff1}$$
 (14)

$$p3 = \frac{1}{Ceff2Reff2}$$
 (15).

where p1 is the pole at the output stage, p2 is the pole at the second gain stage and p3 is the pole at the first gain stage. The compensation is achieved by means of a pole-zero frequency cancellation scheme [3], where a zero resistor is introduced at the output of the second gain stage. The value of the capacitance must be chosen so that the pole formed at the second gain stage lies well beyond the unity-gain bandwidth of the regulator. The capacitance also serves the purpose of fast recovery in large-signal conditions. When the regulated voltage output drops suddenly, the decrease in voltage is fed back directly to the gate of the PMOS. This causes the PMOS to turn on quicker, enabling it to pull up the output node. However, this capacitance might pose the disadvantage of pushing the pole associated with the output node to a higher frequency, if not properly sized, leading to instability.

5. SIMULATION RESULTS

Simulations have been carried out using the Cadence tool. The LDO yields a typical (nominal corner, 65°C) gain of 31 dB and a worst case (slow corner, 125 °C) gain of 27 dB, with a phase margin of 72°.



Figure 3: Gain-frequency curve of the regulator at -40°, 65° and 125°C.

Gain in the slow corner (lightly doped NMOS and PMOS) is lower due to the higher threshold voltages in this corner, because of the lower conductivities the doping levels introduce. Subsequently, the gate-to-source voltage at the input of the pass element might not be sufficiently higher than the threshold voltage, and the pass element is at risk of entering the sub-threshold region. As a result, the pass element behaves as a linear element, with a higher drain-to-source drop, reducing the output voltage, and hence, the gain.



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Figure 4: Phase response of the regulator at -40°, 65° and 125°C.



Figure 5: Power supply rejection curve in nominal corner at 65°C.

A high DC Power Supply Rejection Ratio may be achieved through high open-loop gain. The AC PSRR (at 100 MHz) may go as low as -3 dB in worst cases.



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Figure 7:Worst case transient response measured at -10% power supply fluctuation.

The figure above depicts the worst case (slow corner, 125 °C) transient response of the LDO at a power supply of 1.08 V (10% fluctuation). As can be seen, the output voltage drops to 880mV. A line transient of 33 mV (measured between the output voltages obtained at 1.26(+10%), -40 °C and 1.08(-10%), 125 °C has been obtained.



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Figure 8: Line regulation measurement across process corners.

The maximum line ripple is 11mV. This value has been measured in the no-load to full-load setting.



Figure 9: Load regulation measured across process corners.

The minimum and maximum load ripples are 11mV and 28mV respectively. This has been measured in the full-load to no-load setting.



Figure 10: Equivalent Output Noise

6. CONCLUSIONS

We have designed a low power low drop-out regulator that is capable of delivering four different output voltages, based on the control signals it receives. The design yields a 30 dB gain, but a gain of upto 50 dB may be achieved by further increase in transconductance of the differential pair. The design is disadvantaged from an input offset point of view, as the input offset error is upto 10 mV. Also, a folded cascade topology with resistive biasing can generate greater gain, reducing the number of stages and making phase margin of the system easier to accomplish at lower values of external capacitance.

The regulator sinks a maximum quiescent current of 0.5 mA, hence the low power dissipation of a hundred microwatts. The circuit is capable of furnishing upto 0.88 volts when power supply is at 90% of the desired value, thereby accounting for power fluctuations. Also, the regulator has been shown to be stable over a wide range of temperatures, ie -40 $^{\circ}$ C to 125 $^{\circ}$ C, and across process corners.

Presently, the external capacitor used is quite large (10 μ F), but capacitorless architectures[4] have been proposed and form a significant part of current CMOS LDO design literature. The current design, hence has scope of improvement in this direction, which may be the subject of our future research.

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