DESIGN AND PERFORMANCE ANALYSIS OF ZBT SRAM CONTROLLER

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ABSTRACT

Memory is an essential part of electronic industry. Since, the processors used in various high performance PCs, network applications and communication equipment require high speed memories. The type of memory used depends on system architecture, and its applications. This paper presents an SRAM architecture known as Zero Bus Turnaround (ZBT). This ZBT SRAM is mainly developed for networking applications where frequent READ/WRITE transitions are required. The other single data rate SRAMs are inefficient as they require idle cycles when they frequently switch between reading and writing to the memory. This controller is simulated on the Spartan 3 device. And the performance analysis is done on the basis of area, speed and power.

KEYWORDS

ZBT SRAM, performance analysis, READ/WRITE transitions, speed, area & power

1. INTRODUCTION

The emergence of networking and communication systems requiring higher bandwidth interfaces and lower latency for peripheral components lead to the implementation of designs using high throughput memory with efficient bus utilization and resulted in the development of a new SRAM architecture known as ZBT. The previous generation of static memory types is inefficient as they require idle cycles when they frequently switch between reading from and writing to the memory. IDT, Micron, and Motorola have developed the ZBT SRAM architecture to address this problem.

ZBT SRAM is offered with two intefaces they are: Flowthrough and Pipelined SRAM. Pipelined interface requires two clock cycles for read and two clock cycles for write operations where as flowthrough requires single clock cycle for both read and write operation, respectively. Flowthrough provides one clock cycle less latency then pipelining, where as pipelining provides high clock to data access.

Due to the fast, low latency access to the CPU, SRAMS are widely used in data communication systems. ZBT SRAM architecture was developed to improve the bandwidth of the interface and overcome the several limitations. ZBT SRAM technology was developed for operation in the applications where data rates are below 200MHz.

Synchronous SRAM basically comes under two different flavors: Single data rate SRAMs and Double data rate SRAMs [5].

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The single Data Rate SRAMs are:

- Pipelined vs. Flowthrough SRAMs
- Burst SRAMs
- Network SRAMs - NoBL™/ZBT™ SRAMs.

The Double Data Rate SRAMs are:

- Standard DDR SRAMs
- QDR™ SRAMs.

Table 1. Comparison of ZBT/NoBL SRAM with other single data rate synchronous SRAMs

Other Single Data Rate Synchronous SRAMs	**ZBT/NoBL Synchronous SRAM**
Most effective for Burst Reads/Writes for Level 2 Cache	Ideal for Networking applications
Ideal for Dominated Read or Write	Ideal for Read/Write ratio of 1
Latency occurs when switching from write to read operation	Enables faster memory performance-eliminates the latency cycle

2. ZBT SRAM CONTROLLER

2.1. A Primer on ZBT SRAM

The term "Zero Bus Turnaround" was invented by IDT in October 1996. IDT, Micron, and Motorola are the three companies that developed the ZBT technologies independently, and are offering compatible ZBT products based upon the same architecture. ZBT SRAM provides the maximum system throughput by utilizing every bus cycles. There is no turnaround cycles when switching between read and write cycles. So this feature is beneficial in various applications with random, intermixed read and writes operations on the data bus as compared to long bursts of reads and writes. Some of the applications are LAN and WAN switching, gigabit switching, network interface cards, ATM switching, switch or hub-shared fabric and router tables. ZBT SRAM comes in two varieties i.e. pipelined and flowthrough. Flowthrough devices have shorter latency than pipelined devices, but pipelined devices can operate at higher frequencies. Control signals on both types are identical, and are simpler than Sync Burst. Pipelined ZBT SRAMs are late-late-read RAMs in the sense that data appears two clock cycles after address. In order to allow interleaved reads and writes, it is also called late-late-write RAM. Flowthrough ZBT SRAM is late-read RAMs in that data appears one clock cycle after address. They are also called late-write RAMs [10].

2.2. Block Diagram of ZBT SRAM Controller

In figure 1, the various low level modules of ZBT SRAM Controller are shown. An overview of various signals used in ZBT SRAM controller are control, clock, address and data signals to give an overall functionality description. The ZBT SRAM controller accepts SRAM request from user and performs pipelined or flowthrough read and write operations, respectively. The controller ensures that correct latencies and bus turnaround timings are met. Clock signal which comes under the module clk_ctrl is used for all clocking purposes including reads and writes. All these timing references are made at the rising edge of clock. Pipe_stage covers the control signals, and

there are three primary types of control signals to interface with memory controllers. They are wr_n, mode and adv_load. Wr_n is a synchronous input, asserted LOW for write operation and asserted HIGH for read operation. Mode is a synchronous signal used to select the mode in which memory is working i.e. either pipelined or flowthrough mode. Address signals comes under addr_ctrl_out which uses one synchronous bus input for all read and write operations with memory device. And last one is data signals that come under data_inout module which uses one synchronous bidirectional data bus for all read and write operations to and from the memory device. Further, description of these modules is given below:

- Pipe_delay provides the proper delay for the input data, depending on whether the controller is working in the pipelined or flowthrough mode.
- Addr_ctrl_out registers the address and control signals before outputting them to the ZBT SRAM.
- Data_inout registers the input and output user signals for speed purposes in a stand-alone controller configuration.
- Clk_ctrl provides clock to all modules.

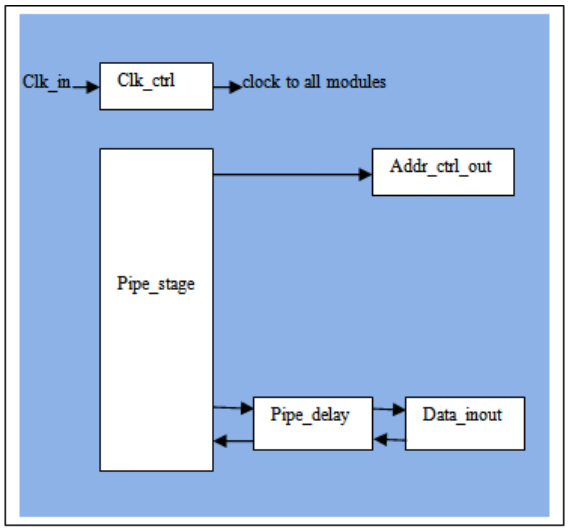

Figure 1. Block Diagram of ZBT SRAM Controller

2.3. ZBT SRAM Sequence

ZBT SRAM uses one system clock input for all clocking purposes including read and write operations. Both read and write commands are sent on the rising edge of the clock. Here read data bus and write data bus are the same. Figure 2(a) shows the timing of read and write operations in the flowthrough ZBT SRAM. In this when address is loaded on the address bus then read/write will be done after one clock cycle as shown in the fig below. Figure 2(b) shows the timing of read and write operations in the pipelined ZBT SRAM. In this when address is loaded on the address bus and read/write signal is given then read/write is done after two clock cycles as shown in the figure below.

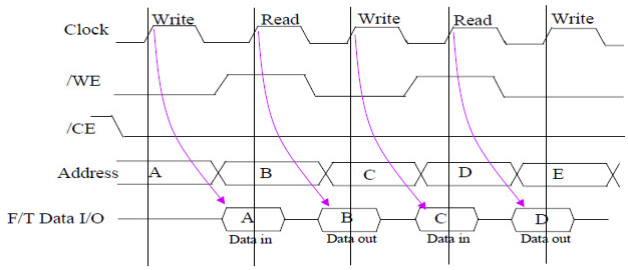

Figure 2(a): Flowthrough operation

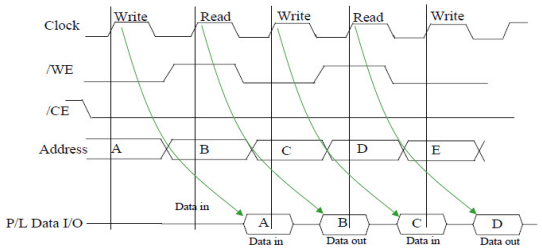

Figure 2(b): Pipelined Operation

3. RELATED WORK

Many researchers have explored the reading and writing from and to the memory in the past with different SRAMs memory architectures and controllers designed. Some of the papers and datasheets are discussed below. Kang Li et. al. [2] proposed a new architecture of shared QDR SRAM controller to make the SRAM Controller suitable for higher bandwidth and speed network communication. In this arbitration method is used to simultaneous read and write operation to the memory can be executed, and tag architecture is adopted to keep the special sequence of the SRAM reference. Thus, the high utilization of bandwidth is done. Ravi Khatwal [1] has worked to design high speed and low power consumption memory for embedded system. And by using Xilinx tool, they calculate the access time that is required for selecting a word and reading it. In this, synchronous static RAM has easily read/writes operation in efficient manner. Abhishek kumar et. al. [4] has worked to design a kind of SDRAM controller. This controller provides a synchronous command interface to the SDRAM memory along with several control signals. It has two main control schemes, command generation and signal generation, simultaneously these modules provide signal to the data path for data transfer. In this memory system operates at double the frequency of processor, without affecting the performance, we can reduce the data bus size. Ranjan Chakraborty [3] discusses about the design of an 8-bit First In First Out Memory which may be utilized in various electronic components and gadgets. In the first stage of design, the RAM 16X4S chips are introduced in the design but here the numbers of bits were reduced from 16 to 8 as it was not being possible to carry the previous number of bits in this renewed design.

4. PROPOSED WORK

The design of the ZBT SRAM controller has been done successfully on Xilinx ISE Design Suite 12.4. The main contributions of this work are as follows:

1). *ZBT SRAM Controller design*: At first, we have to understand the working of address module. Secondly, the most important block is datapath module, the most difficult aspect of ZBT SRAM controller design is to transmit and capture data at proper time delay according to the mode selected.

2). *ZBT SRAM Controller analysis*: After completing the design process, analysis part is done. Analysis can be done on the basis of speed, area, and power consumed. And also the frequency at which it is working.

5. HARDWARE DESIGN AND VHDL MODEL

The hardware design of ZBT SRAM Controller has gone through three different stages. In the first stage, the VHDL code is written and implemented for Flowthrough SRAM. In the second stage, the VHDL code is written and implemented for Pipelined SRAM. In the third and the final stage, Controller is designed and implemented for both techniques. Figure 3 shows the RTL Schematic for ZBT SRAM Controller.

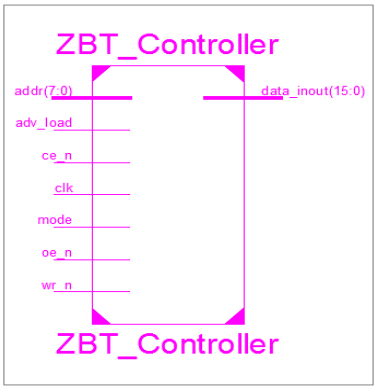

Figure 3: RTL schematic of ZBT SRAM Controller

- clk is the input clock signal to the controller.
- oe_n is the output enable signal.
- ce_n is the chip enable signal.
- wr_n is the read/write signal.
- mode is the mode select signal i.e. either flowthrough or pipelined.
- adv_load is the advance or load pin to the controller.
- addr is the user defined address i.e. the input address to the controller.
- data_inout is the data out from the controller during read process or data in from the user to the memory during write process.

6. SIMULATION RESULTS

Figure 4(a) shows the VHDL simulation of controller in flowthrough mode of ZBT SRAM Controller. Here, the period of clk given is 1us. Here control signals are occurred either at high-to-low transition or at low-to-high transitions. Oe_n is the output enable signal which is active low signal. It is required for read operation, to enable the output. Ce_n is the chip enable signal, which is also active low signal. Wr_n is the read/write signal, when LOW, it worked as write signal and when HIGH, it worked as read signal. Adv_load is the advance or load signal, which when low, loads the new address on address bus and when high, advances the address present on the address bus. As Addr is the input pin and therefore the advanced address is not shown on this pin only the loaded address is visible. Data_inout is the data bus, which is bidirectional in nature that same data bus is used in both read and writes cycles. Reg1 and reg2 are the memory array for flowthrough and pipelined ZBT SRAM, respectively. The simulation results, shown below are the read operation in flowthrough mode that is read operation take only one clock cycle for its operation.

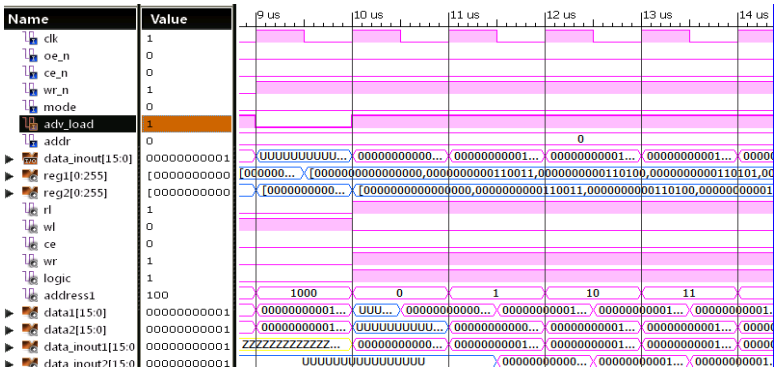

Figure 4(a): Read/Write in Flowthrough ZBT SRAM

Figure 4(b) shows the VHDL simulation of controller in pipelined mode of ZBT SRAM Controller. This simulation results, shows the read operation in pipelined mode that is in this read operation takes two clock cycles for its operation.

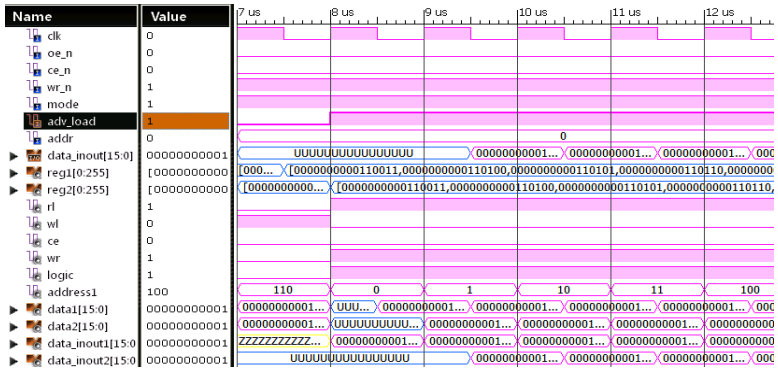

Figure 4(b): Read/Write in Pipelined ZBT SRAM

7. RESULTS AND DISCUSSIONS

Table 2(a) shows the device utilization summary that includes the utilization of slices, slice flip flops, 4 input LUTs, bonded IOBs and GCLKs. Table 2(b) shows the timing summary, which includes minimum time period, maximum frequency needed , minimum time required by input before clock, maximum time that output required after clock and maximum combinational path delay.

Table 2(a): Device Utilization Summary

Logic Utilization	Used	Available	Utilization
Number of Slices	148	768	19%
Number of Slice Flip Flops	201	1536	13%
Number of 4 input LUTs	161	1536	10%
Number of bonded IOBs	25	124	20%
Number of GCLKs	1	8	12%

Table 2(b): Timing Summary

Timing	ZBT SRAM Controller
Speed Grade	-4
Minimum period	5.007ns
Maximum Frequency	199.720MHz
Minimum input arrival time before clock	6.598ns
Maximum output required time after clock	11.325ns
Maximum combinational path delay	12.538ns

8. CONCLUSIONS

In this paper, we have designed various modules of ZBT SRAM Controller and verified the required functionality by using test bench. The main challenging part is to meet all the timing requirements of various modules. We have met all the timing requirements efficiently. All the design features are met according to the requirements. The device utilization summary is given in Table2 (a) and timing summary is given in Table2 (b). And the total power consumed is 243.76 mW.

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