DESIGN OF IMPROVED RESISTOR LESS 45NM SWITCHED INVERTER SCHEME (SIS) ANALOG TO DIGITAL CONVERTER

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ABSTRACT

This work presents three different approaches which eliminates the resistor ladder completely and hence reduce the power demand drastically of a Analog to Digital Converter. The first approach is Switched Inverter Scheme (SIS) ADC; The test result obtained for it on 45nm technology indicates an offset error of 0.014 LSB. The full scale error is of -0.112LSB. The gain error is of 0.07 LSB, actual full scale range of 0.49V, worst case DNL & INL each of -0.3V. The power dissipation for the SIS ADC is 207.987 µwatts; Power delay product (PDP) is 415.9 fWs, and the area is 1.89µm2. The second and third approaches are clocked SIS ADC and Sleep transistor SIS ADC. Both of them show significant improvement in power dissipation as 57.5% & 71% respectively. Whereas PDP is 229.7 fWs and area is 0.05 µm2 for Clocked SIS ADC and 107.3 fWs & 1.94 µm2 for Sleep transistor SIS ADC.

KEYWORDS

CMOS 45nm, flash analog to digital converter, low power, resistorless, switched inverter scheme (SIS), sleep transistor.

1. INTRODUCTION

Recent advances in the field of electronics require data converters for interfacing the signals of real world for various applications as shown in Fig.1 and then processing the obtained information in digital domain [10], [20]. In present scenario an Analog to Digital Converter (ADC) became an unavoidable component and it is also required to be fabricated on the same chip instead of a separate circuit for data conversion.

Since a few years lot of research is done on data converters to achieve maximum speed and minimum power consumption [8]. As technology scaling continues the demand of minimum power dissipation further increases in various modern battery powered applications [25].

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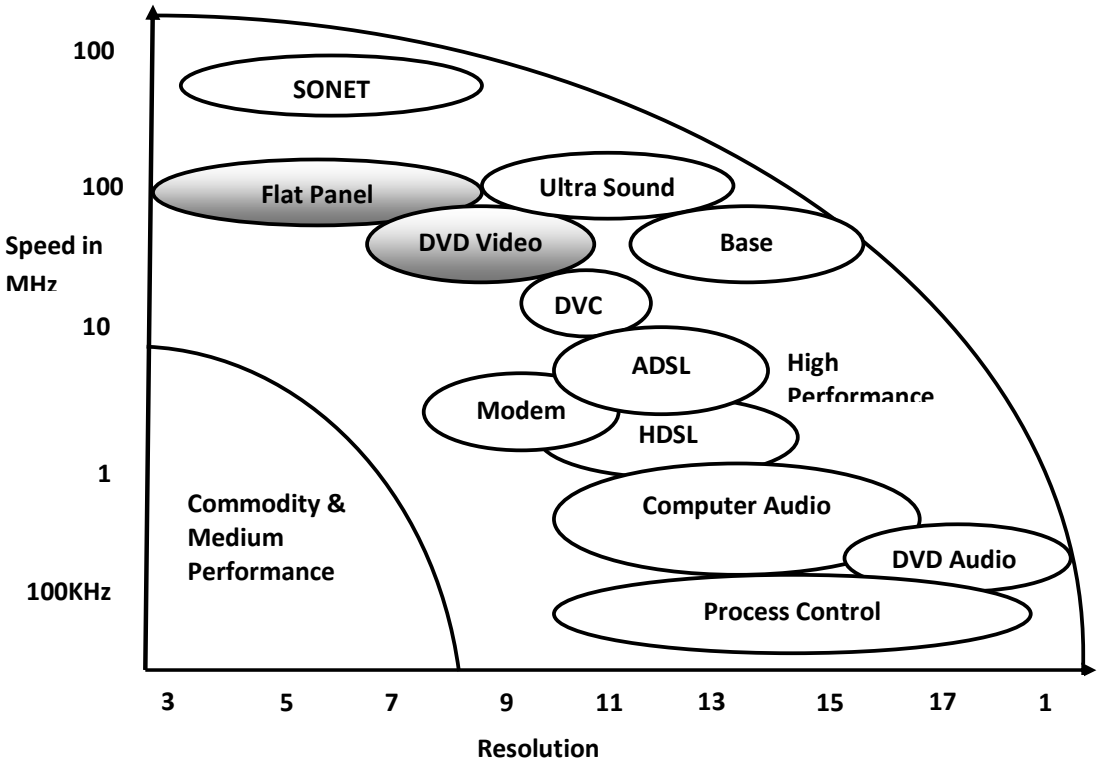

Figure 1. Various Applications of ADC

The research is continuing in various types of data converters like flash, semiflash, sigma delta, pipeline, folding, and successive approximation register (SAR) ADCs to optimize their performance [1], [12]. The insatiable demand of high performance data converters attracts researchers due to their wide usage in digital signal processing. In various applications data converters repress the performance severely if not designed optimally. Investigation of new design techniques for an ADC is in progress in order to reduce power dissipation, increase operating speed and decrease chip area [3].

High speed data converters are the key building blocks in many applications including high data rate serial links [2], [11]. Ultra wide band systems [4], magnetic and optical data storage devices [5], high speed instrumentation, wideband radar and optical communications [8], 3G telecommunication systems, wireless wide area networks, broadband wireless communication network, radio astronomy, optical communication systems [6]. ADCs with high speed and resolution in the range of 6-8 bits are used in digital telecommunications, cryptography, high performance image sensing and processing, digital signal oscilloscopes, gigabit Ethernet. ADCs with low power dissipation are especially required for system on chip (SOC) applications, cellular phones, Digital TVs, & spectrum monitoring systems [7].

Out of various ADC architectures available, the design of flash ADC becomes quite more important as it is used in other ADC architectures like two step ADC and multi bit sigma delta ADC. The block diagram of a flash ADC is as shown in Fig.2 [26], [34].

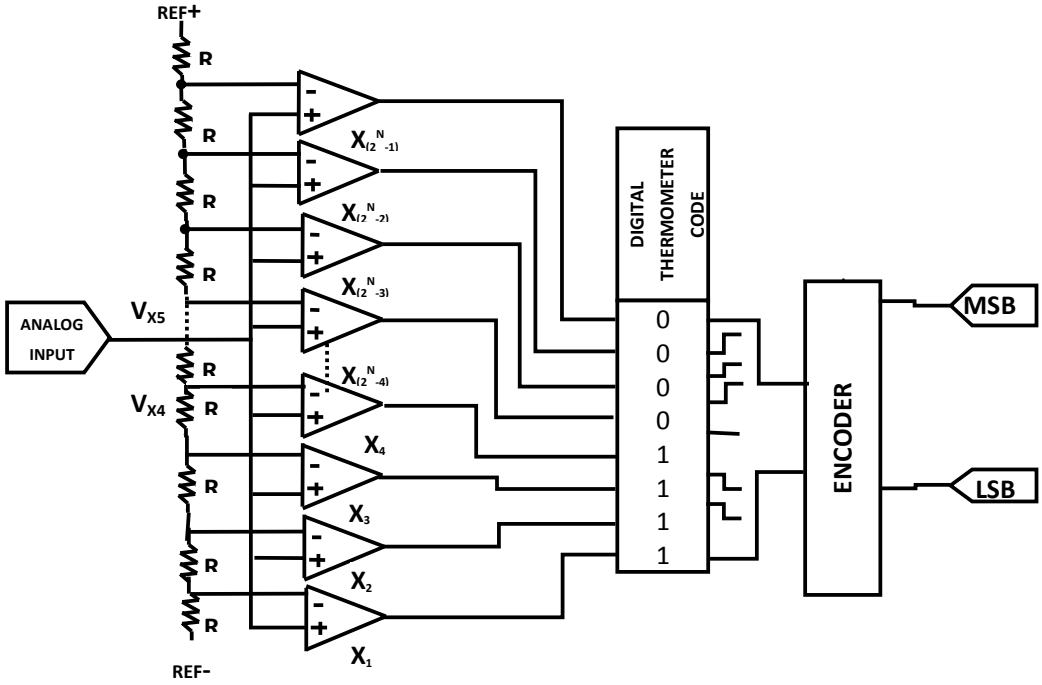

Figure 2. Block Diagram of a Flash ADC

Due to increase in number of resistors and comparators required in designing of fully parallel flash ADCs having resolution 8 bits and above, the layout area & power dissipation also increases. Therefore in recent years the research is carried with resistor less flash ADC architecture.

New methods developed to reduce the power consumption of flash ADCs are [5].

- Use of interpolation and voltage to current converters that operate as preamplifier stage of latches.
- Extension in the input range.
- Use of bisection method to let only half of the ADCs working in every clock cycle.

The aim of this work is to design the ADCs required for battery operated devices. The ADCs are designed and simulated with three different power saving schemes. The main improvements for various schemes are envisaged in power dissipation, differential and integral non linearity. The specifications of the design prototype are selected as 3 bit, for 500 MHz signal, and 0.5 V full scale range, with a supply voltage of 1V. The simulation is carried out in 45nm PTM [35] on LT Spice IV platform.

In section II three different types of flash comparator architectures are discussed along with the flow chart and mathematical relations for sizing the transistors of comparator. The design issues of gain booster and encoder blocks are given in section III. Section IV describes the design of ADC using all three comparators. The complete simulation results are shown in section V. Section VI concludes the work.

2. DIFFERENT TYPES OF FLASH COMPARATORS

2.1. Switched Inverter Scheme (SIS) Comparator

When focusing on overall power for a flash ADC, the power dissipation of the comparator is important contributor. In case of n bit flash converters the number of comparator equals 2^n-1 [39]. The switched inverter scheme (SIS) also called Threshold inverter quantization (TIQ) comparator has very simple architecture as shown in Fig.3 [37], [38]. It is quite different than the conventional operational amplifier based differential input voltage (DIV) comparator [9], [28], [34]. The key difference between the DIV comparator and the (SIS) comparator scheme lies in the way the reference voltage is generated for each level. In DIV comparator conventional method of using resistor ladder is utilized for externally generating the reference voltage. Where as in the SIS comparator scheme all 2^n-1 reference voltage for a n bit ADC are set internally by adjusting the threshold voltage of each voltage comparator separately by sizing the transistor properly. All DIV comparators are identical and duplicated for 2^n-1 times but each SIS comparator is altogether different from others and obtained by varying the ß ratio of the inverters.

The SIS comparator design consists of two pairs of inverters connected back to back. Each of the inverter is sized separately to get a unique switching voltage [13], [17].

The cascaded inverters then work as voltage comparator. The full scale voltage range (VFSR) is equally divided by 2^n-1 SIS comparators.

To achieve optimal sizing for each transistor in SIS comparator scheme is very much time consuming. The analytical expression for (W_p/W_n) of each comparator is determined by equating the pull up and pull down saturation currents as equation (1) [14], [15], [16], [18].

$$I_{DSAT} = K.V_{DSAT}\left(V_m - V_{DD} - V_t - \frac{V_{DSAT}}{2}\right) \quad (1)$$

The expression for switching voltage V_m is thus obtained for a short channel CMOS inverter in 45nm as equation (2) [19], [21], [22], [29].

$$V_m = \frac{V_{DD} - |V_{tp}| + V_{tn}\sqrt{1/r}}{1 + \sqrt{1/r}} \quad (2)$$

Where,

$$r = \frac{v_{satp}\, W_p}{v_{satn}\, W_n} = \frac{K_p V_{DSATp}}{K_n V_{DSATn}} \quad (3)$$

$$r = \frac{\mu_p\left(W_p/L_p\right)}{\mu_n\left(W_n/L_n\right)} \quad (4)$$

$$K_p = K_p'\left(\frac{W_p}{L_p}\right) = \beta_p \quad (5)$$

$$K_p' = \mu_p C_{oxp} \quad (6)$$

$$K_n = K_n' \left(\frac{W_n}{L_n}\right) = \beta_n \quad (7)$$

$$K_n' = \mu_n C_{oxn} \quad (8)$$

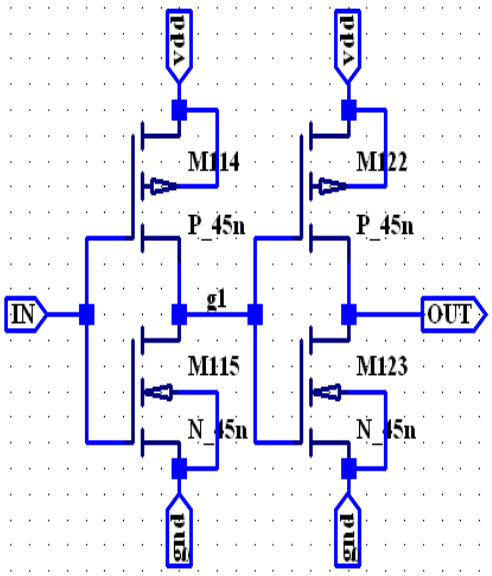

Figure 3. SIS Comparator

The above equations are realized on MATLAB 7.3.0 R2006b or switching voltage calculations. The program is given in Fig.4.

```
>> un= 0.032;
up =  0.0095;
vm = 0.3:0.071:0.801;
vdd = 1;
vtn = 0.22;
vtp = 0.22;
b = sprintf('%.4f', W);
W = (un/(up))*((vm-vtn)./(vdd-vtp-vm))
```

Figure 4. MATLAB code for switching voltage calculation

The main advantage of the SIS comparators is that it does not use any resistor ladder and so it is suitable for low voltage, low power and high speed applications such as cellular mobile phones and touch screen display devices. On the other hand the process parameter variations may cause offset and gain errors to vary considerably when the design is used for higher resolution ADCs. Also noise can be a big challenge for the single ended SIS comparator scheme.

2.2. Clocked SIS comparator

Another type of the comparator as shown in Fig.5.called as clocked SIS comparator (CSIS) uses two cascaded inverters as SIS and two set of PMOS and NMOS connected in parallel. Each pair connected to pull up and pull down networks of the SIS inverter. The pair of PMOS and NMOS is driven by a clock pulse the NMOS is connected to clock whereas PMOS to clockbar. The two pairs are sized to minimum length and width in 45nm technology to get reduction in static power dissipation of the overall voltage comparator. The saving in power dissipation with the modification is approximately 60.37% to that of the SIS comparator.

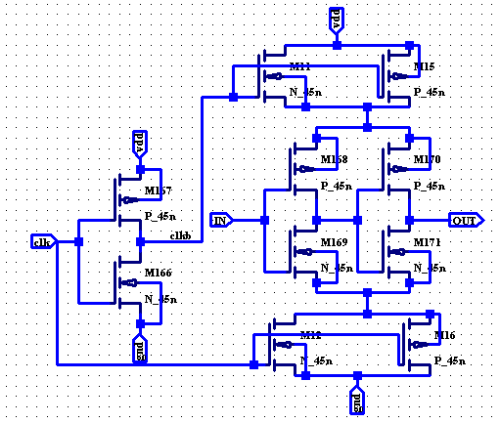

Figure 5. Clocked SIS Comparator

2.3. SIS comparator with sleep transistor

The comparison circuit of SIS comparator is modified by addition of high threshold PMOS and NMOS near the supply rails as shown in Fig.6. The addition of header & footer reduces the static power dissipation to a great extent due to increased resistance of the high threshold PMOS and NMOS transistors [27], [30], [33]. During the period of no activity the section not in use remains completely off. Whereas, the components are invoked again when any activity is detected.

A Local sleep transistor network is used here as opposed to global level network, because every comparator is differently sized and hence the current through each comparator section is also different. The sizing of a sleep transistor is calculated using equation (9).

$$\left(\frac{W}{L}\right)_{Sleep} = \frac{I_{Sleep}}{0.0281\mu_n C_{ox}(V_{DD} - V_T)(V_{DD} - V_{TH})} \quad (9)$$

Where, I_{sleep} is calculated by simulating the circuit without sleep transistor network and finding maximum current that flows through ground or V_{DD}. V_T denotes threshold voltages for short channel device & V_{TH} is equal to threshold voltage of high K device.

$$C'_{ox} = \frac{\epsilon_{ox}}{t_{0x}} \quad (10)$$

$$C_{ox} = \frac{\epsilon_0 . \epsilon_{ox}}{t_{0x}} \quad (11)$$

$$C_{ox} = C'_{ox}.A \qquad (12)$$

$$A = W.L \qquad (14)$$

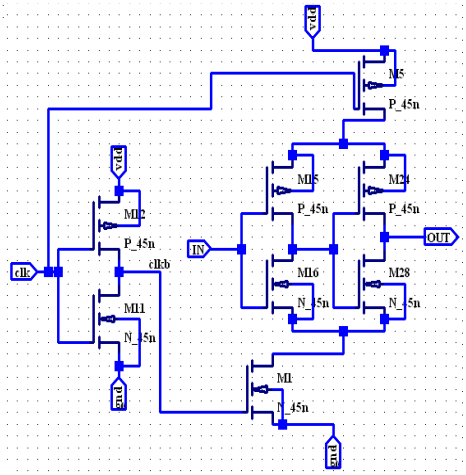

Figure 6. SIS Comparator with Sleep Transistor

The saving in power dissipation with the addition of header & footer is approximately 77.3% to that of the SIS comparator.

3. DESIGN OF ADCS

For the complete realization of any flash ADC the blocks required other than comparator are gain booster and thermometer to binary encoder. The design of these blocks is given here.

3.1. Gain Booster

The gain booster is used to increase voltage gain of the output of a comparator so that it provides a full digital output voltage swing, without which the output of the comparator circuit is unable to drive the next stage, it also makes thresholds sharper for comparator outputs and provide full digital output voltage swing. The gain booster block is designed for lowest switching voltage.

Table 1. Truth table for one out of n code

Input Thermometer code								**Output "01" code**						
T_7	T_6	T_5	T_4	T_3	T_2	T_1		G_7	G_6	G_5	G_4	G_3	G_2	G_1
0	0	0	0	0	0	0		0	0	0	0	0	0	1
0	0	0	0	0	0	1		0	0	0	0	0	1	0
0	0	0	0	0	1	1		0	0	0	0	1	0	0
0	0	0	0	1	1	1		0	0	0	1	0	0	0
0	0	0	1	1	1	1		0	0	1	0	0	0	0

0	0	1	1	1	1	1		0	1	0	0	0	0	0
0	1	1	1	1	1	1		1	0	0	0	0	0	0
1	1	1	1	1	1	1		0	0	0	0	0	0	0

Each gain booster consists of two identical cascaded inverters with the same circuit as that of comparator, but the transistors are sized for minimum aspect ratio for each gain booster [23].

3.1.2. Thermometer code converter

The encoder converts the thermometer code to binary code in two steps [40]. In the first step the thermometer code is converted into one out of n code by using the truth table as shown in Table 1. The one out of n codes is then converted to binary code d2, d1, d0 by Read only memory (ROM) encoder, as shown in Fig.7. [32]. The ROM encoder is a common and straight forward approach to encode the one out of n code to binary bit. The appropriate row m in the ROM is selected by using a row decoder that has the output of comparator m and the inverse of comparator m + 1 as inputs. The output m of the row decoder, connected to memory row m, is high if the output of comparator m is high and the output of comparator m + 1 is low. The row decoder can be realized by, a number of 2-input NAND gates, where one input to each NAND gate is inverted. The main advantage of the ROM decoder approach is its regular structure that is easy to design [31].

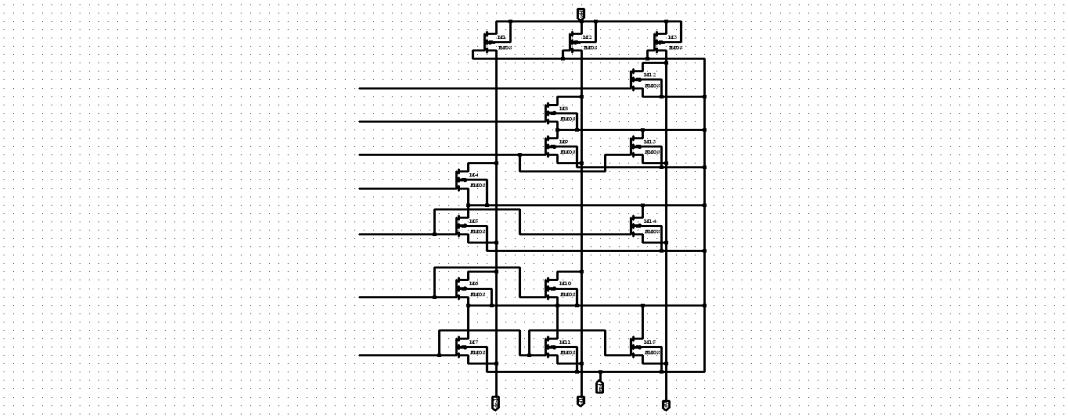

Figure 7. ROM Encoder

4. RESULTS AND DISCUSSION

The proposed technique is applied in the design of 3 bit ADC with chosen specifications as given in table II and the implementation is as shown in Fig.8. for SIS ADC, Fig.10. for Clocked SIS ADC & in Fig.12. for sleep transistor ADC [23], [24].

The design consists of comparator chain, gain booster circuit and a thermometer to binary encoder block and finally a buffer circuitry to reduce the loading effects.

Conventional voltage comparators use a resistor ladder circuit to generate 2^n-1reference voltages (V_{ref}) for comparators, ranging from $V_{ref(max)}$ to $V_{ref(min)}$. Generating equally spaced reference voltages determines the quantization performance of ADCs [21]. The SIS comparator eliminates the use of the resistor ladder circuit by generating the reference voltages internally. The SIS comparator uses two cascaded inverters to generate the range of internal reference voltages. At

the first inverter, the analog input quantization is determined by adjusting the ratio of the PMOS and PMOS transistors. The second inverter is used to increase the voltage gain and prevent unbalanced propagation delays of all comparators.

The results for SIS Comparator are shown in Fig. 8. and for the modified versions 2 and 3 they are given in Fig.11. and Fig.13.

The total power consumption here is determined by summing up the power dissipation of each circuit separately. The various blocks used to realize the design are comparator section, gain booster, XOR gate, ROM Encoder and buffers the comparison results are shown in table III for all three different types of ADCs [9], [17], [30], [37], [38].

Table 2. ADC Specification

S No.	Specification	Value
1	Resolution	3 Bit
2	CMOS tech.	45nm
3	Model File	PTM
4	$L_P = L_N = L_{min}$	45 nm
5	t_{ox}	14 Angstroms
6	C_{ox}	25 fF/ μ m^2
7	Max. Speed	500 MSPS
8	V_{FSR}	0.3 V-0.8 V
9	V_{LSB}	0.0714 V
10	$(W_p/W_n)_{Min}$	0.55
11	$(W_p/W_n)_{Max}$	266
12	V_{DD}	1 V
13	V_{TP}	-0.22V
14	V_{TN}	0.22V
15	$V_{m\ min}$	0.371 V
16	$V_{m\ max}$	0.8 V
17	μ_n	320 cm^2/v-sec
18	μ_p	95 cm^2/v-sec
19	C_L (Load Capacitance)	0.01fF

4.1. Design of SIS ADC

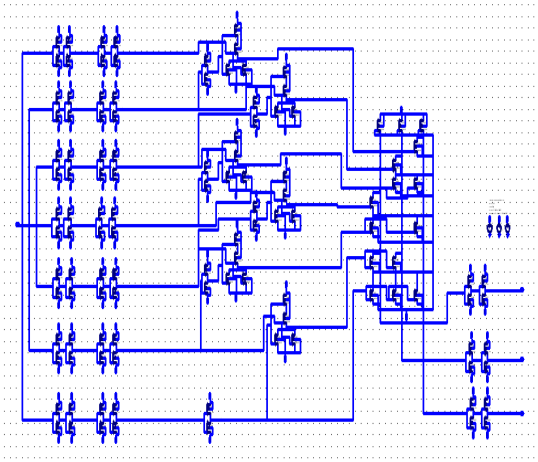

Figure 8. SIS ADC with ROM Encoder

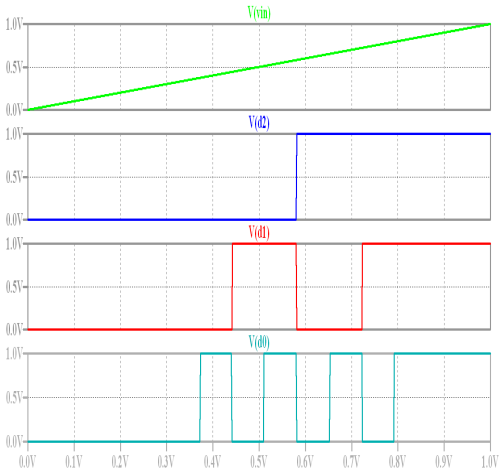

Figure 9. Simulation Results of SIS ADC

4.2. Design of Clocked SIS ADC

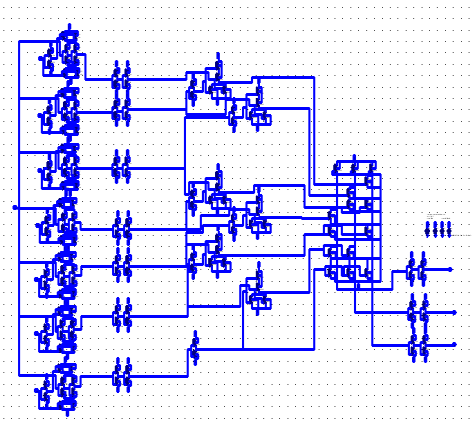

Figure 10. Clocked SIS ADC with ROM Encoder

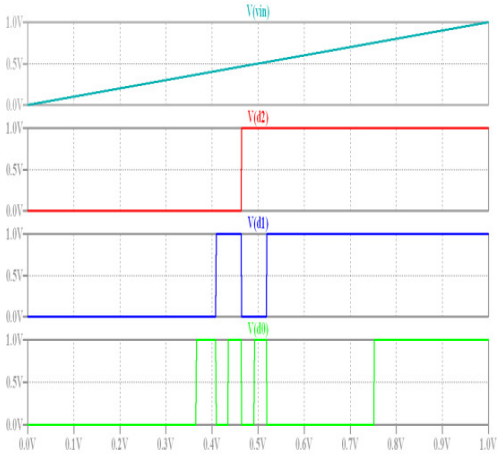

Figure 11. Simulation Results of Clocked SIS ADC

4.3. Design of Sleep Transistor SIS ADC

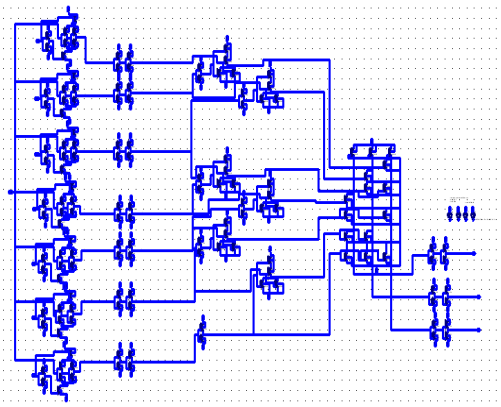

Figure 12. Sleep Transistor SIS ADC with ROM Encoder

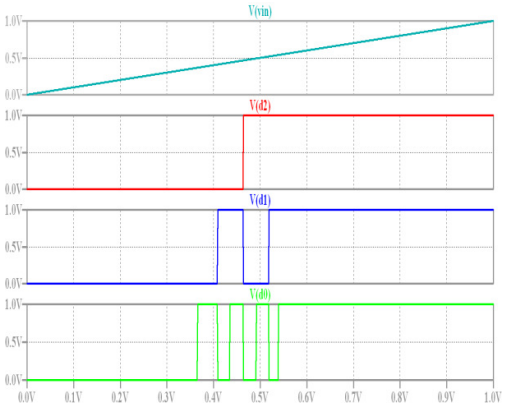

Figure 13. Simulation Results of Sleep Transistor SIS ADC

The power dissipation is calculated and is compared for all the designed ADCs. The finding for saving in power dissipation is shown in Table IV.

The various dynamic parameters for all ADCs are also calculated using the equations (15) – (21) [29], [36] and are tabulated in Table V.

$$\text{Offset error} = \text{Real Transition} - \text{Ideal Transition} \quad (15)$$

$$\text{Offset in LSB} = \text{Offset Error} / \text{One LSB} \quad (16)$$

$$\text{Full Scale Error} = \text{Real last transition} - \text{Ideal last transition} \quad (17)$$

$$\text{Gain error} = \text{Average code width (LSB size)}$$

$$= \text{Real last transition} - \text{First transition} / 2(2^n\text{-}1\text{ -}1) \quad (18)$$

$$\text{DNL} = \text{DNL}[k] = \text{Width}[k] - 1 \quad (19)$$

Where,

$$\text{Width}[k] = \text{Transition}[k+1] - \text{Transition}[k] \quad (20)$$

$$\text{INL}(m) = \text{Transition}[m] - \text{Transition}[\text{ideal}] \ / \ \text{Step Width}[\text{Ideal}] \quad (21)$$

Table 3. Comparison Of Component Power Dissipation In µW

S.No.	Blocks	SIS ADC	Clocked SIS ADC	Sleep SIS ADC
1	Comparator	167.087	66.214	37.88
2	Gain Booster	35.18	18.678	18.48
3	One out of n coder	3.1357	1.9	1.8
4	ROM encoder	2.153	1.1	1.09
5	Buffers	0.437	0.32	0.31
6	Total Power	207.987	88.377	59.64
7	Delay	2ns	2.6ns	1.8ns
8	Power Delay Product	415.9 fWs	229.7 fWs	107.3 fWS
9	Area	1.89 μ m^2	2.05 μ m^2	1.94 μ m^2

$$\text{INL} = \sum_{i=1}^{m} \text{DNL}[i] \quad (22)$$

DNL is Differential non linearity error and INL is Integral non linearity error. The quantization error in each case is less than 0.5 LSB.

Table 4. Block wise % saving in power dissipation as compared to SIS ADC

S.No.	Blocks	Clocked SIS ADC [17], [30], [37], [38]	Sleep SIS ADC
1	Comparator	60.37 %	77.3 %
2	Gain Booster	46.9 %	47.47 %
3	One out of n coder	39.4 %	42.6 %
4	ROM encoder	48.9 %	49.37 %
5	Buffers	26.77 %	29.06 %
6	Total Power	57.5 %	71 %

Table 5. Dynamic Parameters For ADCs In LSB

Parameter	SIS ADC	Clocked SIS ADC	Sleep Transistor SIS ADC
Offset Error	0.014	0.158	-0.084
Full Scale Error	-0.112	-0.26	-0.36
Gain Error	0.07	0.028	0.021
DNL	-0.3	-0.7	-0.6
INL	-0.3	-0.7	-0.4

5. CONCLUSION

Low power architecture for a 3-bit CMOS SIS based flash ADC is presented using PTM 45 nm. The modified versions of SIS ADC can further achieve very low power dissipation; this proposed method can reduce power dissipation upto 71%. It uses smaller silicon area of 1.94μm2. The DNL of the proposed ADC is within -0.3LSB and INL is also within -0.3LSB. The proposed ADC chip so designed can be used for capacitive pressure sensor, video systems as well as it can be used in a low power two-step ADC, pipelined ADC and multi-bit sigma delta ADC. A disadvantage is that for higher no of bits the increased complexity of the circuit consumes more chip area and will likely consume more power.

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