ENHANCING MULTIPLIER SPEED IN FAST FOURIER TRANSFORM BASED ON VEDIC MATHEMATICS

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ABSTRACT

Vedic mathematics is an ancient system of mathematics which has a unique technique of calculations based on 16 sutras. The performance of high speed multiplier is designed based on Urdhva Tiryabhyam, Nikhilam Navatashcaramam Dashatah, and Anurupye Vedic mathematical algorithms. These algorithms gives minimum delay and used for multiplication of all types of numbers. The performance of high speed multiplier is designed and compared using these sutras for various NxN bit multiplications and implemented on the FFT of the DSP processor. Anurupye sutra on FFT is made efficient than Urdhva tiryabhyam and Nikhilam Navatashcaramam Dashatah sutras by more reduction in computation time. This gives the method for hierarchical multiplier design. Logic verification of these designs is verified by simulating the logic circuits in XILINX ISE 9.1 and MODELSIM SE 5.7g using VHDL coding.

KEYWORDS

Urdhva Tiryagbhyam, Nikhilam Navatashcaramam Dashatah, Anurupye, Vedic multiplier.

1. INTRODUCTION

Multiplication is an important function in arithmetic operations. Multiply and Accumulate(MAC) and inner product are some of the frequently used Computation- Intensive Arithmetic Functions(CIAF) that are implemented in many Digital Signal Processing (DSP) applications such as convolution operation, filtering, Fast Fourier Transform(FFT) and in microprocessors in its arithmetic and logic unit(ALU) [2].

The demand for high speed processing has been increasing as a result of expanding computer and signal processing applications. High throughput arithmetic operations are important to achieve the desired performance in many image and real time processing applications. One of the arithmetic operations in such applications is multiplication and the development of fast multiplier circuit. Reduction of both the time delay and power consumption is very essential requirements for many applications [3].

Multiplier design based on Vedic Mathematics is one of the fast and low power multiplier. Minimizing power consumption for digital systems is important and it involves optimization at all levels of the design. This optimization includes one technology that is used to implement the style, topology and the architecture for implementing the digital circuits.

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2. VEDIC MATHEMATICS

Vedic mathematics is a part of four Vedas. Mainly it is part of Sthapatya- Veda which is an upa-veda and the supplement of Atharva Veda. It gives elucidation of several mathematical terms including arithmetic, geometry, trigonometry, factorization, calculus, etc. In the period of 1884-1960, Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja comprised all this work together and gave its mathematical explanation while it is used for various applications. After extensive research in Atharva Veda, Swamiji constructed the 16 sutras (formulae). But it is not found in present text of Atharva Veda because these formulae were constructed by Swamiji itself [6].

Vedic mathematics is not only a mathematical wonder but also it is used for logical operations. Vedic mathematics deals with various branches of mathematics like arithmetic, algebra, geometry etc. These methods and ideas can be directly applied to geometry, trigonometry, and applied mathematics of various kinds. This is an interesting field and it gives some effective algorithms that can be applied to various branches of engineering such as computing and digital signal processing (DSP).

A large amount of work has been done by understanding various methodologies of sutras. The16 sutras are as following:

- **Chalana-Kalanabyham:** Denotes "Differences and Similarities operation".
- **Ekanyunena Purvena:** Denotes "By one less than the previous one operation".
- **Gunitasamuchyah:** Denotes "The product of the sum is equal to the sum of the product operation".
- **Paraavartya Yojayet:** Denotes "Transpose and adjust operation".
- **Sankalana- vyavakalanabhyam:** Denotes "addition and subtraction operation".
- **Shunyam Saamyasamuccaye:** Denotes "When the sum is the same that sum is zero operation".
- **Urdhva-tiryagbhyam:** Denotes "Vertically and crosswise operation".
- **Yaavadunam:** Denotes "Whatever the extent of its deficiency operation".
- **(Anurupye) Shunyamanyat:** Denotes "If one is in ratio, the other is zero operation".
- **Ekadhikina Purvena:** Denotes "By one more than the previous one operation".
- **Gunakasamuchyah:** Denotes "Factor of the sum is equal to sum of the factors operation".
- **Nikhilam Navatashcaramam Dashatah:** Denotes "all from 9 and last from 10 operations".
- **Puranapuranabyham:** Denotes "By the completion or non completion operation".
- **Shesanyankena Charamena:** Denotes "The remainders by the last digit operation".
- **Sopaantyadvayamantyam:** Denotes "The ultimate and twice the penultimate operation".
- **Vyashtisamanstih:** Denotes "Part and Whole operation".

3. DESIGN OF HIGH SPEED VEDIC MULTIPLIER IN FFT

The Vedic multiplier which is designed based on "Urdhva Tiryagbhyam" sutra (algorithm) is a general multiplication formula applicable to all cases of multiplication and it means that "Vertically and crosswise" and it is used for the multiplication of two decimal numbers. The advantage of this sutra is that it is based on novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. This algorithm can be generalized for the design of n x n bit number. The multiplier is independent of the clock frequency of the

processor while calculating the partial products and their sums in parallel. Nikhilam Navatashcaramam Dashatah Vedic mathematical algorithm is done by "All from 9 and last from 10" and it is more efficient to large numbers. Anurupye sutra is done by "if one is in ratio, then other is zero operation".

Digital signal processing (DSP) is a fastest growing technology that is important in almost every engineering discipline. Therefore, it poses tremendous challenges to the engineering community. Fast operation of additions and multiplications are of extreme importance in DSP for digital filters, discrete Fast Fourier transforms etc.
The Vedic multiplier is implemented in FFT, which uses Urdhva Tiryabhyam, Nikhilam Navatashcaramam Dashatah, and Anurupye Vedic mathematical algorithms. The N point DFT is computed by using efficient Fast Fourier transform (FFT) algorithm. It's necessary for a multiplier to be fast and power efficient in order to make this process rapid and simple. It is used to solve partial differential equations and also to perform convolution operations

3.1. Nikhilam Navatashcaramam Dashatah Sutra

Nikhilam Sutra means "all from 9 and last from 10" multiplications. It is applicable to all cases of multiplication but it is more efficient when the numbers involved are large. Small numbers also possible but complexity was increased. The multiplication operation is performed by found out the compliment of the large number from its nearest base. Hence the complexity is lesser for larger original number multiplication.

Nikhilam Sutra performs subtraction of a two number from its nearest power base i.e. 10, 100, 1000, etc. The difference is calculated from the power of 10 is called as Base. It is seen that the difference between the base and the number is Positive and hence it is called as NIKHILAM. The multiplication of two 8-bit numbers is reduced to the multiplication of their compliments and addition is shown in Fig.1.

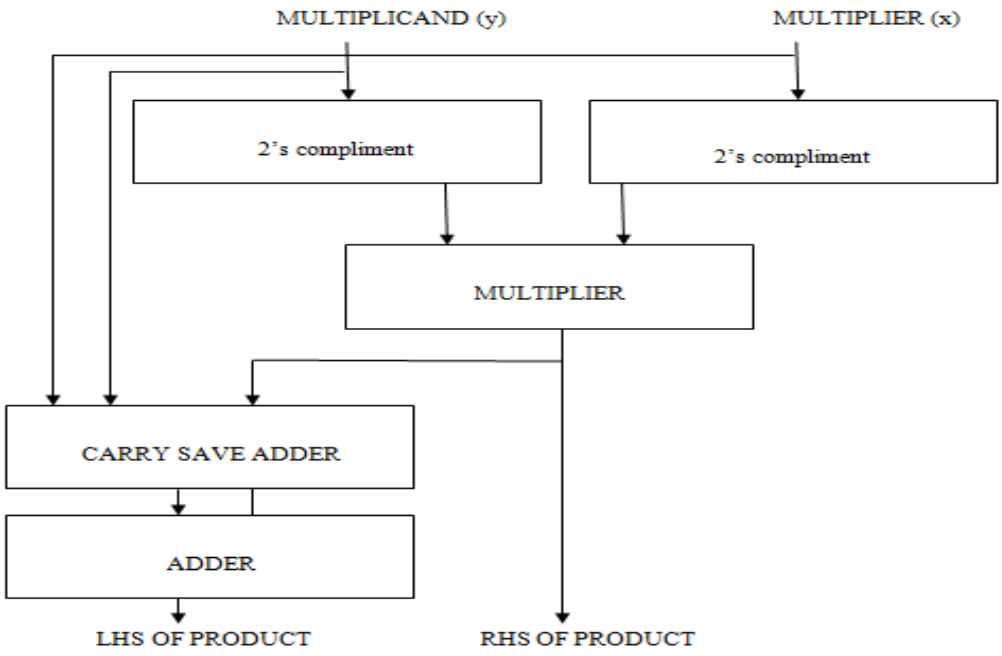

Figure 1.Structure of Nikhilam Navatashcaramam Dashatah Vedic Multiplier

The Nikhilam sutra is applicable to both binary and decimal number system. The subtraction result of multiplicand and multiplier is represented by taking 2"s compliment of those two numbers. The right hand side (RHS) part of the product is implemented using 8x8 bit multiplier. The left hand side (LHS) part of the product is implemented using 8-bit carry save adder. If there is carry in RHS of product then it is added to LHS of product. The multiplication of 97 and 94 using Nikhilam sutra is shown in Fig.2.

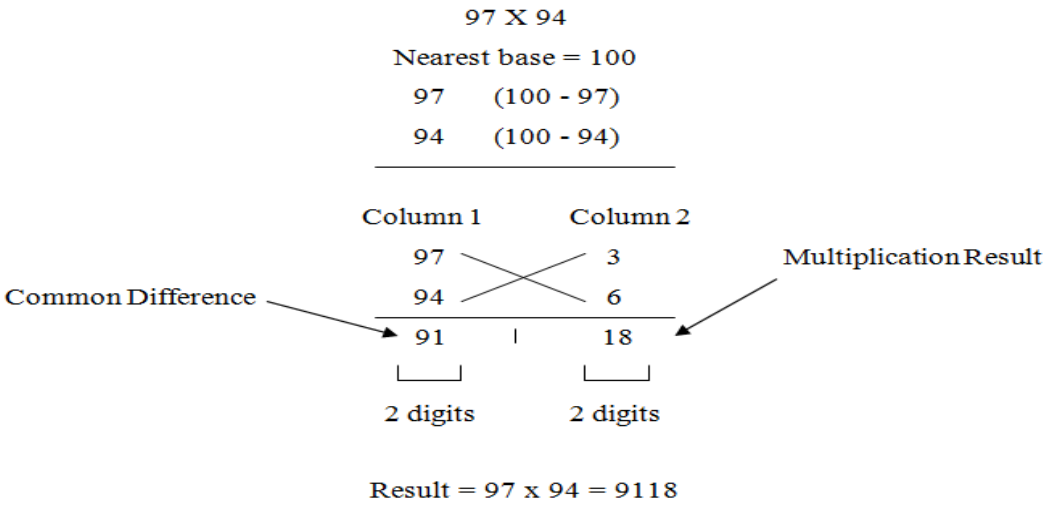

Figure 2.Multiplication Steps using Nikhilam Navatashcaramam Dashatah

3.2. Structure of Urdhva 2x2 Vedic Multiplier

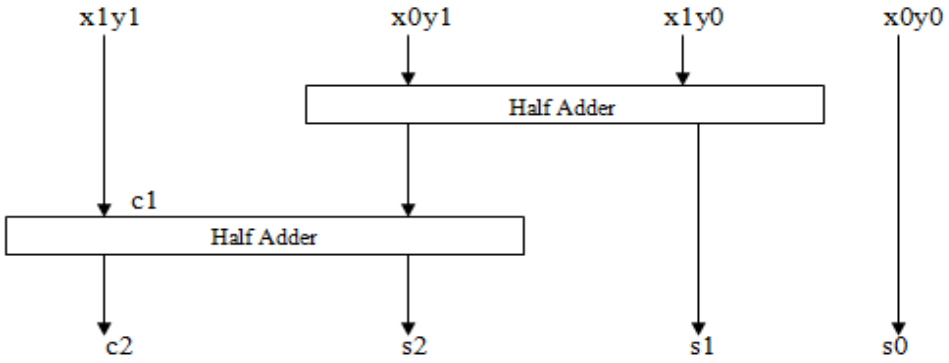

Figure 3.Structure of Urdhva 2x2 Vedic Multiplier

The method is described for two, 2 bit numbers X and Y where X = x1x0 and B = y1y0 as shown in Fig 3. In the first step the least significant bit of the final product (vertical) is obtained by multiplication of least significant bits of two numbers. In the second step the LSB of the multiplicand is multiplied with the next higher bit of the multiplier. Then it is added with the multiplier product of LSB and next higher bit of the multiplicand (crosswise). Likewise the process will be done concurrently.

The sum is obtained in second bit of the final product and the carry is added with the partial product. By multiplying the most significant bits gives the sum and carry. Digital multiplier architecture is

developed by applying Urdhva tiryakbhyam Sutra to the binary number system. This is similar to the popular array multiplier architecture.

Another important multiplication algorithm is Booth multiplication. For high speed applications large booth arrays are required and it provides fast process of multiplying two numbers. The delay is the only time for the signals to propagate through the gates and the multiplication array is formed. An array multiplier is less economical because it requires a large no gates. The method is described for two; 8 bit numbers X and Y is shown in Fig 4.

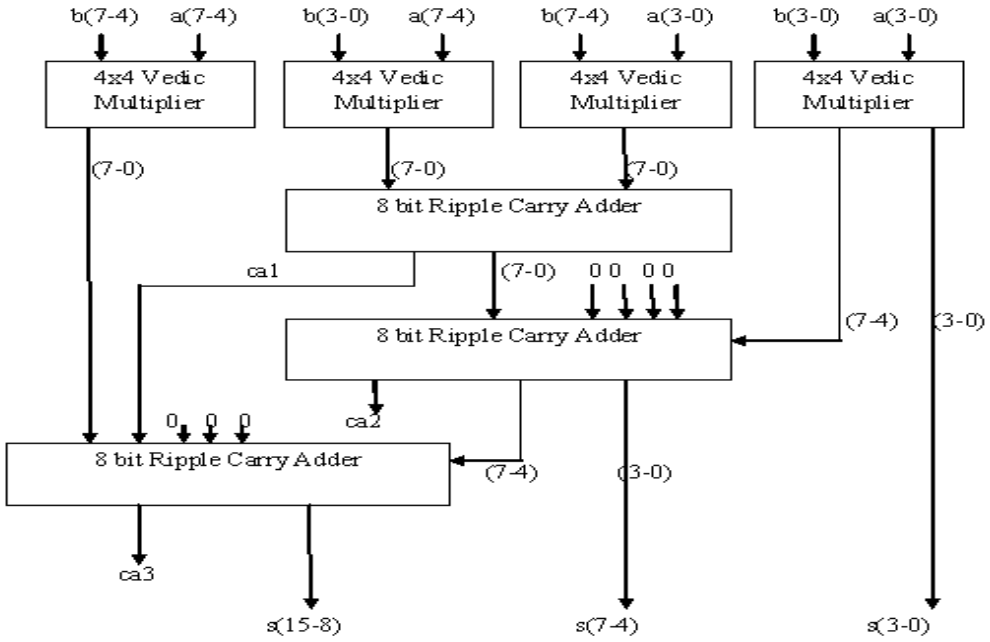

Figure 4.Structure of Urdhva 8x8 Vedic Multiplier

3.2.1. Multiplication of Two Decimal Numbers

This scheme is illustrated by consider the multiplication of two decimal numbers 154 x 142 by Urdhva-Tiryakbhyam method as shown in Fig 5. The result is obtained by multiplying the digits on both sides of the line and added with the carry from the previous step. This generates result for one of the bits and a carry. This process is goes on by adding the carry in the next step. If more than one line is present in one step then all the results are added to the previous carry. In each step, least significant bit (LSB) acts as the result bit and all other bits act as carry for the next step. Initially the value of carry is taken to be zero.

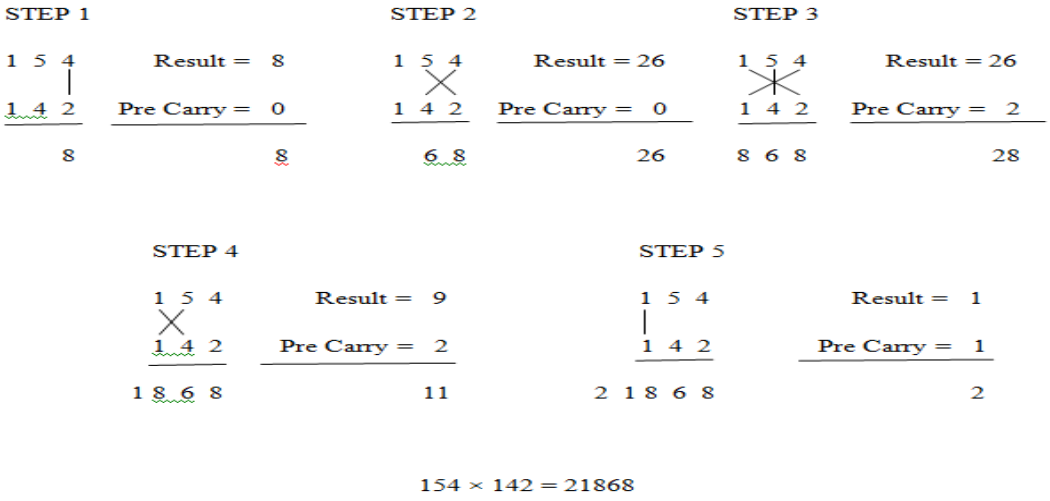

Figure 5.Multiplication Steps using Urdhva

3.3. Anurupye (Shunyamanyat) Sutra

The upa-Sutra Anurupye means 'proportionality'. This Sutra is used to find products of two numbers when both of them are near the Common bases like 50, 60, 200 etc (multiples of powers of 10).

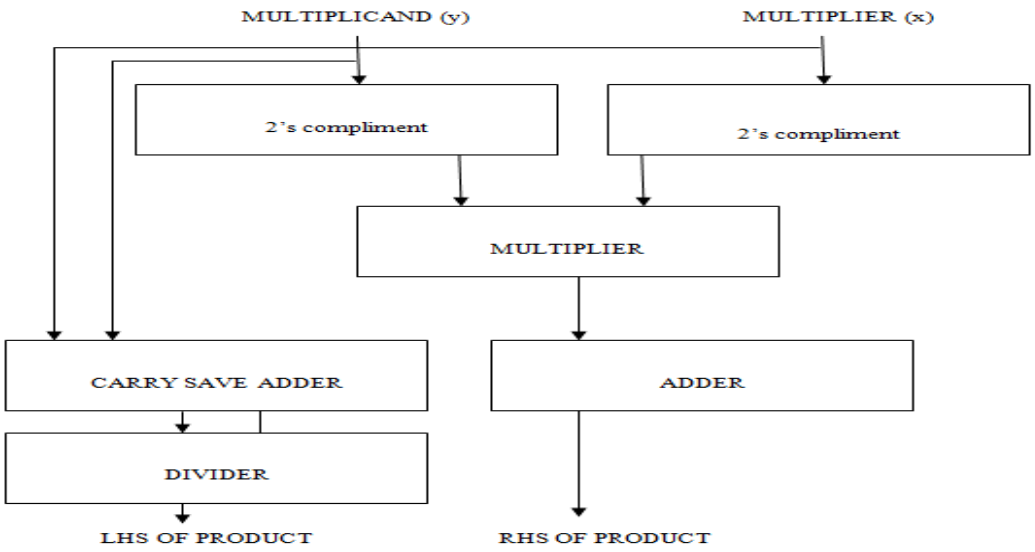

Figure 6.Structure of Anurupye Vedic Multiplier

This scheme is illustrated by consider the multiplication of two decimal numbers 58 x 48 by Anurupye method as shown in Fig 7.

Working base = 50

58 08

48 -02

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2)56 / -16

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28 / -16

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27 / (100-16)

= 27 / 84

= 2784

Figure 7.Multiplication Steps using Anurupye

3.4. Implementation of Sutras in Fast Fourier Transforms

Vedic algorithm is proposed for the implementation of multipliers that are used significantly in Fast Fourier Transform (FFT) and it provides fast and reliable approach to compute the N point DFT**.** Eq. 1. Shows the DFT function of X (k) that is an *N*-point sequence of x (n).

$X(k) = \sum_{n=0}^{N-1} x(n) \exp\{-j(2\Pi/N)kn\}, 0 \le k \le N-1$ ---- (1)

The simplified notation of DFT is mentioned in Eq. 2,

$X(k) = \sum_{n=0}^{N-1} x(n) W_N^{kn}, 0 \le k \le N-1$ ---------- (2)

where $W_N = e^{-j2\pi/N}$, represents the twiddle factor or "Nth root of unity".

4. RESULTS AND DISCUSSIONS

The Output window for 8x8 Anurupye Vedic Multiplier which was implemented in FFT is shown in Fig.8. It performs multiplication of two decimal numbers 58 x 48 by "If one is in ratio, the other is zero operation" (Anurupye method).

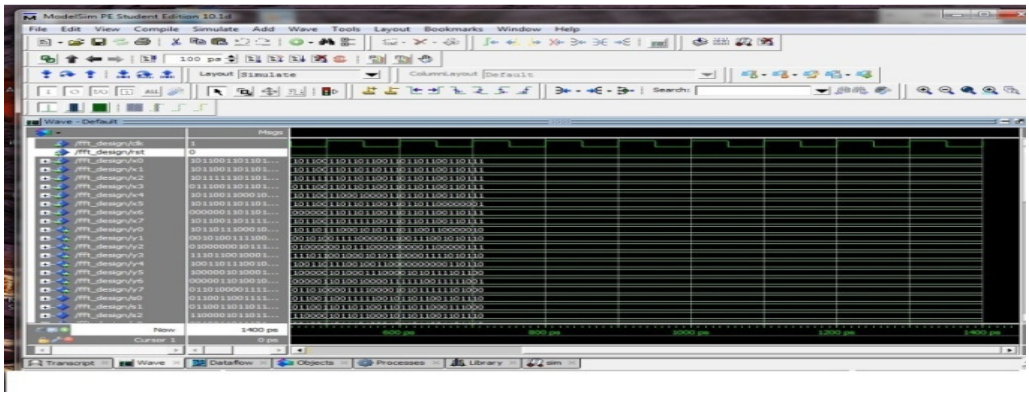

Figure 8.Simulation Output window for 8x8 Anurupye Vedic Multiplier which implemented in FFT

The Output window for 8x8 Urdhva Vedic Multiplier which was implemented in FFT is shown in Fig.9. It performs multiplication of two decimal numbers 154 x 142 by "Vertical and crosswise multiplications" (Urdhva- Tiryakbhyam method).

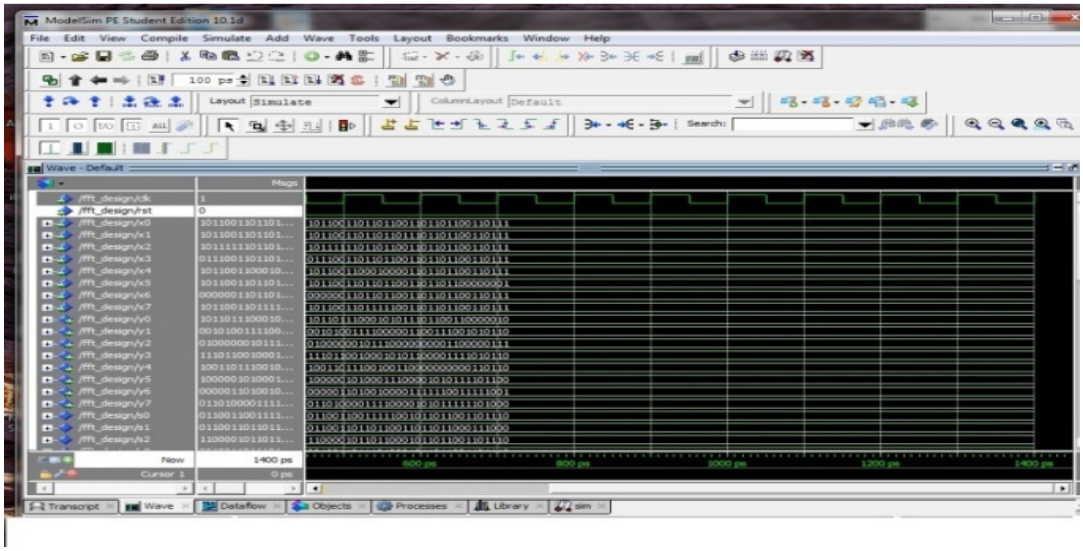

Figure 9.Simulation Output window for 8x8 Urdhva Vedic Multiplier which implemented in FFT

The Output window for 8x8 Nikhilam Vedic Multiplier which was implemented in FFT is shown in Fig.10. It performs multiplication of two decimal numbers 97 x 94 by "all from 9 and last from 10 operations" (Nikhilam method).

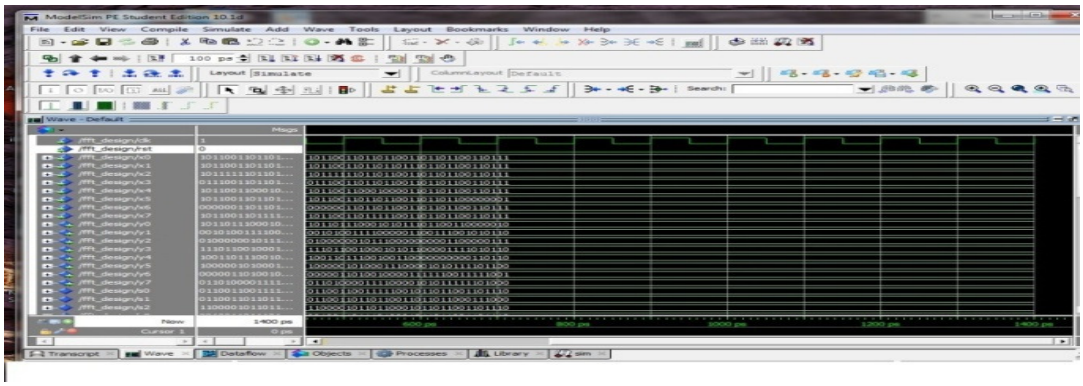

Figure 10.Simulation Output window for Nikhilam Vedic Multiplier which implemented in FFT

The performance analysis of Vedic multiplier with high speed and low delay are explained as in Table No.1.

Table 1.Performance of Vedic Multiplier in FFT

Vedic Multipliers Design in FFT	**Time Constraint(delay)**
8x8 Multiplier using Nikhilam sutra	25.196 ns
8x8 Multiplier using Urdhva sutra	20.844 ns
8x8 multiplier using Anurupye sutra	17 ns

5. CONCLUSION

The Vedic methods of multiplication "Urdhva Tiryakbhyam Sutra, Nikhilam Navatashcaramam Dashatah and Anurupye" are based on Vedic mathematics. It gives us method for hierarchical multiplier design and clearly indicates the computational advantages offered by Vedic methods. The computational path delay for proposed 8x8 bit Vedic multiplier on FFT is found to be minimized. Anurupye sutra on FFT is made efficient than Urdhva tiryabhyam and Nikhilam Navatashcaramam Dashatah sutras by more reduction in computation time. Hence the motivation to reduce delay is finely fulfilled.

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