ANALOG MODELING OF RECURSIVE ESTIMATOR DESIGN WITH FILTER DESIGN MODEL

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ABSTRACT

The low power solution for developing the application specific design methodologies using recursive coding had become central topic of modern research .In 3G mobile communication systems, in order to achieve low power consumption and high speed at low cost design. This paper focuses on implementing a design methodology using recursive encoder /decoder for optimizing the power and area and analyzing the performance interms of bit error rate (BER).

KEYWORDS

Power Optimization, Recursive Encoder/Decoder, low power design,

1. INTRODUCTION

In today's modern and competitive world as there is lot of advancements in research. Many application specific designs at various abstraction levels have been proposed in order to provide cost effective and efficient solutions. Special portable applications such as cellular phones, laptops and modems. The main criteria in these applications are maximizing the battery life by minimizing the power consumption [1, 2].

In digital integrated circuits, there is an enormous technological need of low power design [1]. The importance of power limiting and estimating the power consumption at different levels is described in [3-16]. The power estimation will help in improving the efficiency at various levels of design. There will be great impact on saving power at the lower level abstractions like circuit level and transistor level. Without illustrating brief about register transfer logic architecture, some researchers proposed a DSP design methodology in behavioral level starting from entry level to

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algorithmic level. They propose a design methodology using communication applications for performance analysis.

In 1993 recursive codes were presented. In the research society, recursive codes gathered enormous interest among researchers because of its high performance in low signal to noise ratio (SNR) in comparison to other codes. There will be lot of pressure in implementing these technologies in advance third generation (3G) systems and beyond. to limiting power the objective was to implement complex algorithms for limiting power consumption. Recursive coding is a forward error correction (FEC) scheme. Iterative decoding is the key feature of recursive codes [17, 18]. Recursive codes consist of concatenation of two convolution codes. To achieve high performance the [19, 20] proposed recursive codes and analyzed that the performance of recursive codes is better at low signal to noise ratio (SNR). Interestingly, the name Recursive was given to these codes because of the cyclic feedback mechanism (as in Recursive machines) to the decoders in an iterative manner. Recursive codes with short delay are being heavily researched. When the interleavers exceeds 200 bit length [21] proposed recursive coding whose performance is much better than the conventional convolution al and block codes. Similarly the [22] author proposed a device equipped with 32x32-bit interleaver to achieve high performance than the conventional concatenated codes with outer code using reed –Solomon and inner code using convolution code. Power minimization is an important aspect in remote areas so [23] proposed recursive coding for power minimization. Recursive algorithm are similar to that of the above two methods i.e. [21] and [22]. One aspect which differs between them is interleaving algorithm whose allowable input range and rate of constituent RSC encoders [24].

There are three types of algorithms used in recursive decoder namely MAP, Max-Log-MAP and Log-MAP. In order to minimize the probability of bit error MAP algorithm is used which results in high complexity and instability. This result in higher power consumption in coding and also requires larger area coverage to process. The solution to overcome the above mention problem is to operate in log-domain. The reason behind using is that the multiplication becomes addition and also a correction term in log domain and can be useful for maximization. So Max-Log-MAP algorithm in recursive decoder is used in this work. The approach of designing the recursive code or low power objective in logarithmic domain is focused and a evaluation on the consumption of power for such an operation is suggested.

2. SYSTEM DESIGN

For the implementation of a log-Max MAP approach a coding and decoding approach is been suggested. The computational complexity of the design unit is reduced by the optimal realization of the decoding approach in 5 distinct operations. The operation performed for the operation is as outlined in the following section. The objective of the iterative decoding algorithm is used to calculate the posteriori probability (APP) of the information symbols which shows the reliability of the each symbol.

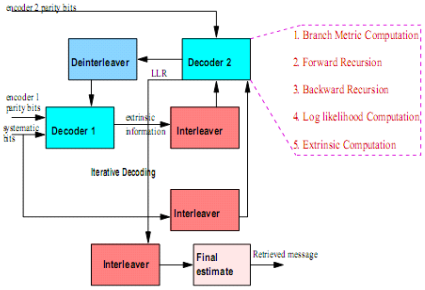


Figure 1: Decoder Schematic Diagram

There are five main computations to be performed during each iteration in the decoding stage as shown in the figure above.

1) Branch metric calculation

By using eqn. (1) one can calculate the branch metric and the branch metric is represented by states. Each state has two branches. As there are four states total eight branch metrics and each branch need to be calculated which is given by below eqn. (1)

$$\gamma[k] = x_s[k] \cdot z[k] + x_s[k] \cdot L_c \cdot y_s[k] + L_c \cdot x_p[k] \cdot y_p[k] \quad \ldots\ldots \quad \text{Eqn. (1)}$$

Where [k] is the branch metric at time k, [k] are the systematic bits of information with frame-length N, [k] is the information that is fed back from one decoder to the other decoder, L_c is the channel estimate which corresponds to the maximum signal to distortion ratio, is the encoded parity bits of the encoder, $x_s[k]$ is the noisy observed values of the encoded parity bits and $x_p[k]$ is the observed values of the encoded systematic bits.

2) Forward metric computation

The second computation step of decoding algorithm is the forward metric. The forward metric can be calculated from eqn.(2) which signify the probability of a state at time k, with the probabilities of states at previous time instance.

$$\alpha_s[k] = \sum_{s' \epsilon S} \alpha_{s'}[k-1] \gamma_{s',s}[k] \quad \text{------Eqn. (2)}$$

At a time instance K at each node the forward direction traversing for states 00,01,10,11 need to be calculated from the eqn. (2).Where the summation represents the total state transitions.

3) Backward metric unit

The third computational step of decoding algorithm is the backward metric the back metric can be calculated by using eqn.(3) in the backward direction. .The backward metric represents the probability of the state at each time k and the future received symbols, is recursively evaluated and stored

$$\beta_{s'}[k-1] = \sum_{s} \beta_s[k] \cdot \gamma_{s',s}[k] \quad \text{------Eqn. (3)}$$

In a 4 state decoder, $\beta_{s'}$ represents the state transition is calculated from states 00, 01, 10, 11. In an 8 state decoder - for states 000, 001,010, 011, 100, 101, 110 and 111 the 3GPP version is calculated.

4) Log likelihood ratio (lr)

The fourth computational step of the algorithm is Log likelihood ratio llr. The recursive decoder output is llr. At time k, llr ouput for each symbol is calculated by below eqn. (4)

$$llr[k-1] = ln\frac{\sum_{u_k=1} \alpha_{s'}[k-1]\beta_{s'}[k]\gamma_{s',s}[k]}{\sum_{u_k=0} \alpha_{s'}[k-1]\beta_{s'}[k]\gamma_{s',s}[k]} \quad \text{----Eqn. (4)}$$

Where input message bit is represented by U[k] 1. The numerator part in the eqn.(4) represents the summation of over all the states from S' to S in γ[k]. The γ values, α unit output and the β values obtained from the above steps are used to compute the llr values. The log likelihood ratio llr[k] for each γ[k] is computed. The reliability can be estimated using magnitude and the sign correspond to the hard decision

5) Extrinsic unit

In the extrinsic unit, extrinsic information need to be estimated which is given to the next decoder based on the order of iteration. The extrinsic information represented by ext[k-1] is computed by using log likelihood ratio given by llr[k-1] and subtracted the weighted channel systematic bits. The obtained information is fed to the other decoder.

The four state and 8 eight state encoders are implemented so as to analyze the performance by comparing the characteristics of both encoders. The difference between the four state and eight state encoder is the usage of memory elements that each encoder utilizes. The four state encoder utilizes two memory elements where as the eight state encoder utilizes three memory elements. This is the encoder that is specified in the 3GPP standards.

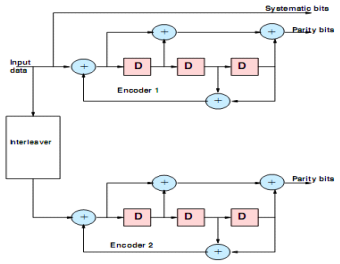


Figure 2: The 8 state encoder – 3GPP version

3. DESIGN MODULES

As soon as the decoding commences, the encoded data information is demultiplexed and separated into the systematic received data (ys), parity data elements from the encoder1 (yp1) and the parity

data values from the encoder2 (yp2).the information is then processed by a unit called interleaving unit. The output data of the interleaving process is provided as an input to the decoder units. The data is segregated with the help of data supply unit and provides the required input for the decoder1 and decoder 2 units.

Now the decoder 1 and decoder 2 are set for processing.

1) Decoder1

The decoder1 unit consist of the following blocks such γ, α, β, llr, extrinsic unit, intermediate storage units with associated feedback units, such as extrinsic interleaver and its storage units. By using FIFO/LIFO the storage units are modeled and pattern analysis is used for accessing the data which was illustrated in the previous chapter.

2) Decoder2

As decoder2 has similar block that were used in decoder1, except inputs are different in the computational blocks the ther difference between the decoder 1 and decoder2 is tat the decoder2 is equipped with an additional decision unit which is not present in the decoder1. The functionality of the decision units is it gives the final estimation values of the retrieved message..In order to process the next iteration the output of decoder2 is stored and fed back to the decoder1.

B) Selector module

In order to carry the processing of second iteration to the sixth iteration a specific selector module in the recursive decoder is required. Decoder receives the encoded data as an input. During first iteration, The encoded data is multiplexed and generates respective parity bits and then data is proceed to interleaving process. After the completion of the interleaving process is data is stored. This process continues for the second till sixth iteration for decoder1 and decoder2. During first iteration the selector module (multiplexer) collect the input signal from the data and provides a start signal to the decoder1 (unit). During the successive iterations, the input signal is collected by the selector module from the last computational unit and gives a start signal to the enable the decoder2 (extrinsic interleaver unit) unit.

C) FSM Controller Unit

The process of the proposed recursive decoder is controlled and managed by a unit called Finite state machine (FSM) controller unit. The proposed recursive decoder unit consist of two decoder with six iteration to perform it operation. In order to control and manages the set of states, Finite state machine (FSM) is required. In recursive decoder, for each iteration, A transition signal is moved from present state to next state. In the recursive decoder the data computation and the iteration control are differentiated by the FSM, which has a typical algorithmic behavior.

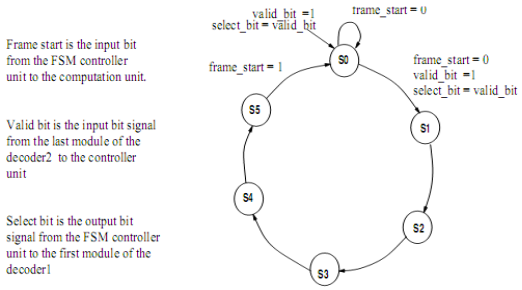


Figure 3: State diagram representation of FSM used in the recursive decoder design

Figure 3 depicts the state diagram of the FSM used in the recursive decoder design to control the number of iterations. In FSM of the recursive decoder design the there are six states S0 to S5. The first iteration starts from state S0 which represents the initial state of the FSM of the recursive decoder design. As there are six states, it requires six iteration where the data need to be received by each stage and get processed. Based on the value of the frame start signal, the decoding process either enables or disable. If the value of the frame start signal is zero (low) then the decoding process of the decoder is disabled. If the value of the frame start signal is one (high) then the decoding process of the decoder enable. Based on the number of iteration the signal of the decoder unit is send to next state and is controlled by the FSM unit. In order to The recursive decoder module requires many memory modules in its design, so as to facilitate the opportunity from which memory location, the data need to read or write with appropriate conditions is specified in the module. In Xilinx, during systhesis process the internal RAM memory of VirtexII device is used for realizing the modules.

4. RESULT ANALYSIS

The proposed design is modeled in active HDL and synthesized in Xilinx synthesizer. For power analysis the Xpower analyzer in xilinx helps in evaluating the power by reading the pre-routed and post routed design data of the device. By using the 0.18m technology the estimated voltage of the design is 2.5V. There is a provision to give a specific switching activity for the design power estimation. The estimates for 20 and 50 activity factor are found. Xpower analyzer of the Xilinx tool one can calculate the power of each element in the design or total power consumed by the whole design.The estimated power consumed is product of capacitance, square of the voltage, activity factor and frequency of operation and its units are mW.

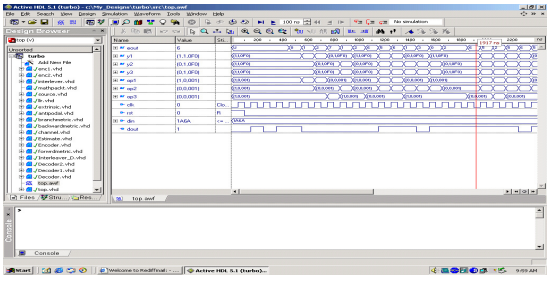


Figure 4: simulation observation illustrating timing result for the developed encoding unit

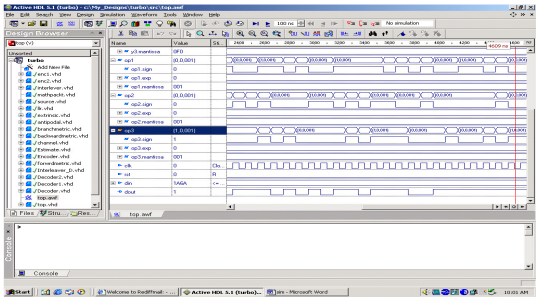


Figure 5: simulation timing observation for the decoding logic developed for the implemented system.

For the realization of the developed logic and its evaluation in physical environment in this work the developed system is synthesized on Xilinx ISE synthesizer targeting on to virtex2p device part number 2vp100ff1696-6. The obtained parameter for this device is given below,

Design Statistics: # IOs : 19
Cell Usage : # BELS : 6549
Maximum Frequency: 141.012MHz

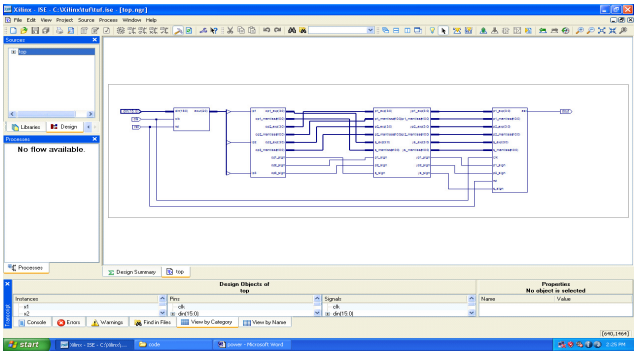


Figure 6: obtained RTL realization for the encoding unit

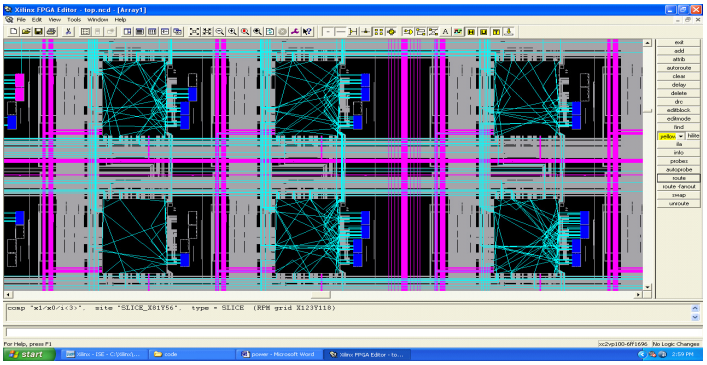


Figure 7. The routed logical operation for the developed system onto the targeted FPGA device.

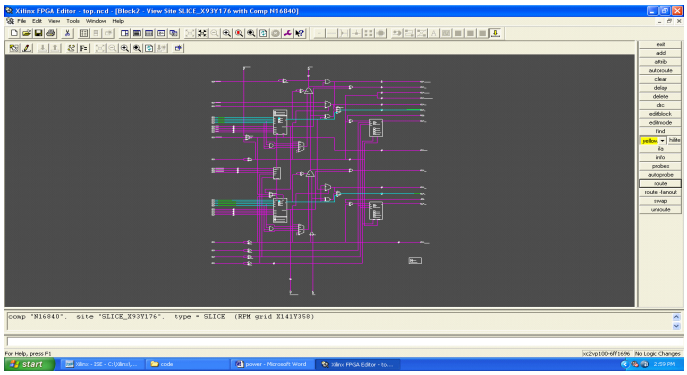
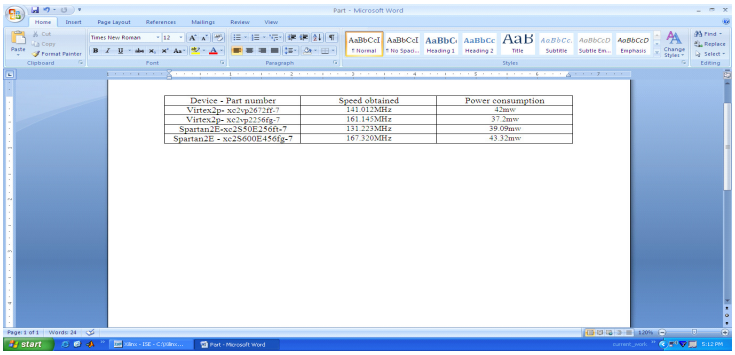


Figure 8. Logical placement of the logical blocks on a targeted FPGA logic.

The summarized observation for different targeted FPGA devices were outlined below,



Device - Part number	Speed obtained	Power consumption
Virtex2p- xc2vp2672ff-7	141.012MHz	42mw
Virtex2p- xc2vp2256fg-7	161.145MHz	37.2mw
Spartan2E-xc2S50E256ft-7	131.223MHz	39.09mw
Spartan2E - xc2S600E456fg-7	167.320MHz	43.32mw

5. CONCLUSION

Based on memory issues, this paper proposed a an application specifc design methodology by using low power design techniques. In communication system for achieving low power consumption using low cost design an recursive coding is used in forward error correction channel coding. Recursive coding uses three steps 1. For simplified decoding, parallel concatenation of codes is allowed. For better weight distribution an interleaving concept is introduced and to maximize the gain of the decoder a soft decoding is used for improving decoder decisions. The proposed methodology developed in Active HDl and evaluated the performance using Xilinx synthesizer. By using different target devices of PLD's, the proposed method is evaluated. The target devices varies from 37.2-43.32mw of power and 131.223 – 167.320MHz of frequency variation.

REFERENCES

[1] A. P. Chandrakasan, S. Shang and R. roderson, "Low Power CMOS Digital Design, "IEEE Journal of Solid State Circuits, vol. 27, no. 4, April 1992, pp. 478-483.

[2] Jan Rabaey, Digital Integrated Circuits - A design perspective, Eastern Economy Edition, Prentice Hall India, 1997.

[3] Q. Wu, C. Ding, C. Hsieh and M. Pedram, "Statistical Design of Macro-models For RT-Level Power Evaluation," Proceedings of the Asia and South Pacific Design Automation Conference, Jan. 1997, pp. 523-528.

[4] D. L. Liu and C. Svensson, "Power Consumption Estimation in CMOS VLSI Chips, "IEEE Journal of Solid State Circuits, vol. 29, no. 6, June 1994, pp.663-670.

[5] C. Y. Tsui, J. Monterio, M. Pedram, S. Devadas and A. M. Despai, "Power estimation in Sequential logic circuits," IEEE Transaction on Low Power Systems, vol. 3, no. 3,Sep. 1995, pp.404-416.

[6] M. Kamble and K. Ghose, "Analytical Energy Dissipation Models for Low Power Caches," Proceedings of the International symposium on Low Power Electronics and Design, Aug. 1997, pp.143-148.

[7] H. Kojima, D.Gomy, K. Nitta, and K. Sasaki, "Power Analysis of a Programmable DSP for Architecture/Program Optimization," In IEEE Symposium on Low Power Electronics, Digest of Tech. Papers, Oct. 1995, pp. 26-27.

[8] H. Mehta, R.M. Owens, M. J. Irvin, R. Chen and D. Ghosh, "Techniques for low energy software," International Symposium on Low Power Electronics and Design, Aug. 1997, pp. 72-75.

[9] T. Indermaur and M. Horowitz, "Evaluation of charge recovery circuits and adiabatic switching for low power CMOS design," Proceedings of the 1994 Symposium on Low-Power Electronics: Digest of Technical Papers, Oct 1994, pp. 102-103.

[10] D. Somashekhar and K. Roy, "Differential current switch logic: A low power DCVS logic family," IEEE Journal of Solid-State Circuits, vol.31, no.7, July 1996, pp.981-991.

[11] R. Gonzalez and M. Horowitz, "Energy dissipation in general purpose Microprocessors," IEEE Journal of Solid-State Circuits, vol.31, no.9, Sep. 1996, pp.1277-1284.

[12] Kanad Ghosh, "Reducing energy requirement for Instruction Issue and dispatch in superscalar Microprocessors," International Symposium on Low Power Electronics and Design, July 2000, pp.231-234.

[13] H. Mehta, R. M. Ovens and Mary Jane Irwin, "Energy Characterization based on Clustering,"33rd Design Automation Conference, Las Vegas, Nevada, June 1996, pp.702-707.

[14] Naehjuck Chang, Kuranho Kim and H. G. Lee, "Cycle accurate Energy consumption measurement and analysis: Case study ARM7 TDM1," International Symposium on Low Power Electronics and Design, Italy, July 2000, pp. 185-190.

[15] C. Piguet et al., "Low Power Design of 8-b Embedded CoolRISC Microcontroller Cores, "IEEE Journal of Solid-State Circuits, vol. 32, no. 7, July 1997, pp.1067-1078.

[16] T. Sato, M. Nagamatsu and H. Tago, "Power and Performance Simulator: ESP and its Applications for 100 MIPS/W Class RISC Design," IEEE Symposium on Low Power Electronics, San Diego, CA, USA, October 1994, pp. 46-47

[17] M. Valenti, "Iterative Detection on Decoding for Wireless Communications," PhD dissertation, Virginia Polytechnic Institute and State University, July 1999.

[18] C. Berrou, A. Galvieux and P. Thitimajshima, "Near Shannon Limit Error-Correcting Coding and Decoding: Recursive Codes," Proceedings ICC 93, Geneva Switzerland, May 1993, pp. 1064-1070

[19] Tranter, W.; Taylor, D.; Ziemer, R.; Maxemchuk, N.; Mark, J., "Near Optimum Error Correcting Coding and Decoding: TurboCodes " Wiley-IEEE Press 2007.

[20] D. Divsalar and R. J. McEleice, "Effective free distance of recursive codes," Electronics Letters, vol. 32, no. 5, Feb. 1996.

[21] Bee Leong Yeap, Tong Hooi Liew, Hamorsky, J. Hanzo, L "Comparative study of turbo equalization schemes using convolutional, convolutional turbo, and block-turbo codes" Wireless Communications, IEEE Transactions on Volume: 1 , Issue: 2 2002

[22] Valadon, C.G.F.; Tafazolli, R.; Evans, B.G. "Performance evaluation of concatenated codes with inner trellis codes and outer Reed-Solomon code" IEEE Transactions rolume: 49 , Issue: 4 2001.

[23] Qingchun Chen; Wai Ho Mow; Pingzhi Fan "Some New Results on Recursive Convolutional Codes and Their Applications " IEEE 2006.

[24] Liao, Xin; Ilow, Jacek; Al-Shaikhi, Al "Trellis Termination in Turbo Codes with Full Feedback RSC Encoders" 6th International ITG-Conference on Source and Channel Coding (TURBOCODING), IEEE 2006