

# DESIGN OF HIGH EFFICIENCY TWO STAGE POWER AMPLIFIER IN 0.13UM RF CMOS TECHNOLOGY FOR 2.4 GHZ WLAN APPLICATION

Shridhar R. Sahu<sup>1</sup> and Dr. A. Y. Deshmukh<sup>2</sup>

<sup>1</sup>Research Scholar, Department of Electronics Engineering, G. H. Raisoni College of Engineering, Nagpur, India

sahu.rs1404@gmail.com

<sup>2</sup>Professor, Department of Electronics Engineering, G. H. Raisoni College of Engineering, Nagpur, India

aydeshmukh@gmail.com

## ABSTRACT

A two stage CMOS power amplifier is implemented in 0.13 $\mu$ m RF CMOS technology using ADS tool operating at 2.4 GHz with dc supply of 2.5 V. Driver stage as the input stage and power stage as the output stage are the two stages. A cascode topology is used in the driver stage and basic topology is used in the power stage. Output power at 1dB compression point is 20.028 dBm and maximum output power delivered by this circuit is 22.002 dBm. Power added efficiency calculated at 1 dB compression point is 44.669 % whereas the maximum power added efficiency comes out to be 70.196 %. The input return and output return losses are -11.132 dB and -12.467 dB respectively. Isolation loss and small signal gain are calculated to be -61.889 dB and 43.745 dB respectively. This circuit shows power gain of 42.728 dB at 1dB compression point. The total dc current flowing through this circuit is 0.0901 A. MOSFET only bias circuits are used to reduce total dc current. This circuit is designed for application in WLAN.

## KEYWORDS

RFIC, RF CMOS, PAE, Impedance Matching, Cascode Topology

## 1. INTRODUCTION

Radio Frequency Integrated Circuits (RFIC) are integrated circuits operated in radio frequency range. RF Power Amplifiers are part of the transmitter front-end, and are used to amplify the input signal to be transmitted [1][3].

The main performance parameters for the power amplifier are the level of output power it can achieve, depending on the targeted application, linearity, and efficiency. There are two basic definitions for the efficiency of the power amplifier. The drain efficiency (DE) is the ratio between the RF output power to the dc power dissipated, and the power added efficiency (PAE) which is the ratio between the difference of the RF output power and the RF input power to the total dc power of the circuit. The PAE is a more practical measure as it is responsible for the power gain of the amplifier [1].

$$PAE = \frac{P_{out(RF)} - P_{in(RF)}}{P_{dc}} \quad (1)$$

$$DE = \frac{P_{out(RF)}}{P_{dc}} \quad (2)$$

RFICs are fabricated using CMOS, GaAs, SiGe BiCMOS, Hetero-Junction Bipolar Transistor (HBT), High Electron Mobility Transistor (HEMT) technologies. Existing power amplifiers mostly use GaAs (Gallium Arsenide) or GaN (Gallium Nitride) for high output power. But it also leads to high power dissipation, large chip area and more cost. The GaAs technology provides high output power at high frequency, but it is quite expensive and the uniformity of the device structure may be affected due to process variations [6]. The GaN process also operates at higher frequencies and deals with high power capacity but due to wide band gap materials used more voltage supply is needed for operation which in turn leads to high power dissipation [7].

CMOS power amplifiers can also be operated at high frequencies and by using some techniques output power can be increased. CMOS power amplifiers show more linearity as compared to GaAs and GaN technologies. As CMOS can operate on low power supplies there is drastic decrease in overall power dissipation of the circuit and hence better PAE can be expected. CMOS power amplifiers are cost effective and use minimum chip area for fabrication.

As power amplifiers are extensively used in transceivers it's better to have a device dissipating less power and having less chip size operating at the same frequency, achieving similar gain, power added efficiency and return losses. The main objective behind this paper is to design a CMOS Power Amplifier for 2.4 GHz WLAN application because of its low power consumption, less chip size and thereby provide trade-off between output power, power added efficiency and dc input power.

A two stage CMOS Power Amplifier is described here. The tool used for designing this circuit is ADS (Advanced Design System) tool of Agilent Systems. This circuit is designed in RFCMOS 0.13µm technology provided by ADS tool. The layout of this paper is follows: Initially this paper deals with the design methodology implemented for designing this high efficiency CMOS Power Amplifier then it discusses the results obtained after simulation. Finally, conclusions are drawn out after observing the simulation results.

## 2. DESIGN METHODOLOGY

### 2.1. Block Diagram

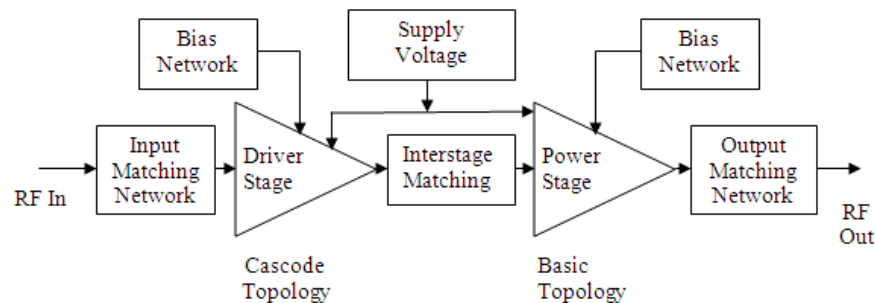


Figure 1: Block Diagram of complete two stage CMOS Power Amplifier

The above figure shows the functional block diagram of the designed two stage Power Amplifier. Input matching and Output matching networks are used at input and output stage respectively to minimize return losses which results in increased gain and output power. Input matching is done by calculation of input impedance using the ratio of the input voltage and input current. Passive elements having some impedance are connected at the input side forming a input matching network to match this impedance. The loss occurred in this part of the circuit due to improper matching is known as Input return loss and denoted as  $S_{(1,1)}$ . The same concept is utilized to find  $S_{(2,2)}$  at the output side. An interstage matching network is also used as two stages are used for power amplification.

Driver stage and Power stage with the supply and bias network are main blocks of the power amplifier. A cascode topology is used in the driver stage and a basic power amplifier topology is used in the power stage. MOSFET-only biasing circuit is used for biasing of the both stages. The circuit is operated in 2.4 GHz ISM band.

## 2.2. Complete Two Stage Power Amplifier

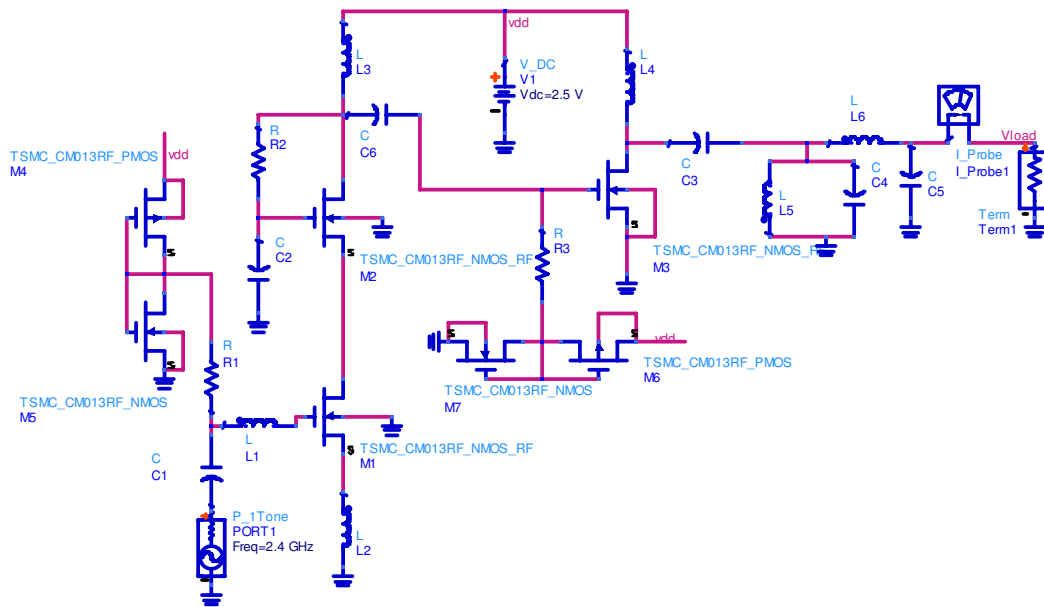


Figure 2: Schematic of complete Two Stage CMOS Power Amplifier

### 2.2.1. Driver Stage

Driver stage is the first of the two stages of the power amplifier circuit. A cascode topology is implemented in the driver stage. The transistor M1 is the main amplifying device of this stage and transistor M2 is cascaded with M1. An inductor of a large value is connected between the drain of M2 and VDD. This inductor which opposes the change in current and the cascaded transistor is to prevent large flow of drain current through M1 which can damage the transistor. The transistor M2 is biased in saturation by connecting a resistor between gate and drain. A low value capacitor is connected between drain and ground to discharge the current which may flow through gate. The main amplifying device in this stage, transistor M1 is biased by a MOSFET only bias circuit whose output is 0.5 Volts to operate in triode region. The transistor was first analyzed with different biasing voltages and found to be operating better at 0.5 V in similar conditions. This biased voltage is fed to the transistor M1 through a resistor R1 and the gate inductance. As mentioned in the block diagram an input matching network is connected to the driver stage i.e.,

the input stage for input impedance matching. For this matching purpose gate inductance  $L_g$  ( $L_1$ ) and source inductance  $L_s$  ( $L_2$ ) are used. The values of these inductances and the size of the transistors are such selected that the operation of the circuit is tuned to the resonance frequency of 2.4 GHz. The gate length of the transistors is fixed at 130nm and the width of gate is varied. Bulk of both the transistors is connected to ground. The output power of this topology is not as high as the power stage but the isolation provided between output and input is very high. Also the dc power consumed by this circuit is far less than the power stage circuit. The dc current through this stage is 6.31 mA.

### **2.2.2. Power Stage**

The second stage of the designed two stage CMOS power amplifier is known as the power stage as it is mainly responsible for power amplification considering the overall circuit. The size of the transistor used in this stage is large as compared to the size the transistors used in the driver stage. A big fat inductance is connected between the dc supply and the drain of the transistor M3. This inductor opposes any change in dc current flowing through the drain and source of the transistor and thereby controls the flow of current through the transistor. The output of the driver stage is fed to the gate of the transistor M3 through the capacitor C6. As this is the power stage the transistor is allowed to conduct higher amount of current essential for power amplification. The dc current here is controlled by varying the size of the transistor. The amplification of the signal also depends on the bias voltage supply. The circuit was initially biased with 0.5 V where satisfactory results were observed. After this, the circuit was tested with different bias voltages ranging from 0.5 V to 1 V. Best results were observed in 0.75 V. Beyond 0.75 V the output power increased but the s-parameters were unsatisfactory. As shown in the block diagram the power stage is connected to output matching network for output impedance matching. Here, a LC tank circuit is designed for matching purpose and to tune the circuit to its operating frequency, so that the output return loss is better at resonance frequency. The total dc current of this stage comes out to be 83.5 mA.

### **2.2.3. Input Matching**

Matching networks are an integrated part of RFICs. Every circuit has its own input and output impedances. Before applying matching networks the input and output side were terminated by impedances of 50 ohms using a function for the same in ADS tool. For input matching two inductors were used, one of which was connected between the gate and input and the other between source and ground. The value of source inductance  $L_2$  is kept very low around 0.1 nH. The gate inductance  $L_1$  value is varied to accordingly to be tuned resonance frequency of 2.4 GHz. This matching is responsible for the input return loss. If this matching is perfect then there should be no power reflected back at the input side transmitted from the source.

### **2.2.4. Output Matching**

Output matching is responsible for output return loss, output power and also gain of the circuit. A LC tank circuit with a series-parallel connection of inductor and capacitor is used for output matching network. The tank circuit is mainly for tuning the output part of the circuit to the fundamental resonance operating frequency 2.4 GHz. It was found that there was a considerable increase in output power after inclusion of this network at the output side. The values of the matching elements may it be input or output also depends of the size of the transistors used for amplification.

### 2.2.5. Bias Circuit

Two types of bias circuits were tried in this circuit. First one was the resistor-MOSFET bias and then the MOSFET only bias. The MOSFET only bias circuit was chosen because of its less power consumption as compared to the resistor-MOSFET bias which contributes to the total dc current of the circuit. Basic n-channel and p-channel transistors were used instead of RF NMOS or RF PMOS as used for amplification. The sizes of the transistors were selected according to the bias supply required, 0.5 Volts for driver stage and 0.75 V for power stage. Both bias circuits consumed total 0.268 mA.

## 3. SIMULATION RESULTS

S – Parameters are an important part of Power amplifiers. There are four s-parameters essential to observe after designing a power amplifier. They are input return loss  $S(1,1)$ , output return loss  $S(2,2)$ , gain  $S(2,1)$  and isolation loss  $S(1,2)$ . Input return loss subjects to the amount of power reflected back after transmitting from the source at the input. Ideally there should be no reflection of power at the input during transmitting. Practically it should be as small as possible. As shown in figure 3, the input return loss of this amplifier is -11.132 dB at 2.4 GHz which means that 27.7 % of transmitted power is reflected back at the input side. Output return loss gives the idea about the power reflected back after transmitting from the antenna at the output side. In figure 4 output return loss is shown which comes out to be -12.467 dB at 2.4 GHz which states that 23.8% of output power is reflected back. Gain of the circuit also known as forward transmission coefficient is the fraction of output voltage and input voltage. It shows the amount of gain obtained at the output with respect to input. In figure 5, gain of 43.745 is observed at 2.4 GHz. Figure 6 shows the isolation loss graph where -61.889 dB of isolation loss is observed which states that there is  $\approx$  100 % isolation of input from output. This graph describes how well the input of the circuit is isolated from the output. Observing the figures it can be seen that best results are obtained at the operating frequency of the amplifier i.e., 2.4 GHz. This is because of the input and output matching networks connected at the input of the driver stage and output of the power stage respectively. These simulations were carried out using s-parameter palette by sweeping the values of frequency from 0 to 5 GHz with a step size of 100 MHz.

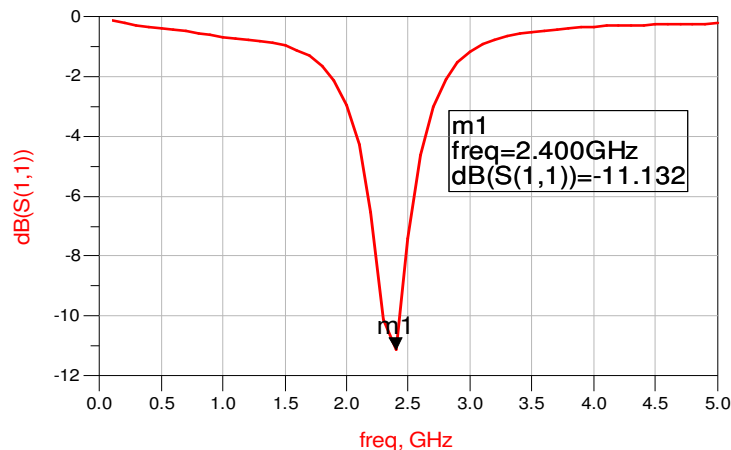


Figure 3: Input Return Loss

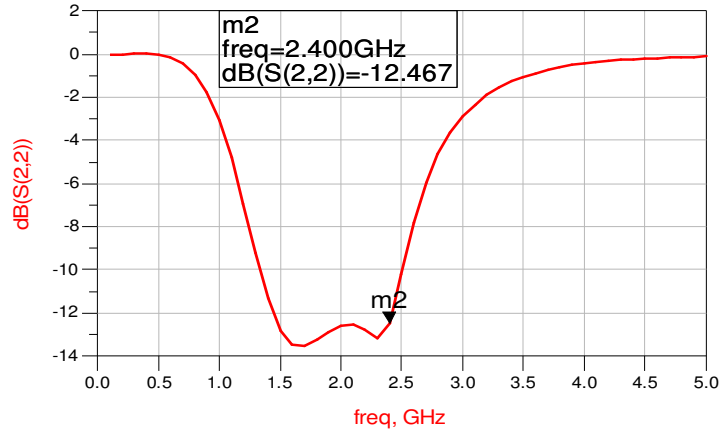


Figure 4: Output Return Loss

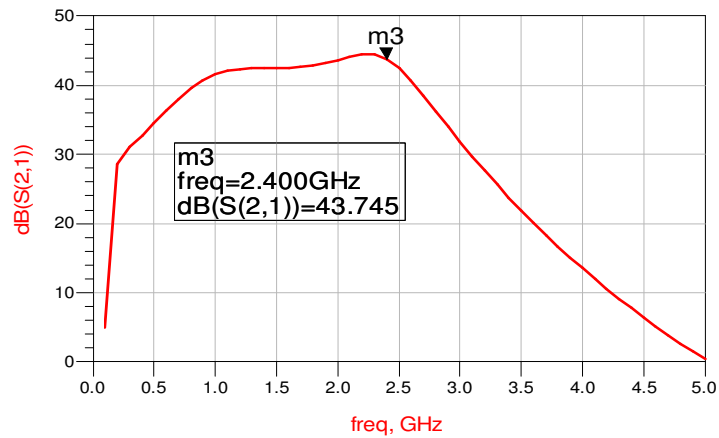


Figure 5: Gain

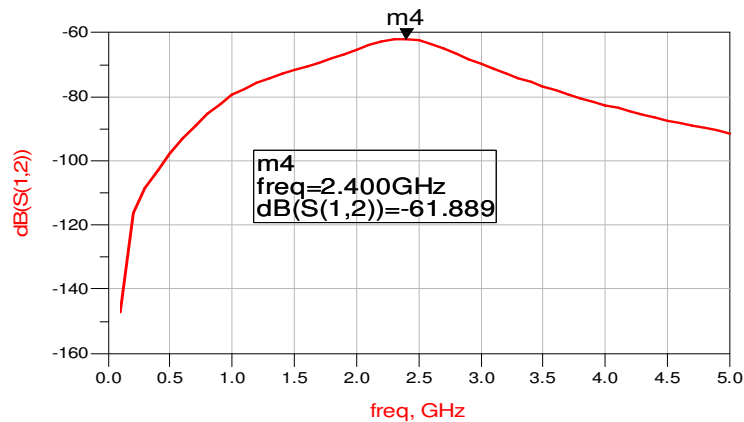


Figure 6: Isolation Loss

After obtaining the s-parameters, focus shifts to the most important results as far as the power amplifier is concerned. Basically power calculations are carried out at 1dB compression point of the gain of the circuit. As shown in the figure 7, graph of gain in dB is plotted v/s input power in dBm. First a marker is set at maximum gain available of the circuit and the other at that point where the gain compresses approximately by 1dB. According to the figure 1dB compression

point is obtained at -22.7 dBm of input power. Now, output power is observed at the same input power which comes out to be 20.008 dBm. This can be observed in figure 8. This output power is known as output power at 1dB compression point. The maximum output power delivered by this circuit is 22.002 dBm. This amount of output power is considered to be on the higher range as CMOS technology is used instead of GaAs or GaN which are high power handling devices. From the graph, it can be seen that output power has a linear increase with increase in input power but as crosses the 1dB compression point, it stays approximately constant. The unit used for power calculations of a power amplifier is dBm instead of watts. The conversion of watts to dBm and dBm to watts is given as in equation (3). The equation for power gain is given as in equation(5).

$$P(dBm) = 10 \times \log\left(\frac{P(W)}{1mW}\right) \quad (3)$$

$$P(W) = 10^{\left(\frac{P(dBm)}{10} - 3\right)} \quad (4)$$

$$P(dB) = 10 \times \log\left(\frac{P_{out}(W)}{P_{in}(W)}\right) \quad (5)$$

The power gain will vary with changing values of  $p_{out}$  and  $p_{in}$  but power gain at 1dB compression point is 42.728 dB. All power calculations were carried with the help of HB simulation palette in harmonics of order 5.

Power added efficiency; the factor by which the power amplifiers are analyzed is the deciding parameter between different types of power amplifiers. This CMOS power amplifier operating at 2.4 GHz with a main supply of 2.5 V gives PAE of 44.669 % at 1dB compression point. The maximum PAE achieved by the circuit is 70.196 %. These values can be observed in figure 8 where on left y axis  $p_{out}$  is plotted and on right y axis PAE is plotted. The equations for the same are given as

$$PAE_{1dB} = \frac{P_{out(1dB)}(W) - P_{in(1dB)}(W)}{P_{dc}(W)} \quad (6)$$

$$PAE_{max} = \frac{P_{out(max)}(W) - P_{in}(W)}{P_{dc}(W)} \quad (7)$$

$$P_{dc} = V_{dd} \times I_{dc} \quad (8)$$

This two stage CMOS power amplifier achieves high efficiency because of low operating voltage and low dc current flowing through the circuit. Figure 9 and figure 10 show noise figure and stability factor respectively of the circuit at 2.4 GHz. The total dc current delivered by the supply to the circuit is 90.1 mA. All the results and specifications are presented in a tabular format in table 1.

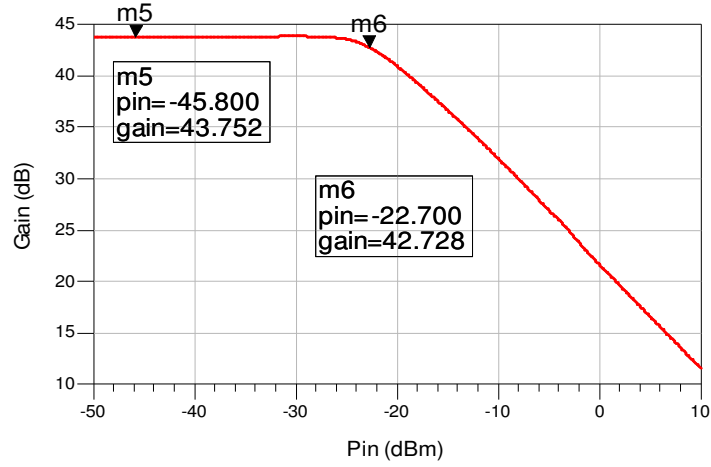


Figure 7: Gain v/s Input Power

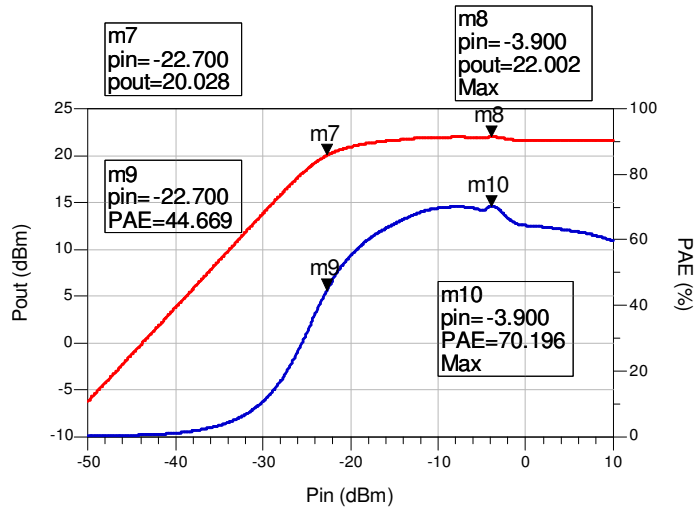


Figure 8: Output Power and PAE v/s Input Power

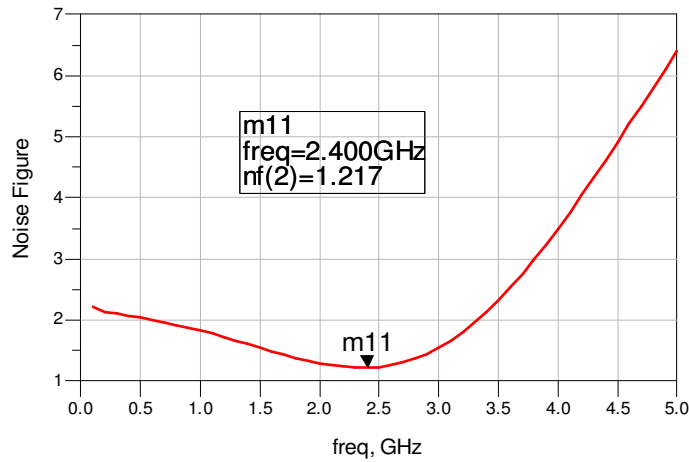


Figure 9: Noise Figure



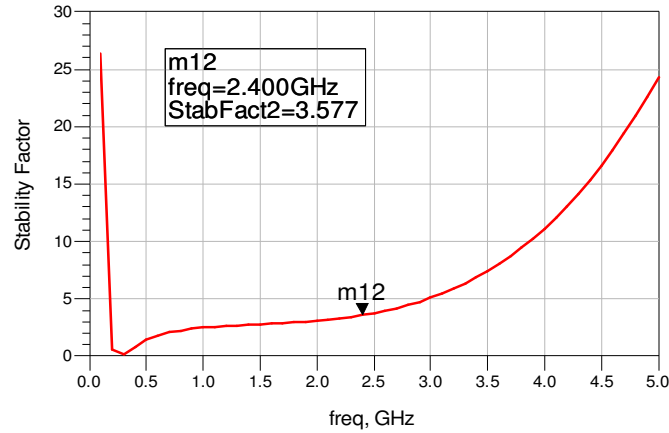


Figure 10: Stability Factor

Table 1. CMOS Power Amplifier Specifications.

Parameters	Value
Operating Voltage	2.5 V
Technology	0.13 $\mu\text{m}$ RF CMOS process
Operating Frequency	2.4 GHz ISM Band
$S_{(1,1)}$ Input Return Loss	-11.132 dB
$S_{(2,2)}$ Output Return Loss	-12.467 dB
$S_{(2,1)}$ Gain	43.745 dB
$S_{(1,2)}$ Isolation Loss	-61.889 dB
$P_{\text{out}(1\text{dB})}$ Output Power at 1dB compression point	20.028 dBm
$P_{\text{out}(\text{max})}$ Maximum Output Power	22.002 dBm
Power Gain at 1dB compression point	42.728 dB
Total DC Current	0.0901 A
PAE <sub>(1dB)</sub> Power Added Efficiency at 1dB compression point	44.669 %
PAE <sub>(max)</sub> Maximum Power Added Efficiency	70.196%

#### 4. CONCLUSIONS

High output power with high efficiency is obtained using CMOS device for the power amplifier. As shown in the results this power amplifier dissipates low amount of power and therefore is responsible for high efficiency. Efficiency can be increased or decreased depending on the power requirement of the target device and vice-versa. Output power of 20.028 dBm with PAE of 44.669% is obtained at 1dB compression point which meets the IEEE 802.2 b/g standards for WLAN applications. After observing the results it can be concluded that CMOS RF Power Amplifiers can replace GaAs HBT and GaN HEMT Power Amplifiers if the power requirement is of the same range as high efficiency is achieved with CMOS power amplifiers

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## AUTHORS

### Shridhar R. Sahu

Shridhar R. Sahu was born in Mumbai, India on 14th April 1989. He obtained his B. E. degree in Electronics and Telecommunication Engineering from Saraswati College of Engineering, Mumbai University in 2010. He completed his M. Tech degree in VLSI from G. H. Raisoni College of Engineering, Nagpur in 2013. He is currently working as Assistant professor in Department of electronics and telecommunication engineering, Saraswati College of Engineering. His areas of interests are VLSI and MEMS.



### Dr. A. Y. Deshmukh

Dr. A. Y. Deshmukh completed his Ph.D from VNIT Nagpur in 2010. He is currently working as Professor (Electronics Engg.) & Dean (Quality and Planning Assurance) at G. H. Raisoni College of Engineering Nagpur, India. He is also working as Coordinator TEQIP-II (World Bank Assistance Project) and Associate Dean (R&D). He is Technical Committee Member of IEEE Soft Computing, USA. He is also Counselor of IEEE Students Branch. He has to his credit around 45 International Conference and Journal Publications. He has also worked as International Co-Chair for ICETET-08, ICETET-09, ICETET-10, ICETET-11, ICETET-12 (International Conference on Emerging Trends in Engineering & Technology). He has worked as Reviewer & Session Chair for many conferences. He has also worked as Guest Editor for International Journal IJSSST. He received research grant from AICTE. He has received Best Teacher Award in 2004 at GHRCE.

