# LOW COST REVERSIBLE SIGNED COMPARATOR

Farah Sharmin[1], Rajib Kumar Mitra[2], Rashida Hasan[3], Anisur Rahman[4]

Department of Computer Science and Engineering
[13]{University of Dhaka, Dhaka-1000, Bangladesh}
[2]{Patuakhali Science and Technology University, Dumki-8602, Bangladesh}
[4]{Daffodil International University, Dhaka-1207, Bangladesh}

## *ABSTRACT*

*Nowadays exponential advancement in reversible computation has lead to better fabrication and integration process. It has become very popular over the last few years since reversible logic circuits dramatically reduce energy loss. It consumes less power by recovering bit loss from its unique input-output mapping. This paper presents two new gates called RC-I and RC-II to design an n-bit signed binary comparator where simulation results show that the proposed circuit works correctly and gives significantly better performance than the existing counterparts. An algorithm has been presented in this paper for constructing an optimized reversible n-bit signed comparator circuit. Moreover some lower bounds have been proposed on the quantum cost, the numbers of gates used and the number of garbage outputs generated for designing a low cost reversible signed comparator. The comparative study shows that the proposed design exhibits superior performance considering all the efficiency parameters of reversible logic design which includes number of gates used, quantum cost, garbage output and constant inputs. This proposed design has certainly outperformed all the other existing approaches.*

## *KEYWORDS*

*Reversible Comparator, Quantum Computing, Signed Arithmetic, Low Power.*

## 1. INTRODUCTION

In recent time every sort of computation is getting complex and researchers are facing enormous challenges over billions of arithmetic operations per second. According to Gordon Moore, the transistor count and performance of logic circuits is doubled in every two years [1], this process will continue until semiconductor circuits reach to its physical limit. Thus achieving ultra-speed computation leads us to various kinds of computing technology such as Quantum Information Processing [2], DNA Computing [3], etc. But we live in a world of classical or irreversible architecture where unused energy is dissipated due to power loss. This is because, Landauer [4] proved erasure of each bit of information dissipates at least $KT \times \ln 2$ joules of energy where $K$ is the Boltzamann's constant and $T$ is the absolute temperature at which the operation is being performed. In 1973, Bennet [2, 5] had shown that energy dissipation problem of VLSI circuits can be overcome by using reversible logic. This is so because reversible computation does not erase any bit of information and consequently it does not dissipate any energy for computation. Generally, reversible logic performs Boolean operations having equal number of inputs and outputs where input states are uniquely mapped to individual output states or vice versa [6]. Also reversible logic should never permit feedbacks. Reversible logic does multiple operations per cycle without losing any input bits. As a result zero power dissipation would be achieved if a logic circuit consists of reversible gates. Reversible logic can easily be manipulated for Fault

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Testing [5], Embedded Devices [7], Digital Signal Processing [8], Quantum Dot Cellular Automata [9-10], etc.

Comparison of two binary numbers finds its wide application in general purpose microprocessors, communication systems, encryption devices, sorting networks, etc [11]. This paper presents an *n*-bit signed comparator which has less number of gates, produces less garbage outputs and quantum cost. In the process of designing this architecture, two very efficient reversible gates RC-I and RC-II have also been proposed. Quantum realization of these two gates shows that they significantly improve the overall cost of the proposed *n*-bit signed binary comparator. With the help of theorems and lemmas the efficiency of reversible logic synthesis of *n*-bit signed comparator has also been proved in this paper. This design is based on the reversible comparator gate RC-I which produces 2 outputs $q= xLy$ (*x* less than *y*)= $x'y$ and $r= xGy$ (*x* greater than *y*)= $xy'$ and RC-II gate which produces 3 outputs $r= xEy$ (*x* equals *y*)= $(x \oplus y)'$, $q= xLy$ (*x* less than *y*)= $x'y$ and $p= xGy$ (*x* greater than *y*)= $xy'$. RC-I has been used to compare two single bits whereas RC-II compares two signed bits therefore they are named as Reversible Comparator gate RC-I and RC-II.

The paper is organized with the following sections: Section 2 gives the idea about the reversible gate, basic definition and quantum realization of some reversible circuits which have been used in this work. Evaluation of some existing approaches of designing reversible comparator has been focused in Section 3. Section 4 introduces the proposed logic synthesis of reversible *n*-bit signed comparator. Section 5 gives the simulation results of all the proposed circuits and comparison with the other existing researches. Finally the paper concludes in section 6 highlighting the future direction of the proposed work.

## 2. BACKGROUND STUDY

Before going into the detail of reversible *n*-bit signed comparator, some preliminaries on reversible computations and related topics have been discussed in this section.

### 2.1. Reversible Gate

Reversible Gate is an $n \times n$ data stripe block which uniquely maps between input vector $I_v= (I_0, I_1, \ldots I_n)$ and output vector $O_v = (O_0, O_1, \ldots O_n)$ denoted as $I_v \leftrightarrow O_v$ [12].

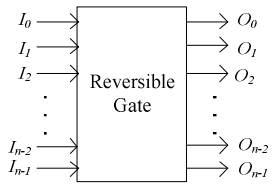


Figure 1. A $k \times k$ Reversible Gate

### 2.2. Gate Count(GA)

Total number of reversible gates used in a circuit isconsidered to be as gate count (GA) [13]. Figure 2 shows that the required number of Peres gates (PG) for implementing a reversible full adder circuit is 2 (i.e GA=2).

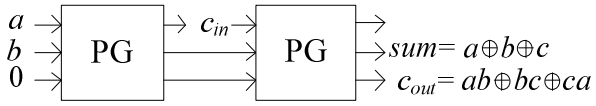


Figure 2. Reversible Full Adder Circuit Realization using Two Peres Gates

## 2.2. Garbage Count (GB)

Every gate output that is not used as input to other gates or not considered to be as a primary output is known as Garbage. Therefore garbage count is the total number of garbage outputs generated from a circuit. Figure 2 shows two garbage outputs are generated while realizing a full adder circuit using Peres gates (i.e GB=2).

## 2.3. Quantum Cost (QC)

Every quantum circuit is built from 1 × 1 and 2 × 2 quantum primitives and its cost is calculated as a total sum of 2 × 2 gates used since 1 × 1 gate costs nothing i.e. zero. Basically the quantum primitives are matrix operation which is applied on qubits state. All the gates of the form 2 × 2 has equal quantum cost and the cost is unity i.e. 1 [14]. Since every reversible gate is a combination of 1 × 1 or 2 × 2 quantum gate, therefore the quantum cost of a reversible circuit calculates the total number of 2 × 2 gates used. The quantum cost of reversible full adder in Figure 2 is 8 (i.e QC= 8).

## 2.4. Constant Input (CI)

Total number of constant inputs in a reversible circuit is often referredas Ancilla Inputs [14]. Figure 2 shows that the totalnumber of ancilla input or constant input used to construct the reversible full adder is 1 (i.e CI= 1).

## 2.5. Feynman Gate

Let $I_v$ and $O_v$ be the input and output vector of a 2 × 2 Feynman gate, (FG) [15] respectively, where $I_v = (a, b)$ and $O_v = (p=a, q= a \oplus b)$. FG gate is used to perform copy or invert operation, as shown in Figure 3.

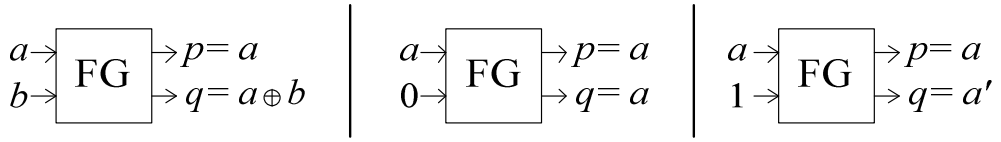


Figure 3. Reversible 2 × 2 Feynman gate and corresponding copy and invert operations

## 2.6. Peres Gate

Let $I_v$ and $O_v$ be the input and output vector of a 3 × 3 Peres Gate (PG) [16] respectively shown in Figure. 4(a), where $I_v = (a, b, c)$ and $O_v = (p = a, q = a \oplus b, r = ab \oplus c)$. The quantum cost of Peres gate is 4 [16] which has been shown in Figure 4(b).

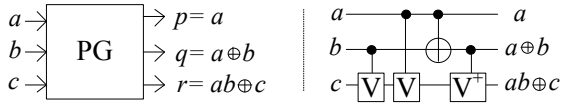


Figure 4(a). Reversible 3 × 3 Peres Gate and (b) It's Equivalent Quantum Realization

## 2.6. TS-3 Gate

Let $I_v$ and $O_v$ be the input and output vector of a 3 × 3 TS-3 gate [17] respectively, where $I_v$ = (*a, b, c*) and $O_v$ = ($p$ = *a, q* = *b, r* = $a \oplus b \oplus c$) which has been shown in Figure 5(a). Its equivalent quantum cost realization circuit has been shown in Figure 5(b) which indicates that it has QC of only 2.

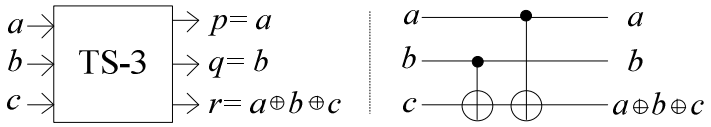


Figure 5(a). Reversible 3 × 3 TS-3Gates and (b) It's Equivalent Quantum Realization

## 2.7. RC-I (Reversible Comparator) Gate

A new 3 × 3 reversible gate has been proposed in this work which produces two outputs indicating whether a single bit binary number *x* is greater than another single bit binary number *y* or *x* is less than *y*. Therefore it has been named as Reversible Comparator gate RC-I. Figure 6 shows RC-I gate along with its state mapping. State mapping shows that there are $2^3$= 8 states for this proposed reversible gate. Each circle denotes all possible input states of the reversible 3 × 3 RC-I which directs to its corresponding output state. That means the state mapping shows unique input-output mapping of the proposed reversible RC-I.

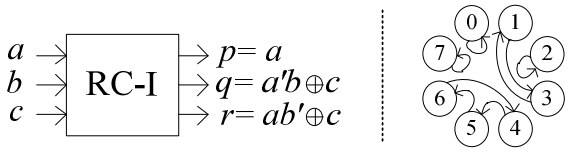


Figure 6. Reversible 3 × 3 RC-I Gate and Corresponding State Mapping

This proposed gate has been used to construct a single bit comparator circuit shown in Figure 7 as it produces two outputs indicating *x* less than *y* and *x* greater than *y*.

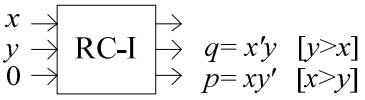


Figure 7. Application of RC-I as a Single Bit Comparator Circuit

## 2.8. RC-II (Reversible Comparator) Gate

In this paper, another new 4 × 4 reversible gate has been proposed which produces three outputs indicating whether a single bit binary number *x* is greater than another single bit binary number *y* or *x* is less than *y*or *x* equals *y*. It has been named as Reversible Comparator gate RC-II. The

proposed gate has been shown in Figure 8 together with its state mapping. Since it is a 4 × 4 reversible gate, state mapping diagram shows that there are $2^4$ = 16 states for this reversible gate. Each circle denotes all possible input states of the reversible 4 × 4 RC-II gate which directs to its corresponding output state. That means the state mapping shows unique input-output mapping of the proposed RC-II.

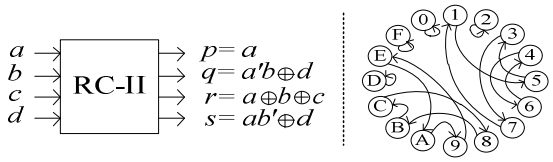


Figure 8. Reversible 4 × 4 RC-II Gate and Corresponding State Mapping

RC-II gate has been used to construct a reversible sign bit comparator shown in Figure 9. It generates three outputs *q*= *y* greater than *x*, *r*= *x* equals *y* and *p*= *x* greater than *y* when it is comparing two unsigned numbers.

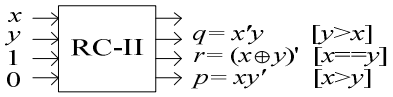


Figure 9. Reversible Sign Bit Comparator including Equal Option

## 2.9. Quantum Cost Realization of Reversible Circuit

In Quantum Computing, single data unit is called qubit and the value of qubit is the superposition of constant |0> and |1>. Any quantum operation is a unitary matrix and it performs multiplying the state of qubit which then generates resultant state [18]. Single bit quantum NOT works on single qubit, where the resultant state of qubit is the inverted of prior state (shown in Figure 10).

$$|0\rangle = \begin{bmatrix} 1 \\ 0 \end{bmatrix} \quad |1\rangle = \begin{bmatrix} 0 \\ 1 \end{bmatrix} \quad \text{NOT} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \quad \Big| \quad \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} 1 \\ 0 \end{bmatrix} = \begin{bmatrix} 0 \\ 1 \end{bmatrix}$$

Figure 10. Matrix Representations of Single Qubit Limits i.e. |0>or |1> and Quantum NOT Operation. The Operational Behaviour of Quantum NOT Operation can be Achieved by Multiplying |0> state of Qubit using NOT Matrix

### 2.9.1 Square Root of NOT Quantum Primitive

Square Root of NOT (SRN) operation is the square root of 2 × 2 NOT matrix called V [19]. Any unitary matrix, ($U^+$) is called hermitian matrix of U if $UU^+$= I (Identity Matrix). Operational behaviour of V and $V^+$ can be written as VV= $V^+V^+$ = NOT and $VV^+$= $V^+$V= I (shown in Figure 11) [20].

$$V = \sqrt{\text{NOT}} = \left( \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \right)^{1/2} = \frac{1+i}{2} \begin{bmatrix} 1 & -i \\ -i & 1 \end{bmatrix} \quad \Big| \quad V^+ = \frac{1-i}{2} \begin{bmatrix} 1 & i \\ i & 1 \end{bmatrix}$$

Figure 11. Matrix Representation of Square Root of NOT (SRN) gate i.e. V, where $V^+$ is the Hermitian Matrix of V

### 2.9.2 Behaviour Analysis of Quantum XOR Operation

Two quantum XOR acts on two-input qubit and corresponding 4 × 4 unitary matrixes, (UC) and its behaviour can be expressed as shown in Figure 12.

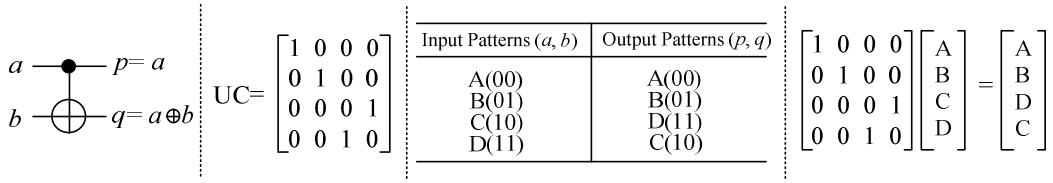


Figure 12. Quantum XOR; Matrix Representation of Quantum XOR Operation i.e. 4 × 4 UC; Input-Output States (A, B, C and D) Mapping of Quantum XOR Gate; Multiplying Input States of using UC to Generate Corresponding Output states which is similar to the State Table

### 2.9.3 Quantum Realization of Toffoli Gate

As shown in Figure 13, a 3 × 3 Toffoli gate propagates its first two inputs to its first two outputs , while the third output performs a logic operation on all three inputs. Total number of 2 × 2 Quantum gates to realize Toffoli operation is 5. The operational behaviour of controlled inputs (*a*, *b*) over input *c* is shown in Figure 14(a-e). The quantum Toffoli gate is also called as Controlled Controlled NOT (CCN) gate which can perform according to the Algorithm. 1 as follows:

**ALGORITHM 1. Quantum Cost Calculation of Controlled Controlled NOT gate**

**Input:** *a*, *b* and *c*
**Output:** *p*= *a*, *q*= *b* and *r*= *ab*⊕*c*
**Start**
**If**($a = 1$ && $b = 1$)**Then** $r = c'$ [Use two controlled Vs as shown in Figure 14c]
**End If**
**If**($a = 0$ &&$b = 1$)| |($a = 1$ &&$b = 0$)**Then** $r = c$
[Add a XOR and $V^+$ neutralizes V's as shown in Figure 14d]
**End If**
**If**($a = 0$ &&$b = 0$) **Then** $r = c$
[Both Vs and $V^+$ are remain deactivated but 2nd output in Figure 14e is not similar to TG]
**End If**
[Use of another XOR can neutralize 2nd output to *q*= *b* (shown in Figure 14f)]
**End**

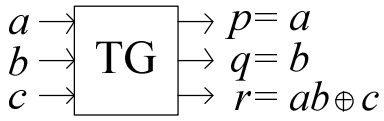


Figure 13. Reversible 3 × 3 Toffoli Gate

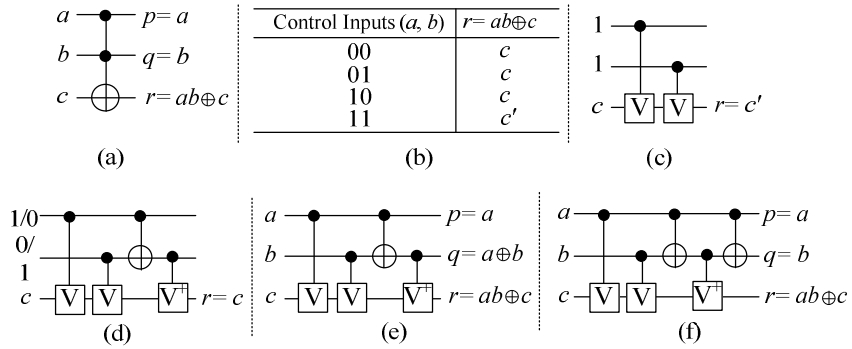


Figure 14. Quantum Realization of Controlled Controlled NOT (CCN) gate: (a) Symbolic Notation of Toffoli Gate, (b) Value of 3rd Output Controlled by *a* and *b* Inputs (c) Realization of NOT Operation, (d) Neutralization of the Effect of Vs when a⊕b= 1, (c) Projection of all Equations after Calculating 3rd Output *r* and (e) Equivalent Quantum Realization of Toffoli Gate

Quantum cost of RC-I and RC-II gates can be realized using Toffoli gate. Thus the quantum cost of Reversible Comparator gate RC-I and RC-II is 4 and 5 respectively shown in Figure 15(a) and 15(b).

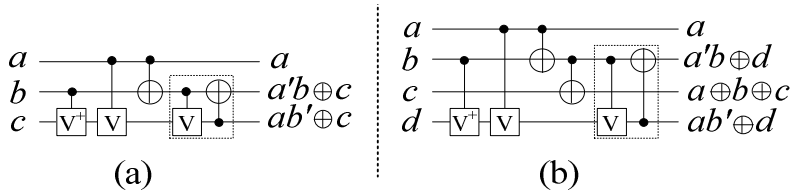


Figure 15. (a) Equivalent Quantum Realization of RC-I and (b) RC-II gates

Analysis on equivalent quantum circuit of any reversible circuit and corresponding cost minimization technique has been described in [21, 22].

## 3. EXISTING WORK

The existing reversible design of the binary comparator is a serial architecture in Ref.[23] which has the latency of O(*n*) [24]. In this design approach, the comparator consisted of a chain of reversible comparison cells that performed the operation of comparing a bit of the first number say *x* with the corresponding bit of the second number say *y* [24]. In Ref.[23], a 1-bit comparator cell was designed using reversible Toffoli gates, Feynman gates and the NOT gates. But in Ref.[23], the design of reversible comparator has not been generalized for *n*-bit. Another design approach of the reversible binary comparator was tree based in Ref.[24]. The existing reversible binary tree comparator had a binary tree structure in which each node consisted of a 2-bit reversible binary comparator that can compare two 2-bit numbers $x(x_i, x_{i-1})$ and $y(y_i, y_{i-1})$, to generate 2-bit outputs indicating whether $x(x_i, x_{i-1}) > y(y_i, y_{i-1})$ or $x(x_i, x_{i-1}) < y(y_i, y_{i-1})$ [24]. The existing approach has been further illustrated with the design of 8-bit and 64-bit reversible comparators [24] but it has not been generalized for *n*-bit. There was another approach [25] that showed the reversible design of 1-bit binary comparator. In Ref. [25], a 1-bit comparator has been designed with many popular reversible gates but again the design has not been generalized further for *n*-bit. In recent time, some quality work has been done on this reversible architecture of comparator. Among which Ref.[26] introduces a tree based comparator where an *n*-bit sequential comparator has been designed. It was capable of producing bitwise AND, bitwise OR, *A* greater than *B*, *A* less than *B* and *A* equals to *B* outputs. This sequential design incurs a cost of 17*n*-12 and

$5n$-1 garbage outputs [26]. In the same paper, the sequential architecture has been modified to implement $n$-bit tree based comparator. Tree based architecture also incurs quantum cost of $17n$-12 which is identical to the sequential design. This reversible design of comparator [26] is based on two gates RC and UPG proposed in [26] which have been extensively used to create a 4-bit and 8-bit reversible comparator. Ref. [26] has brought significant improvement in quantum cost over previously presented tree based comparators.

## 4. PROPOSED DESIGN

This section presents the architecture of proposed reversible $n$-bit signed comparator. The construction process includes a sign bit comparator circuit and a sign bit comparator module which later on has been extended to create 2-bit, 8-bit, 64-bit and $n$-bit comparators.

### 4.1. Sign Bit Reversible Comparator Circuit

In this paper, a sign bit reversible comparator circuit using only one gate named RC-II has been proposed. This gate is shown in Figure 16 which produces three outputs indicating whether a sign bit of a binary number $x$ is greater than another sign bit of a binary number $y$ or $x$ is less than $y$. RC-II gate incurs quantum cost QC of 5, gate count (GA) of 1, garbage count (GB) of 1 and constant inputs (CI) of 2. When we compare two signed numbers, the one with msb (most significant bit) 0 is always greater than the one with msb 1. It means that the sign bit comparator circuit shown in Figure 16 works slightly different from the circuit shown in Figure 9 as it has to produce an output $q = x$ greater than $y$ when $x$ is 0 and $y$ is 1.

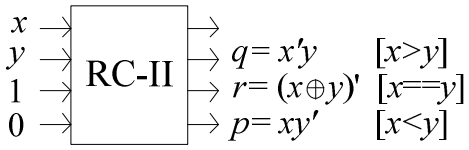


Figure 16. Reversible 4 × 4 RC-II Gate as a Sign Bit Comparator Circuit

### 4.2. Single Bit Reversible Comparator Module

A reversible single bit comparator module has been designed in this subsection which consists of one RC-I gate, two PG gates and one TS-3 gate. This module produces $x$ less than $y$, $x$ greater than $y$ and $x$ equals to $y$. It takes $(n\text{-}2)_{th}$ bits of two binary numbers $x_n$ and $y_n$ and three more inputs $p_{n-1}$, $q_{n-1}$, $r_{n-1}$ which are the results of comparing previous $(n\text{-}1)_{th}$ bits of the two binary numbers. Thus the module produces three outputs $x$G$y$, $x$L$y$ and $x$E$y$ which indicate whether the given numbers $x_n$ and $y_n$ are equal to each other or one greater/less than the other. This proposed circuit has been shown in Figure 17.

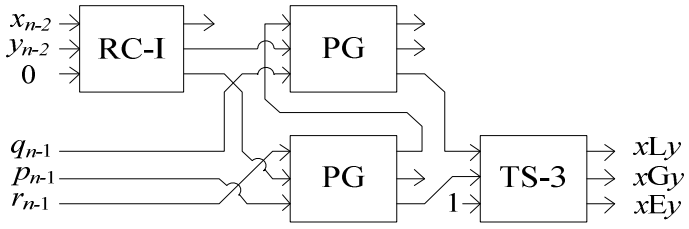


Figure 17. Proposed Design of Reversible Single Bit Comparator Module

### 4.3. 2-bit Reversible Comparator Design

This subsection shows the reversible design of a 2-bit binary comparator which consists of the proposed reversible sign bit comparison circuit and a single bit comparison circuit. In Figure 18, we can see the reversible design of 2-bit binary comparator where 5 reversible gates have been used to realize the functionality. Cost factor analysis of the proposed designhelps use to determine the value of the efficiency parameters. 5 is the total garbage outputs where the number of constant inputs is 4 and total quantum cost of the proposed circuit is 19.

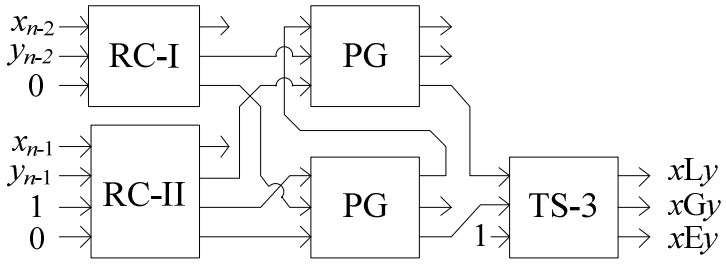


Figure 18. Proposed Design of Reversible 2-bit Comparator Circuit

### 4.4. 8-bit Reversible Comparator Design

A reversible 8-bit comparator circuit has been proposed in this paper shown in Figure 19. Total 29 gates have been used here to generate an 8-bit comparator circuit. 29 garbage outputs are produced and the number of constant inputs required is 16. This reversible architecture is certainly low cost as the total number of QC is 103. Table 1 has shown that this design is more efficient than the existing counterparts.

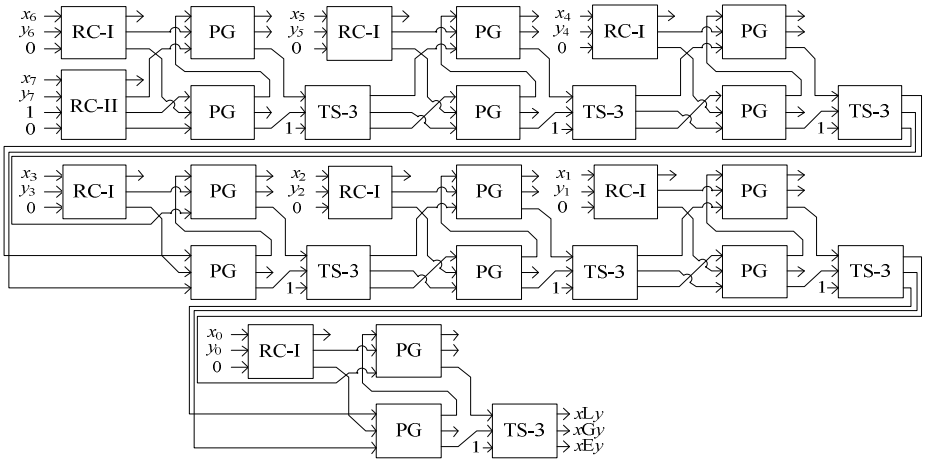


Figure 19. Proposed Design of Reversible 8-bit Comparator Circuit

### 4.5. 64-bit Reversible Comparator Design

Figure 20 shows the proposed reversible 64-bit comparator circuit of this paper. Total 253 gates are required to complete the design where 253 garbage outputs are produced and the number of

constant inputs is 128. This reversible architecture is certainly low cost as the total number of QC is 887 comparing to the existing researches shown in Table 2

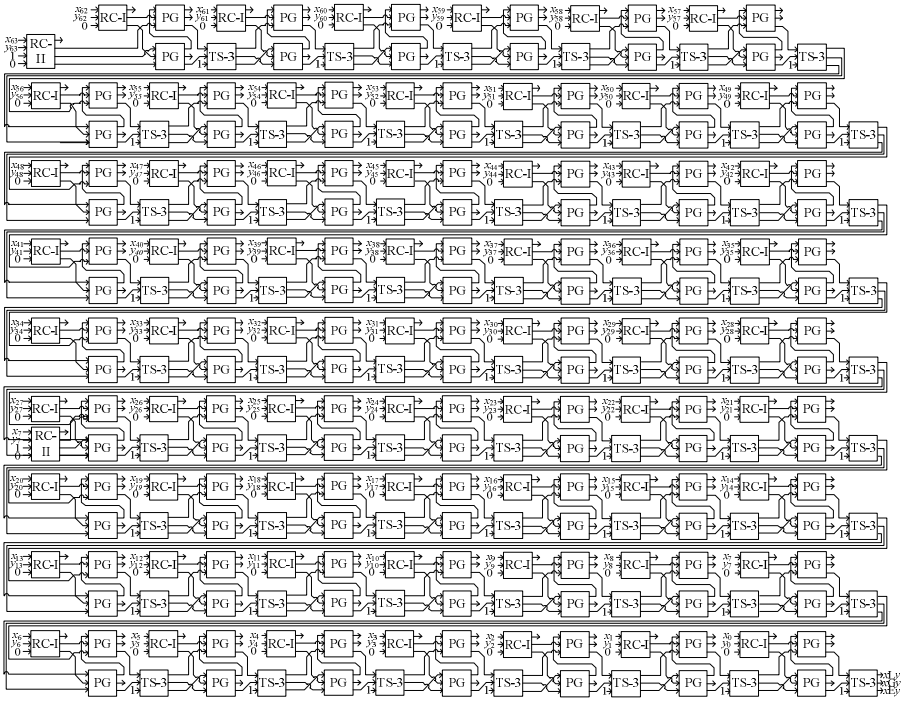


Figure 20. Proposed Design of Reversible 64-bit Comparator Circuit

## 4.6. *n*-bit Reversible Comparator Design

An *n*-bit reversible binary comparator has been proposed in this work. Figure 21 shows this architecture which consists of one sign bit comparison circuit and (*n*-1) single bit RC module. The algorithm for constructing an *n*-bit reversible comparator is given in Algorithm 2.

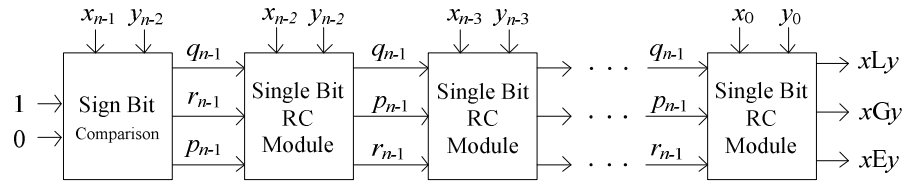


Figure 21: Proposed Design of Reversible *n*-bit Comparator Circuit

**ALGORITHM 2. *n* -bit Reversible Comparator when *n*≥ *2***

**1.** Take one Input Circuit $I_n$. Outputs of this block are considered to be of Level $L_n$.

**2.** a) **For each** $n_{th}$ input of two *n*-bit numbers

1. $I_n[I_1]$= $n_{th}$ input of $A_n$
2. $I_n[I_2]$= $n_{th}$ input of $B_n$
3. $I_n[I_3]$ = 1
4. $I_n[I_4]$ = 0

b) **If** $I_n[I_1] < I_n[I_2]$ then

$I_n[O_1] = q_{Ln}=1$

**Else if** $I_n[I_1] > I_n[I_2]$ then

$I_n[O_2] = p_{Ln} = 1$

**Else**

$I_n[O_3] = r_{Ln} = 1$

**EndIf**

3. **For each** single bit comparison circuit Level of Inputs and Outputs are considered to be of $L_n$ and $L_{n-1}$ respectively.
4. **Loop**

**For** $j = 1$ to $n-1$

i. Take one single bit comparator module $C_j$

ii. **If** $j = 1$ then

$C_j[I_1] = I_n[O_3] = r_{Ln}$
$C_j[I_2] = I_n[O_2] = p_{Ln}$
$C_j[I_3] = I_n[O_1] = q_{Ln}$
$C_j[I_4] = (n-1)_{th}$ input of $A_n$
$C_j[I_5] = (n-1)_{th}$ input of $B_n$

**Else**

$C_j[I_1] = C_{j-1}[0_3] = r_{Ln-1}$
$C_j[I_2] = C_{j-1}[0_1] = p_{Ln-1}$
$C_j[I_3] = C_{j-1}[0_2] = q_{Ln-1}$
$C_j[I_4] = (n-1)_{th}$ input of $A_n$
$C_j[I_5] = (n-1)_{th}$ input of $B_n$

iii. **Endif**

5. **End Loop**
6. **End**

---

**Theorem 1:** Let $n$ be the bits of two binary numbers. A reversible $n$-bit binary comparator can be realized with at least $4n-3$ gates which produce at least $4n-3$garbage bits when $n \geq 2$.

**Proof:** The proposed 2-bit reversible comparator shown in Figure 18 has been realized with 4.2-3= 5 reversible gates which produce at least 4.2-3= 5 garbage bits. Again the proposed 8-bit comparator shown in Figure 19 has been realized with 4.8-3= 29 reversible gates which in turn produce at least 4.8-3= 29 garbage bits. In the same way the proposed reversible 64-bit comparator contains 4.64-3= 253 gates and 4.64-3= 253 garbage outputs which have been shown in Figure 20. Thus we can say that the $n$-bit reversible comparator can be realized with at least $4n-3$ gates which in turn produce $4n-3$ garbage outputs where $n \geq 2$.

**Theorem 2:** Let $n$ be the bits of two binary numbers. A reversible $n$-bit binary comparator can be realized with at least $14n-9$ quantum cost when $n \geq 2$.

**Proof:** The proposed 2-bit reversible comparator shown in Figure 18 has been realized with at least quantum cost of 14.2-9= 19. Again from the Figure 19, the proposed reversible 8-bit comparator can be realized with at least 14.8-9= 103 quantum cost. In the same way the 64-bit reversible comparator can be realized with 14.64-8= 887 quantum cost shown in Figure 20. Finally we can say that the proposed reversible $n$-bit comparator will be realized with at least quantum cost of $14n-9$ where $n \geq 2$.

**Theorem 3:** Let $n$ be the bits of two binary numbers. A reversible $n$-bit binary comparator can be realized with at least $2n$ constant inputs when $n \geq 2$.

**Proof:** The proposed 2-bit reversible comparator shown in Figure 18 has been realized with at least constant inputs of 2.2= 4. Again from the Figure 19, the proposed reversible 8-bit comparator can be realized with at least 2.8= 16 constant inputs. In the same way the 64-bit reversible comparator can be realized with 2.64= 128 constant inputs shown in Figure 20. Finally we can say that the proposed reversible *n*-bit comparator will be realized with at least 2*n* constant inputs where $n \geq 2$.

## 5. SIMULATION AND COMPARISON

The proposed designs of reversible binary comparators have been functionally verified through simulations in DSCH. The simulation results show that the comparators give perfect output for all possible combinations of inputs. The simulation results for 1-bit, 2-bit, 3-bit and 4-bit reversible binary comparator are shown in Figure 22, 23, 24 and 25 respectively.

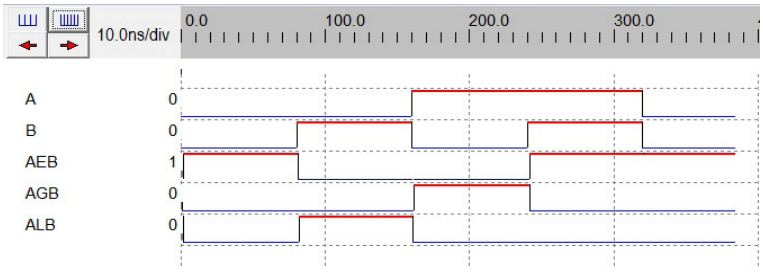


Figure 22. Simulation Result of Reversible 1-bit Comparator

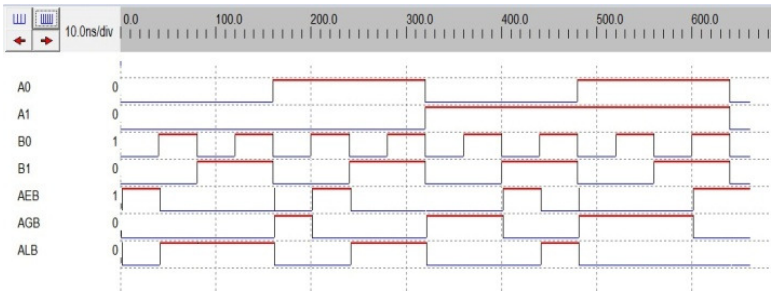


Figure 23. Simulation Result of Reversible 2-bit Comparator

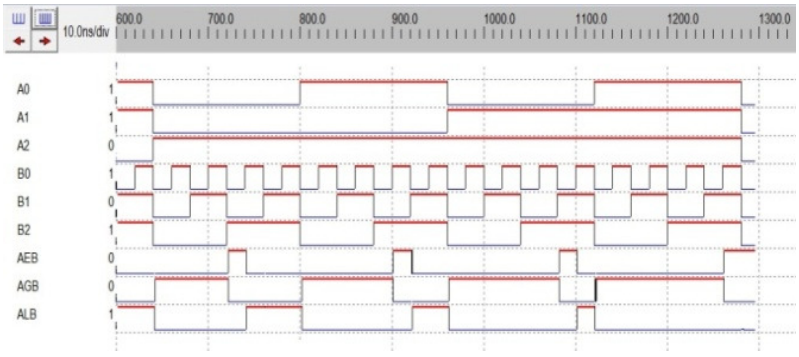


Figure 24. Simulation Result of Reversible 3-bit Comparator

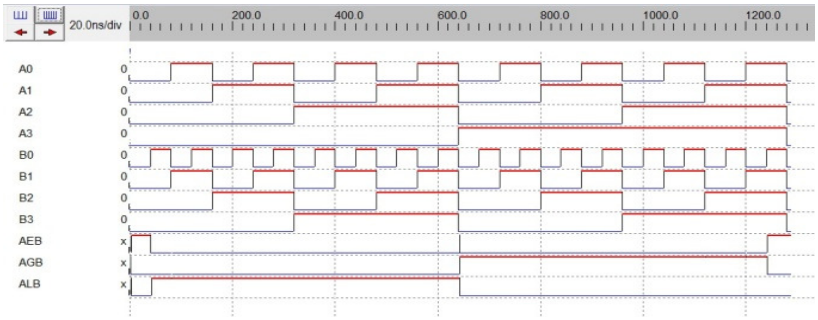


Figure 25. Simulation Result of Reversible 4-bit Comparator

Table 1 and 2 show the comparative study of the proposed design with the other existing researches. From the tables it can be seen that the proposed design performs better than those of the others. And certainly a minimum cost is required to design the 8-bit and 64-bit reversible comparator. GB and QC are the two performance criteria where this proposed work has shown significant improvement over all the other counterparts.

Table 1. Comparison of Reversible 8-bit Comparator

| | GA | GB | QC | CI |
|---|---|---|---|---|
| Proposed Circuit | 29 | 29 | 103 | 16 |
| Existing Circuit[26] | 29 | 36 | 124 | 23 |
| Existing Circuit[25] | 72 | 42 | 135 | 59 |
| Existing Circuit[24] | 40 | 64 | 321 | 27 |

Table 2. Comparison of Reversible 64-bit Comparator

| | GA | GB | QC | CI |
|---|---|---|---|---|
| Proposed Circuit | 253 | 253 | 887 | 128 |
| Existing Circuit[26] | 253 | 316 | 1076 | 191 |
| Existing Circuit[25] | 576 | 378 | 1143 | 451 |
| Existing Circuit[24] | 320 | 512 | 2505 | 195 |

## 6. CONCLUSIONS

This paper presents a systematic approach to design an *n*-bit signed comparator in reversible mode. With the help of comparisons and theorems it has been shown that the paper exhibits its efficiency over all the existing designs in terms of all the performance parameters. Quantum cost minimization is the strength of the proposed architecture. Since comparison of two numbers can be useful in many operations inside the microprocessor, communication systems, encryption devices, sorting networks [11] and many more, it can be expected that the optimized low cost design will surely bring more efficiency and scalability in the world of reversible computing. Currently, studies are being performed to extend this design in a form of tree based architecture to bring more features of reversibility.

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