

STATIC POWER OPTIMIZATION USING DUAL SUB-THRESHOLD SUPPLY VOLTAGES IN DIGITAL CMOS VLSI CIRCUITS

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Abstract

Power dissipation in high performance systems requires more expensive packaging. In this situation, low power VLSI design has assumed great importance as an active and rapidly developing field. As the density and operating speed of CMOS VLSI chip increases, static power dissipation becomes more significant. This is due to the leakage current when the transistor is off this is threshold voltage dependent. This can be observed in the combinational and sequential circuits. Static power reduction techniques are achieved by means of operating the transistor either in Cut-off or in Saturation region completely and avoiding the clock in unnecessary circuits. In this work, "Dual sub-threshold voltage supply" technique is used to operate the transistor under off state or either in on state by applying some voltage at the gate of the MOS transistor. This static power reduction technique is to digital circuits, so that the power dissipation is reduced and the performance of the circuit is increased. The designed circuits can be simulated by using Mentor Graphics Backend Tool.

Keywords

Dual sub-threshold, reliability, power dissipation, leakage current.

1. INTRODUCTION

Low power design is the upcoming design technology due to its high performance battery-portable digital systems. Presently there are many portable devices that run on batteries, laptop, tablet PC, mobile phone, ipod, etc. The power dissipation in these devices is high. This is due to the supply of high voltage to the low power components in the device. If the supply power is low then the circuits operating with that power should be capable of holding the loads. For example, if an amplifier circuit is working with low input power then the output should be capable of driving a loud speaker. The circuits which requires low power is better to use battery, so that the device will be portable. If the power is reduced then the circuits that require low power to be used and thus the number of circuit's increases but the power supply remains the same. As the circuits are operated in parallel the output of one circuit will depend on other circuit or may be

independent and the usage of clock circuit is mandatory. Therefore the complexity of circuits increases and the power (energy) supply remains same.

If the speed is increased then the circuits must be operated with high frequency clock pulse, at the same time, if some circuits needs low frequency thus there is a need of a frequency divider and some extra hardware is required to connect the circuits. Thus, the complexity is increased for the high speed devices. Thermal problems arise due to more hardware in a dense packing. For this there is a need for the cooling process. So, there is a need for heat sinks and cooling fans for heat exhaust. By the use of low power circuits, there is no need of heavy weighted devices like transformers. Due to these considerations the weight, size and cost are reduced. The dual sub-threshold supply voltage technique would help to operate where complex devices need to consume less power. Thereby, the complex circuits will dissipate less amount of power.

At the same time, due to the use of battery power there is no fluctuations in the supply power and the noise produced by the circuits is very low. The need for low power is to reduce the power dissipation, to increase the battery life time, reducing heat sinks, cooling fans and finally the cost of the device also reduces. In this work, the circuits are designed and simulated in mentor graphics back-end tool through Linux operating system. This provides the better way to design the circuits from physical design and the circuits can be simulated easily as in the real time. The remaining sections of the paper as follows: section 2 is about different low power design techniques, design principles, power dissipation are given in section 3 and 4, implementation of the circuits are given in section 5 and finally results and conclusion are discussed.

2. DIFFERENT LOW POWER DESIGN TECHNIQUES

There are certain low power techniques that provide low power dissipation by using the low power design techniques. Techniques used in low power design includes

2.1 Clock gating technique

In this technique, the circuit consumes more power when the clock is on and the clock pulse must be provided to every circuit which leads to complexity. The clock signal generator also consumes power every time when the supply is on. The disadvantage of this technique is increase of leakage power [1] [2] in the circuit when there is no input.

2.2 Multi-threshold CMOS (MTCMOS)

In multi threshold technique [3] different supply voltages are given to different circuit components depending on the circuit path length. If the path length is long then high threshold supply voltage must be given, if not low threshold supply voltage must be given so that low voltage drop takes place. In this technique, the disadvantage is different threshold supply voltages are provided in the circuit, this leads to the degradation of the compatibility.

2.3 Stacked Transistors

In this technique, more number of transistors can be incorporated on a single wafer. So the transistor stacking will allow them to increase circuit density. They appear to be building silicon wafers and stacking them together. Advantage of this technique is reducing IC size. Low power is sufficient to drive an IC due to reduced wire length and power dissipation can also be reduced. The disadvantage of the circuit is operated at high voltage, but the power dissipation due to resistance is reduced due to reduced wire length.

2.4 Dynamic Threshold MOS (DTMOS)

In this technique, the threshold supply voltage can be varied between some fixed range of voltage. As the circuit will be designed with a predefined technology and once if the IC is manufactured it cannot be modified internally for a designed technology. The disadvantage of this technique is that the components do not have certain limit of threshold supply voltage.

2.5 Dynamic/voltage/frequency scaling [4-7]

In this technique, the supply voltage can be reduced without change in the technology of the circuit that is designed and the frequency of the input can be scaled down these are dynamic changes done externally. The disadvantage in this technique is the supply voltage is technology dependent, if high voltage is given to the components then the component is damaged.

2.6 Near sub-threshold supply [4-7]

In this technique, the supply voltage is scaled down such that the devices are also scaled down. So the devices can be operated at sub-threshold voltage. The disadvantage in this technique is when the component is used just above the threshold voltage then there can be an electron migration in the transistors used in the circuit.

3. DESIGN PRINCIPLES

Transistors are designed in such a way that the width of the gate should be more when compared with the length of the channel this is made such that the for applied gate voltage the channel must be formed for logic high in NMOS and logic low in PMOS transistors. If the insulator used at the gate of the MOS transistor is of very less width than the channel length, hence if the transistor is off even though certain current flows due to charge induced due to capacitance effect. To reduce the leakage current the length and width of MOS transistor is made suitably for low voltage applications that to near sub-threshold voltages.

In this paper, by using multi threshold supply voltages that are provided with near sub-threshold voltage and the voltage can also be varied around below sub-threshold and near sub-threshold voltages. Transistors are designed to operate at weak inversion, so that sub threshold supply voltage is sufficient to operate these transistors with negligible leakage current. Static power consumed by these transistors is very less. The dynamic power consumed by the transistors depends on the switching frequency of the signal that is applied at the gate of the transistor, full supply voltage and the load capacitance used.

Supply voltage scaling was developed for switching power reduction. It is an efficient method for reducing switching power. It also helps to reduce leakage power because the sub-threshold leakage is due to Gate Induced Drain Leakage (GIDL) and Drain Induced Barrier Leakage (DIBL), these are also reduced as well as the gate leakage component when the supply voltage is scaled down. Static supply voltage scaling is a multiple supply voltage where as different supply voltages are provided. The speed of the non-critical paths are not deterministic where as the speed of the critical paths are lowered when compared with the non-critical paths. In order to satisfy the speed performance the critical and non-critical paths are made to operate with same speed without disturbing the system performance. By using multiple supply voltage technique the interconnect delays are made negligible depending upon the lengths of the interconnects.

4. POWER DISSIPATION

Static power is reduced by reducing the length of the channel and width of the gate of transistors [3], this is the easy way to reduce the static power consumption of a transistor without disturbing its operation. The low voltage operation is that the conduction is due to diffusion of charge carriers. Transistors connected to low threshold supply voltage conduct as the channel will be formed for very low voltage. So that, even for a high threshold supply voltage the power dissipation by the transistors is less. The near sub-threshold supply voltage is sufficient for the transistors to conduct. Static power essentially consists of the power used when the transistor is not in the process of switching.

$$P_{\text{static}} = I_{\text{static}} * V_{\text{dd}} \quad (1)$$

The near threshold supply voltage is also provided in order to make the transistors to conduct if there are equal paths that there are no critical and non-critical paths. Hence all the transistors need equal voltages. Thereby, the static power dissipation is reduced. Dynamic power is the sum of transient power consumption ($P_{\text{transient}}$) and capacitive load power (P_{cap}) consumption. $P_{\text{transient}}$ represents the amount of power consumed when the device changes logic states. Capacitive load power consumption is the power used to charge the load capacitance.

$$P_{\text{dynamic}} = P_{\text{cap}} + P_{\text{transient}} = (C_L + C) * V_{\text{dd}}^2 * f * N^3 \quad (2)$$

Where 'N' is the number of logic values that are switching, 'f' is the switching frequency. The short circuit power depends upon the frequency of the transition. Hence the total power dissipated is the sum of all the power dissipations in the circuit.

$$P_{\text{total}} = P_{\text{ststic}} + P_{\text{sc}} + P_{\text{dynamic}} \quad (3)$$

The power dissipation can also be further reduced by placing a transmission gate between the circuit and the power supply. The inputs are connected to the transmission gate also. Depending upon the inputs the transmission gate conducts that means there is some input to the circuit. When there is no input the transmission gate will be in off state. If the transistors are not designed as per our requirement the leakage power dissipation will be high as the leakage power is inversely proportional to the threshold voltage. A way to reduce leakage power consumption is to raise the V_{th} of some gates. A higher V_{th} reduces the sub-threshold leakage. Hence, the transistors are designed in order to reduce the power dissipation to maximum level. The use of two power supplies makes some devices to allow the leakage current hence by providing a third power supply that is greater than the threshold supply voltage. The delay increases as the supply voltage is scaled down. This technique can be applied to any circuit either combinational or sequential circuit.

5. IMPLEMENTATION

Any CMOS circuits can be designed by implementing the dual sub-threshold supply voltages along with V_{dd} . The designed combinational circuits are decoder, 4x1 multiplexer and sequential circuits are Moore and Mealey machine, ring counter. The logic gates are designed with CMOS transistors, the gates are designed as shown below. The inverter with V_{DD} as supply voltage is given in Figure 1.

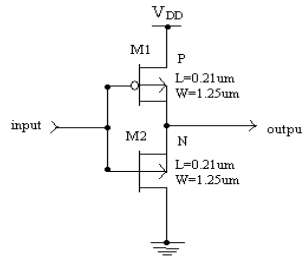


Figure 1. Inverter with V_{DD} as supply voltage

In this circuit the input is applied to both transistors depending on the applied input logic the transistors conduct and the output is obtained. The inverter circuit uses very less number of transistors connected through the supply voltage to the ground. Hence very low voltage is sufficient to operate the inverter with very less power dissipation. The power dissipation for different supply voltages is tabulated.

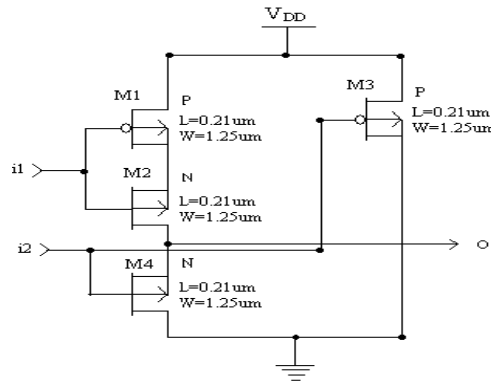


Figure 2. NAND gate with V_{DD} as supply voltage

The NAND gate with V_{DD} as supply voltage is given in Figure 2. The circuit inputs are i_1 and i_2 , depending on the input voltage applied transistors conduct and the output at O is obtained. The designed NAND gate uses supply voltage either V_{DD} or Low V_{th} or High V_{th} . Depending upon the voltage applied the NAND gate is operated with low leakage current and very low power dissipation.

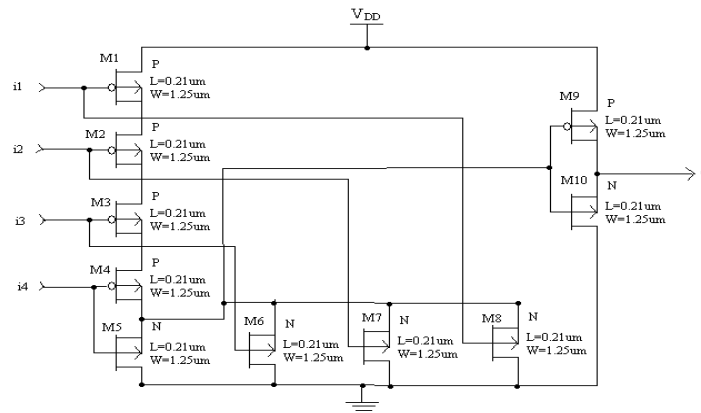


Figure 3. 4-input OR gate with V_{DD} as supply voltage

Figure 3 gives the functionality of 4-input OR gate with V_{DD} as supply voltage. In this circuit, the inputs are i_1 , i_2 , i_3 , i_4 and the output is O. The input is applied to the transistors as the input

voltage is very low the transistors conduct. Depending upon the number of transistors used in the circuit the supply voltage is also varied, if there are a number of transistors connected in series the supply voltage is to be increased in order to obtain the required output for the given input.

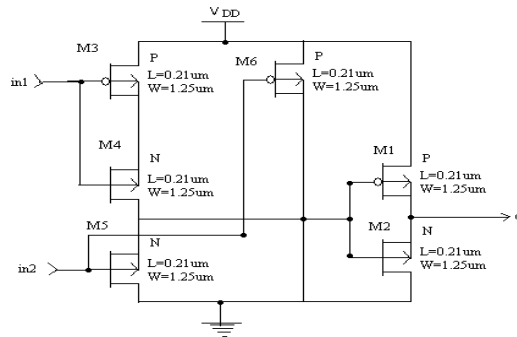


Figure 4. 2-input AND gate with Vdd as supply voltage.

The 2-input AND gate with V_{DD} as supply voltage is given in Figure 4. In this circuit the inputs are in1 and in2. The output is O. Depending upon the applied logic the transistors conduct and the output is obtained. The AND gate designed with an inverter and the NAND gate, hence inverter requires very low power supply, NAND gate uses some high voltage than the inverter. Hence High V_{th} supply voltage is sufficient to drive the AND gate.

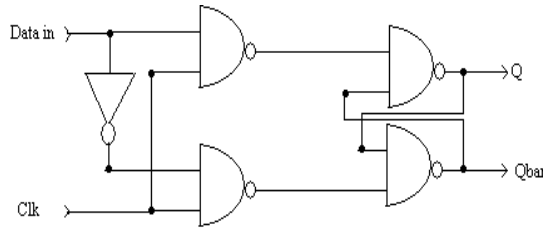
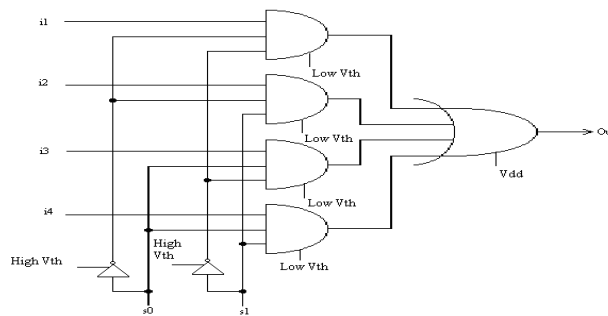


Figure 5. D-Flip Flop

The D-Flip flop is given in Figure 5. In this circuit, the inputs are Data in and Clk. The outputs are Q and Qbar. The NOT gate applied between the two NAND gates to provide the inverted operation for the given input so that output at Qbar is obtained. For the given input the required output at Q is obtained. The D-Flip flop requires (high threshold supply voltage) High V_{th} supply voltage, hence in order to dissipate low power the transistors are designed with required parameters such as channel length and gate width of the transistor. Further, the designed circuits are discussed below. The 4x1 Multiplexer with dual sub-threshold supply voltage is given in Figure 6.



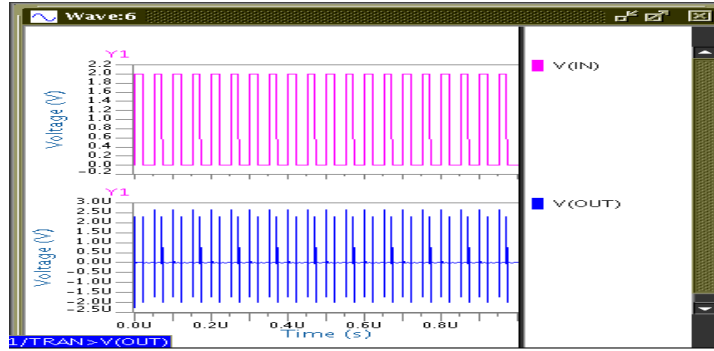


Figure 9. Simulation waveform of DCVS level converter for NOT gate

The 2×4 Decoder with dual sub-threshold supply voltage and its simulation waveforms are given in Figures 10 and 11 respectively.

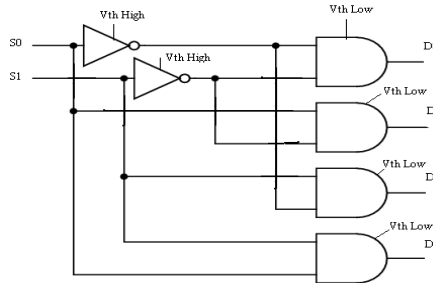


Figure 10. 2×4 Decoder with dual sub-threshold supply voltage

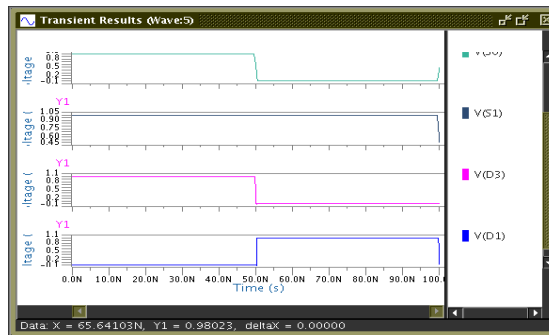


Figure 11. Simulation waveform of 2×4 Decoder with dual sub-threshold supply voltage

Later, the same technique was applied for sequential circuits and its functionality was verified. The Mealey and Moore machine with dual sub-threshold supply voltage are shown in Figures 12 and 13. The simulation waveforms of the designed circuits are given in Figure 14 and 15 respectively. In this circuit, inputs are A, D1 and Clk. Outputs are D2 and Z. Depending on the inputs applied to the AND gate the D-flip flop output is obtained, this is connected to the NOR gate the output Z is obtained. Similarly the output is at D2. The mealey machine is designed with D-Flip flops, AND, OR, NOR gates depending upon the path lengths connected in the circuit the supply voltage to the different blocks in the circuit is also varied. In this inputs are Vin and Clk. Output is Y. Depending on the inputs applied to the D-flip flops through the logic gates output is obtained, this is connected to the OR gate and the output Y is obtained.

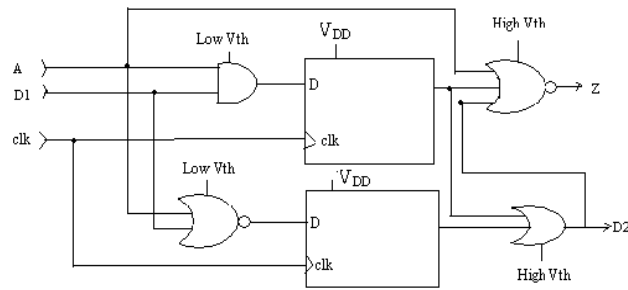


Figure 12. Mealy Machine with dual sub-threshold supply voltage

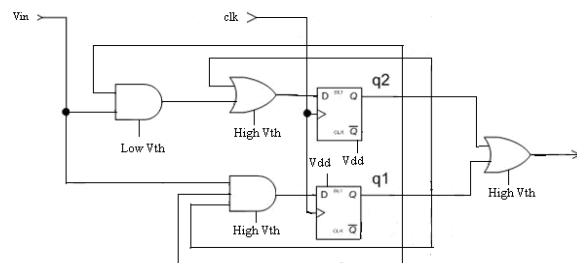


Figure 13. Moore Machine with dual sub-threshold supply voltage

The Moore machine is designed with D-flip flop, OR, AND gates depending upon the path lengths the power is supplied in order not to waste the supply power in the form of power dissipated as heat. Longest paths require high threshold supply, shortest paths require low threshold supply voltage, and circuit blocks with more number of transistors require Vdd as supply voltage that is greater than the high threshold supply voltage.

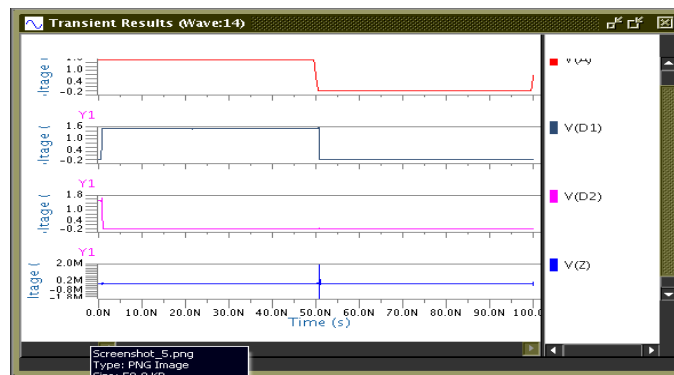


Figure 14. Simulation waveform of Mealy Machine with dual sub-threshold supply voltage

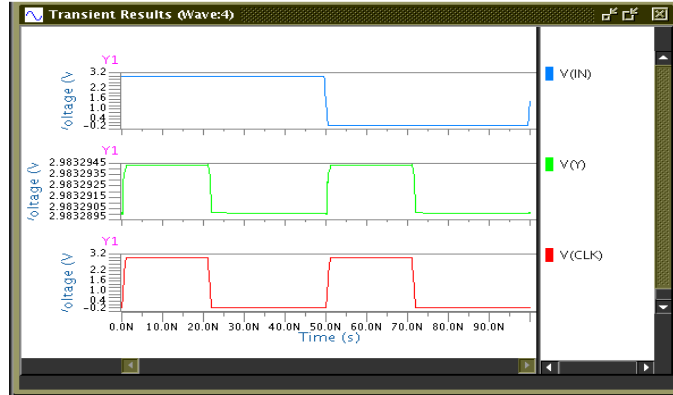


Figure 15. Simulation waveform of Moore Machine with dual sub-threshold supply voltage

The ring counter with dual sub-threshold supply voltage is given in Figure 16. In this inputs are reset and Clk. Outputs are R0, R1, R2, R3 and R4. Depending on the inputs applied to the D-flip flops output R1, R2, R3, R4 are obtained this is due to the delay by each flip-flop, this is connected to the NOR gate and the output R0 is obtained. The output can be clearly obtained for clock pulse with less with. Ring counter uses only two power supplies that are high threshold supply voltage and V_{dd} supply, for 4-input NOR gate as there are more number of transistors required hence V_{dd} supply is provided. D-flip flop uses few gates than the NOR gate in this circuit so high threshold supply voltage is provided. This dual supply voltage also provides an advantage depending upon the path length in the circuit.

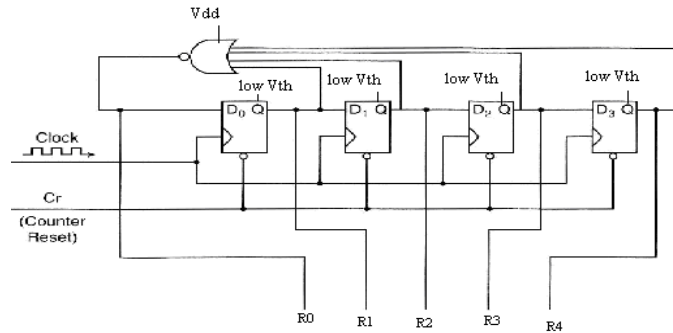


Figure 16. Ring Counter with dual sub-threshold supply voltage

Some circuit designs allow only low threshold, some other high threshold, some circuits uses both low and high threshold supply voltages. Power consumption is different in different circuits, as it depends upon the supply voltage, load applied, type of components used to design the circuit, the technique and technology used to design the circuit. The $1.25\mu\text{m}$ technology is used to implement these designed circuits. The power dissipation of circuits with sub-threshold supply voltages along with V_{dd} is given in Table 1. The results of power dissipation of circuits with dual sub-threshold supply voltages are given in Table 2.

Table 1. Power dissipation of circuits with sub-threshold supply voltages along with V_{dd}

Designed circuit	Supply voltages(volts)			Power dissipation (watts)
	Vdd	V _{dd} high	V _{dd} low	
DCVS for NOT gate	0.7	0.35	0.15	2.279 μ
Nand	-----	-----	0.15	39.9354n
Inverter	-----	-----	0.15	25.9438f
2 to 4 Decoder	0.7	0.35	0.15	1.7851 μ
Moore	0.7	0.25	0.15	18.6552 μ
Ring counter	1.5	-----	0.15	690.1097n
Up-down counter	0.7	0.25	0.15v	4.6425 μ

Table 2. Power dissipation of circuits with dual sub-threshold supply voltages

Designed circuit	Supply voltages(volts)		Power dissipation (watts)
	V _{dd} low	V _{dd} high	
DCVS for NOT gate	0.24	0.15	6.385 μ
Inverter	0.24	0.15	34.680n
Nand	0.24	0.15	244.0433n
2 to 4Decoder	0.24	0.15	5.417 μ
Up-down counter	0.24	0.15	35.9634u

6. POWER DISSIPATION COMPARISON

The power dissipation by using the dual sub-threshold supply voltage is more this is because of the more leakage power and the output results are not accurate, when compared with the power dissipation using the dual sub-threshold supply voltage along with V_{dd} and the output is accurate. The Table 3 describes the percentage of power dissipation between dual sub-threshold supply voltage along with Vdd and dual sub-threshold supply voltage.

Table 3. Percentage reduction of power dissipation for dual sub-threshold supply voltage with and without supply voltage

S.No.	Designed circuits	Power dissipation (watts)		Power reduction (%)
		without V _{DD}	withV _{DD}	
1	DCVS	6.385 μ	2.279 μ	73.69
2.	Decoder	5.417 μ	1.7851 μ	75.21
3.	Nand	244.0433n	39.9354n	85.93
4.	Up-Down counter	35.9634 μ	4.6425 μ	88.56

7. CONCLUSION

The power dissipation by using dual sub-threshold supply voltage along with V_{DD} is less when compared to the dual sub-threshold supply voltage without V_{DD} . The power dissipation increases while increasing the V_{DD} supply voltage. The leakage power dissipation is high for very low supply voltages due to the leakage current through the ground. This technique can be applied for any CMOS digital circuits depending on number of components used. High supply voltages can not be applied for these designed circuits. Hence this technique provides a better solution for the low power devices.

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