

# DESIGN OF LOW POWER CMOS LOGIC CIRCUITS USING GATE DIFFUSION INPUT (GDI) TECHNIQUE

Y. Syamala, K. Srilakshmi and N. Somasekhar Varma

Department of Electronics and Communication Engineering, Gudlavalleru Engineering College, Gudlavalleru, A.P. India

## ABSTRACT

*The Gate diffusion input (GDI) is a novel technique for low power digital circuit design. This technique reduces the power dissipation, propagation delay, area of digital circuits and it maintains low complexity of logic design. In this paper, the 4×1 Multiplexer, 8×3 Encoder, BCD Counter and Mealy State Machine were implemented by using Pass Transistors (PT), Transmission Gate (TG) and Gate Diffusion Input (GDI) technique and then they were compared with each other for power dissipation. The Multiplexers and Encoders are combinational circuits and Counters and mealy machines are sequential circuits both of them are very important digital systems so power optimization should be done to those digital circuits. The whole processes for development of digital circuits and simulation was done by using the mentor graphics backend tool. This method can also be extended to the processors and other high level designs for optimization of power dissipation, area and delay in order to increase the circuit efficiency.*

## KEYWORDS

*Pass Transistors, Transmission Gate, Gate Diffusion Input, Digital Circuits, Power Dissipation.*

## 1. INTRODUCTION

Power management has become a major issue in the development of a digital system especially, in the portable devices in which enhancement of the battery life time and reducing the charging time are becoming a challenging issues day by day. The major problem in the power management is power dissipation. Technology scaling leads to increase leakage current, which leads to increase in sub threshold leakage power. Therefore, reduction of the leakage power nothing but minimizing power dissipation. There are different techniques existed in literature [1] [2] among them, Gate Diffusion Input (GDI) technique is one to minimize the power dissipation.

In this paper, some of the digital circuits such as 4×1 Multiplexer, 8×3 Encoder, BCD Counter and Mealy Machine were designed by using Pass Transistors (PT), Transmission Gate (TG) and Gate Diffusion Input (GDI) techniques. The designed circuits are functionally verified, and the analysis of power dissipation is performed. The remaining sections of the paper as follows: section 2 is about implementation styles, the implementation of digital circuits using Gate Diffusion Input is given in section 3, results and conclusion are given in section 4 and 5 respectively.

## 2. DIFFERENT IMPLEMENTATION TECHNIQUES

Pass Transistors, Transmission Gates and Gate Diffusion Input are different techniques in design of low power digital circuits. Pass transistor design have small nodal capacitance which results in high speed. The amount of transistors used here were very low so that there is low power dissipation. Reduced number of transistors occupies small area which leads to minimize the interconnection of the wires [1]. There are two main disadvantages with pass transistor design; one is the threshold voltage across the single channel Pass Transistor, which results in reduced drive and slow operation. Other one was, full swing voltage at output is not possible. Another technique was, Transmission gate used to realize complex logic functions. The degradation voltage level at output problem can be overcome by using this technique. Where as, this technique requires more area than pass circuitry and requires complemented control signals. To realize any logic function, the basic AND and OR are used in any design of digital circuits. So, first these logic gates were developed by using Pass Transistor, Transmission Gate and Gate Diffusion Input techniques. The AND logic using Pass Transistors is shown in Figure 1.

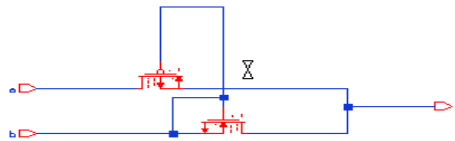


Figure 1. AND Logic using Pass Transistors

To realize the functionality of AND logic using Pass Transistors which requires two transistors such as P-type and N-type. When the logic '1' is applied to the gate inputs of the transistors, then PMOS will turn off and NMOS will turn on. At the same time, if logic '1' is given to the input 'b' then the output will be '1'. If logic '0' is given to the input 'b' then the output will be zero through on transistor. If logic '0' is given to the input a then PMOS turns on by applying gate input as logic 0 then that zero goes to the gate of NMOS and drain of PMOS then whatever logic comes from b multiplies with logic '0' and finally the result will be zero. So, here the two inputs 'a' and 'b' are logic '1' then the output will be '1'. If any of inputs are '0' output will be zero which is nothing but AND logic. The OR logic using Pass Transistors is shown in Figure 2.

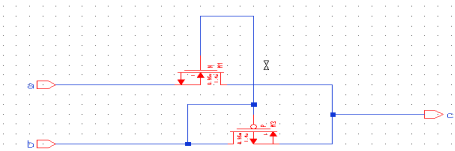


Figure 2. OR Logic using Pass Transistors

When the logic '0' is applied to the gate inputs then NMOS will turn off and PMOS will turn on. At this instant, what ever the inputs are applied at terminals 'a' and 'b', then the output will be produced at 'c' through on transistor. If logic '0' is given to the input 'a' then NMOS turns on by controlling gate input as logic 1, then that zero goes to the gate of PMOS and drain of NMOS then what ever logic comes from 'b' multiplies with logic '1' and finally the result will be '1'. So, here the two inputs are logic '0' then output as '0'. If any of inputs are '1' then output as '1' which is nothing but OR Logic. The AND logic can also be implemented by using Transmission Gate and it was shown in Figure 3.

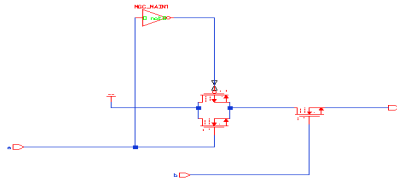


Figure 3. AND Logic using Transmission Gate

AND logic using transmission gate uses two NMOS and one PMOS transistors. In addition to that of inverter, the control signals are also used. The control signals avoid signal degradation. when logic '0' is applied to the input 'a' then through NMOS device turns off and PMOS device turns on and the logic '0' is passed as logic '1' to another NMOS. The gate of the second NMOS device will take the another input through 'b' if that is one then the output will be '1' or logic is zero then the output will be zero irrespective of the input from 'a', which is AND operation. The implementation of OR logic using the Transmission Gate was shown in Figure 4.

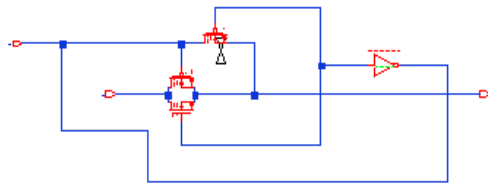


Figure 4. OR Logic using Transmission Gate

The next technique is Gate Diffusion Input Technique here one of the inputs are directly diffused into the gates of the transistors of N-type and P-type devices so it is called as gate diffused input technique. Gate Diffusion Input technique reduces power dissipation, propagation delay, and area of digital circuits [3-7]. This method is based on the simple cell. A basic GDI cell contains four terminals they are G (common gate input of NMOS and PMOS transistors), P (the outer diffusion node of PMOS transistor), N (the outer diffusion node of NMOS transistor), and D (common diffusion node of both transistors). The basic GDI cell, and implementation of AND, OR logics are given in Figures 5, 6 and 7 respectively.

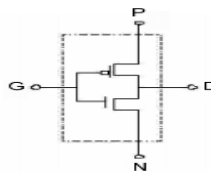


Figure 5. Basic GDI cell

Table 1. Logic function implemented with GDI cell

N	P	G	D	Function
0	B	A	$A*B$	F1
B	1	A	$A+B$	F2
1	B	A	$A+B$	OR
B	0	A	$AB$	AND
C	B	A	$AB+AC$	MUX
0	1	A	A	NOT

Any logic functions can be implemented using GDI Technique. The Table 1 gives us the information about the logic functions which are implemented by using Gate Diffusion Input. The operation of GDI based AND gate can be explained with respect to basic GDI cell 'P' of the transistor is given '0' it will cut-off from its operation, hence the logic either '1' or '0' at the input 'a' will be reflected at the output 'z'. Thus the output will be  $z = a*b$ .

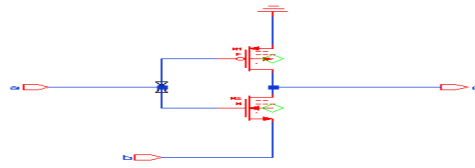


Figure 6. AND Logic using GDI

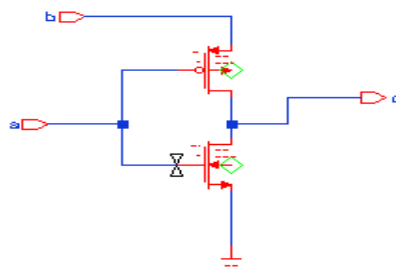


Figure 7. OR Logic using GDI

By using this technique the various digital circuits can be designed with low transistor count as compared with other CMOS designs which results in low power dissipation.

### 3. IMPLEMENTATION OF GDI DIGITAL CIRCUITS

In this paper, the main aim of this work was to minimize the power dissipation using GDI technique. Therefore, the 4×1 Multiplexer, 8×3 Encoder, BCD Counter and Mealy Machine were implemented with the Pass Transistor, Transmission Gate and Gate Diffusion Input. Among those, circuits which are implemented using GDI technique are discussed in this section. These circuits are simulated and the power dissipation values are tabulated for supply voltage of 1volt. The design of 4×1 Multiplexer using GDI Technique was given in Figure 8.

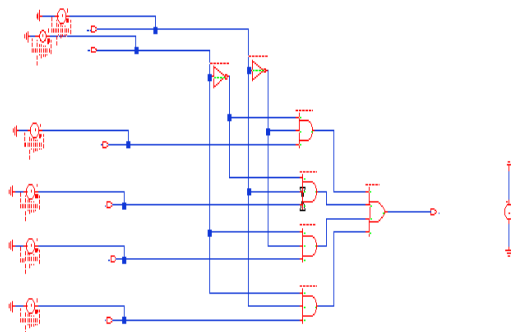


Figure 8. 4×1 Multiplexer using Gate Diffusion Input

Multiplexers are used as a data selector. A Multiplexer is a device that selects one of several input signals and forwards the selected input into a single output line. A multiplexer has  $n$  select lines of  $2^n$  inputs. They are used to select the input line to send the output with the help of selection lines. Encoder is another digital combinational circuit whose function is quite opposite to that of decoder. It is having  $2^n$  inputs and  $n$  number of outputs here  $8 \times 3$  encoder is developed by using PT, TG and GDI Logic. This encoder is used to convert data from octal to binary data. The developed circuit is checked for their power dissipation and their values are tabulated. The development of  $8 \times 3$  Encoder using GDI was shown in Figure 9.

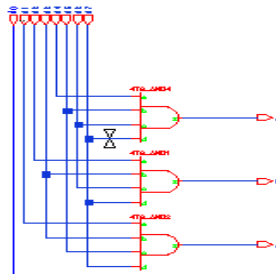


Figure 9.  $8 \times 3$  Encoder using Gate Diffusion Input

A counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal the counter is sequential circuit to which optimisation of power dissipation is very essential. The power reduction is done by developing this circuit with Pass Transistors, Transmission Gate and Gate Diffusion Input Techniques. The BCD counter using GDI was given in Figure 10.

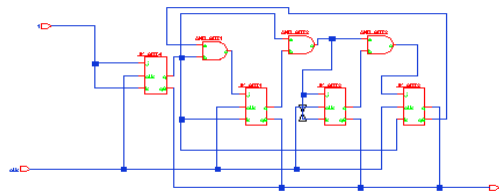


Figure 10. BCD Counter using Gate Diffusion Input

Mealy machine is one of the finite state machine which is used to depend upon the states and inputs. The main advantage with this state machine is used to reduce the number of states. The mealy machines are developed by using Pass Transistors, Transmission Gates and Gate Diffusion Input. The power dissipation of the Mealy Machine are compared and tabulated. The Mealy machine was shown in Figure 11.

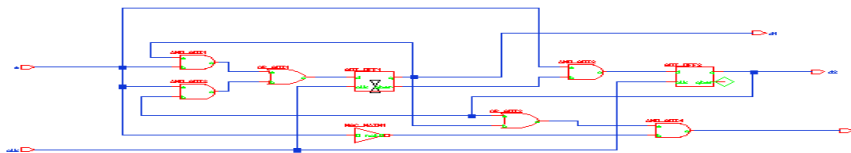


Figure 11. Mealy Machine using Gate Diffusion Input

#### 4. RESULTS

The power dissipation values are analysed for different supply voltages of the designed circuits and they were compared with each other. Finally, it was observed that, the designed digital circuits dissipate less amount of power using GDI technique.

Table 2. Power dissipation of 4x1 Multiplexer

S.No	Techniques used	Power Dissipation ( $\mu$ W)
1	Pass Transistors	5.6909
2	Transmission Gate	18.8684
3	Gate Diffusion Input	2.77400

Table 3. Power dissipation of 8x3 Encoder

S.No	Techniques used	Power Dissipation (pW)
1	Pass Transistors	4.5084
2	Transmission Gate	22.4860
3	Gate Diffusion Input	1.2569

Table 4. Power dissipation of BCD Counter

S.No	Techniques used	PowerDissipation ( $\mu$ W)
1	Pass Transistors	15.1506
2	Transmission Gate	36.221
3	Gate Diffusion Input	11.8373

Table 5. Power dissipation of Mealy Machine's

S.No	Techniques used	Power Dissipation
1	Pass Transistors	10.1605 $\mu$ W
2	Transmission Gate	15.0023 $\mu$ W
3	Gate Diffusion Input	185.7001 PW

The whole process was carried out by using mentor graphics back end tools. Out of the three techniques which were mentioned in the above tables GDI Technique dissipated less amount of power. So, the GDI is an efficient technique when compared with other techniques.

#### 5. CONCLUSION

The digital circuits 4x1 Multiplexer, 8x3 Encoder, BCD Counters and Mealy Machine were developed by using Pass Transistors, Transmission Gates and Gate Diffusion Input techniques and then their power dissipations are compared and they are simulated by using the Mentor

International Journal of VLSI design & Communication Systems (VLSICS) Vol.4, No.5, October 2013  
graphics backend tools. The power dissipation values of designed digital circuits with different techniques are observed. It was found that, the circuits using GDI has less amount of power dissipation as compared to pass transistor and transmission gate. Similarly, this technique can also be extended to complex circuits for their minimum power dissipation.

## REFERENCES

- [1] Kaushik Roy and Sharat C Prasad, "Low power CMOS VLSI circuit design", Wiley India Publication, 2011.
- [2] Janaki Rani, S.Malarkkan "Leakage power optimized sequential circuits for use in nanoscale VLSI systems " Indian Journal of Computer Science and Engineering (IJCSE) Vol. 3 No. 1 Feb -Mar 2012.
- [3] Arkadiy Morgenshtein, Alexander Fish, and Israel A. Wagner, "Gate Diffusion Input (GDI): A power efficient method for combinational circuits" , IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 10, NO. 5, October 2002.
- [4] Adarsh Kumar Agrawal, S. Wairya, R.K. Nagaria and S. Tiwari, "A new mixed gate diffusion input full adder topology for high speed low power digital circuits", World Applied Science Journal 7, pp.138-144, 2009, ISSN1818.4952.
- [5] A. Morgenshtein, A. Fish, and I. A. Wagner, "Gate-Diffusion Input (GDI) - A technique for low power design of digital circuits: analysis and characterization," in Proc. Int. Symp. Circuits and Systems, ISCAS, pp. 477-480, Oct. 2002.
- [6] T. Kalavathidevi and C. Venkatesh, "Gate Diffusion Input (GDI) circuits Based low power VLSI architecture for a viterbi decoder", Iranian Journal of Electrical And Computer Engineering, pp- 77-84, Vol. 10, No. 2, Summer-Fall 2011.
- [7] Arkadiy Morgenshtein, Idan Shwartz and Alexander Fish, "Gate Diffusion Input (GDI) logic in standard CMOS nanoscale process", 2010 IEEE 26th Convention of Electrical and Electronics Engineers in Israel.

## Authors

**Syamala** born on Sept 14<sup>th</sup> 1980 in kavali, India. Obtained B.E degree from Bharatiyar University, India in 2001. M.E degree in Applied Electronics from Anna University in 2005. In 2005 she joined as an Assistant Professor in Gudlavalluru Engineering College. In 2011, she promoted as an Associate Professor in department of ECE, GEC, India. She has been a member of IEEE, FIETE, and MISTE. She has published several papers in the area of VLSI. Her research interest includes Low power VLSI design, Digital design and Testing.



**Srilakshmi** born at Karnataka. She completed her B.Tech degree from JNTUK, Kakinada, India in 2009, and M.Tech in 2011 from the JNTUK University in VLSI System Design as specialization. She is currently working as a Assistant Professor in Department of ECE in Gudlavalluru Engineering College, India. Her research interest includes Low power design, VLSI design, Embedded design. She has been published several papers in different various conferences.



**Somasekhar Varma.N** born in Bapatla India He has obtained his B Tech degree in Electronics and Communication from Bapatla Engineering College Bapatla in 2010. Presently he is Pursuing his Masters degree in Embedded Systems of Electronics and Communication in Gudlavalluru Engineering College Gudlavalluru from 2011 to 2013. He is interested in Low power VLSI design. He is currently working on a project titled "Design of Low Power CMOS Logic Circuits using Gate Diffusion Input (GDI) Technique" as a partial fulfilment of his M.Tech degree.

