

DESIGN OF ULTRA LOW POWER 8-CHANNEL ANALOG MULTIPLEXER USING DYNAMIC THRESHOLD FOR BIOSIGNALS

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ABSTRACT

The design of an ultra low voltage, low power high speed 8 channel Analog multiplexer in 180nm CMOS technology is presented. A modified transmission gate using a dynamic threshold voltage MOSFET (DTMOS) is employed in the design. The design is optimized with respect to critical requirements like short switching time, low power dissipation, good linearity and high dynamic range with an operating voltage of 0.4V. The ON and OFF resistances achieved are 32 ohms and 10Mohms respectively with a switching speed of 10MHz. The power dissipation obtained is around 2.65uW for a dynamic range of 1uV to 0.4V.

KEYWORDS

Analog multiplexer, low power, high speed, body-bias.

1. INTRODUCTION

Advances in CMOS technology have led to a renewed interest in the design of basic functional units for digital systems. The use of integrated circuits in high performance computing, telecommunications, and consumer electronics has been growing at a very fast pace. This trend is expected to continue, with very important implications for power-efficient VLSI system designs. Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift where power dissipation has become as important consideration as performance and area.

The increasing demands on portable devices have motivated the development of CMOS Analog Multiplexer Integrated circuits. These portable devices require low power dissipation to maximize battery lifetime. Some low power applications, such a multichannel recorders, require the portable devices to operate at a low supply voltage with a small battery or environment energy, so the power and supply voltage constriction is a key issue for these designs [1]. However, due to standby power consideration, the threshold voltage of a metal oxide semiconductor field effect transistor (MOSFET), which doesn't scale down with supply voltage of future standard CMOS technologies , makes a limitation for the CMOS low voltage designs.

An analog multiplexer is a key part in bio-medical applications MEAs (multi electrode arrays) are widely used for recording signals from human body. For analog multiplexer design, low voltage applications make the trade-off between switching frequency, signal losses and power consumption very challenging. Many efforts [2], have been made to develop low power Analog Multiplexer, but little research has been reported for Ultra Low voltage applications. In this work a 0.4 V fully integrated Analog Multiplexer is presented, meeting the requirement of both Ultra Low power applications and Ultra Low voltage applications. By using a modified transmission gate and forward body bias technology, the supply voltage is successfully reduced to 0.4 V. At such a low supply voltage, a good trade-off is made between power and other performances.

High-density arrays comprising tens of electrodes driven for the development of multi-channel integrated circuits for selective recording of signals from the human body [3]. One of the important building block of such integrated circuits are analog multiplexers. A multiplexer is required to reduce the number of output data links as for a system comprising several tens of recording channels. It is not feasible technically and it would be expensive to transfer signals from each individual electrode to a data acquisition system via a separate cable.

In a typical measurement sequence the signals from all the channels are read out at very high speed to avoid any loss of signals through a multiplexer and routed to single output. The multiplexer in our design essentially built into a decoder and switches. Analog systems carry the signals in the form of physical variables such as voltage, currents which are continuing functions of time. The manipulation of these variables must often be carried out with high accuracy. Analog circuits continue to be used for direct signal processing in some very high frequency or specialized applications. The development of VLSI technology has led to computers being pervasive in telecommunications, bio-medicine, robotics etc. since analog circuits are needed together with digital once in almost any complex chip most of the current analog circuits are CMOS circuits. CMOS switches have an excellent combination of attributes. In its most basic form, the MOSFET transistor is a voltage-controlled resistor. In the "on" state, its resistance can be less than 100 Ω , while in the "off" state, the resistance increases to several hundreds of mega ohms, with Pico-ampere leakage currents. CMOS technology is compatible with logic circuitry and can be densely packed in an IC [4]. Its fast switching characteristics are well controlled with minimum circuit parasitic. MOSFET transistors are bilateral, that is they can switch positive and negative voltages and conduct positive and negative currents with equal ease.

A transmission gate is used as an analog switch, it is defined as an electronic element that will selectively block or pass a signal level from the input to the output. This analog switch is comprised of a PMOS transistor and NMOS transistor shown in fig:1

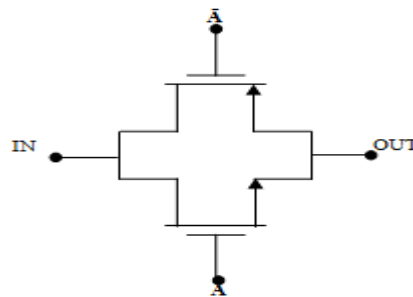


Fig:1. Transmission gate

The control gates are biased in a complementary manner so that both transistors are either ON or OFF. When a signal is passed through this transmission gate there will drop in amplitude of the signal at the output. To overcome this problem and getting the original signal without any loss the transmission gate is modified as shown in Fig-2.

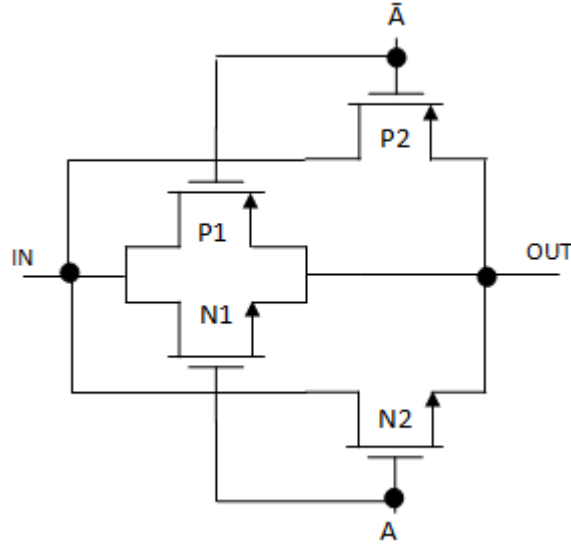


Fig: 2(a). Modified Transmission gate

2. BODY BIASING

Body effect refers to the change in the transistor threshold voltage (V_T) resulting from a voltage difference between the transistor source and body. Because the voltage difference between the source and body affects the V_T , the body can be thought of as a second gate that helps determine how the transistor turns on and off. The strength of the body effect is usually quantified by the body coefficient γ (gamma). The threshold voltage of MOSFET is well known as,

$$V_{Th} = V_{Th0} + \gamma \frac{\sqrt{2\phi_F} + V_{SB}}{\sqrt{2\phi_F}} - (\sqrt{2\phi_F})$$

where V_{Th0} is the threshold voltage when $V_{SB} = 0$, γ is the body-effect coefficient, ϕ_F is the bulk Fermi-potential, V_{SB} is the voltage between source and body. Thus, changing V_{SB} can modify V_{Th} , which can achieve a dynamic threshold voltage MOSFET (DTMOS). Usually, the junction between source and body is zero-biased or reverse-biased. To further improve performance with lower V_{Th} , forward-body-biased MOSFETs are also used in some circuits [5], [6]. Here, we introduce this concept into low power Analog Multiplexer design. A 0.4 V forward body bias is used to make the transistors in strong inversion region. The MOSFETs with W/L of $30\mu\text{m}/0.18\mu\text{m}$ for P1, P2 and $15\mu\text{m}/0.18\mu\text{m}$ for N1, N2 are used in the Modified transmission gate is shown in Fig-2(b).

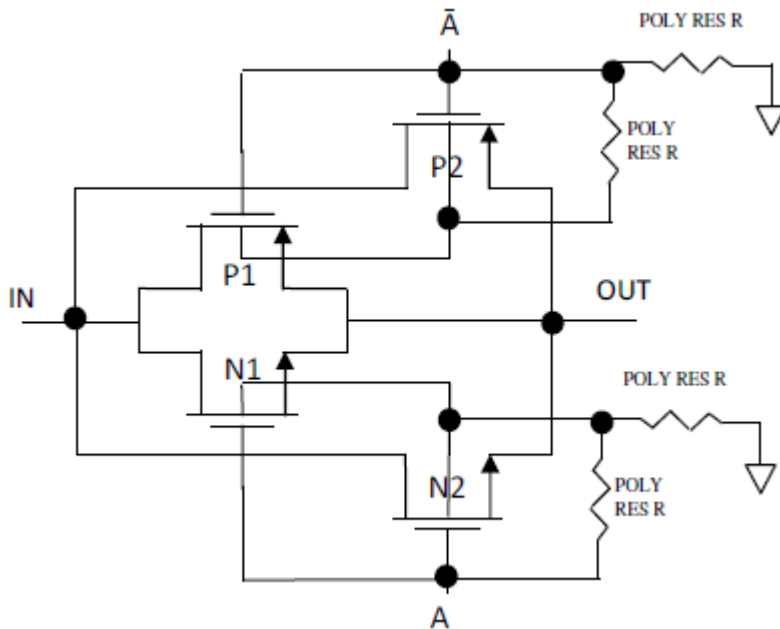


Fig: 2(b). Modified Transmission gate with Dynamic Body Bias.

Strong body effect enables a variety of effective body biasing techniques, and these techniques were used effectively in older process generations. The body bias can be supplied from an external (off-chip) source or an internal (on-chip) source. In the on-chip approach, the design usually includes a voltage divider to generate a forward body bias voltage. The poly resistors are used voltage divider network is Reverse body bias, which involves applying a negative body-to-source voltage to an n-channel transistor, raises the threshold voltage and thereby makes the transistor both slower and less leaky. Forward body bias, on the other hand, lowers the threshold voltage by applying a positive body-to-source voltage to an n-channel transistor and thereby makes the transistor both faster and leakier. The polarities of the applied bias described above are the opposite for a p-channel transistor.

3. MULTIPLEXER DESIGN

Several designs of multiplexers developed in the past are based on the concept of a shift register with walking one described in. The shift register is built as a chain of serially connected D-latches triggered synchronously with the external clock. Each latch activates readout of one S&H cell. A drawback of this circuit is the clock feed-through to the output line. The glitches occur synchronously with every positive and negative clock edge. This problem is minimized in proposed multiplexer design.

Dynamic body bias, on the other hand, changes the body bias multiple times while the chip is operating rather than setting the body bias just once either during design or at production test. Consequently, dynamic body bias can be used to reduce temperature and aging effects as well as to make power management modes more effective at optimizing very low power operation[7], [8].

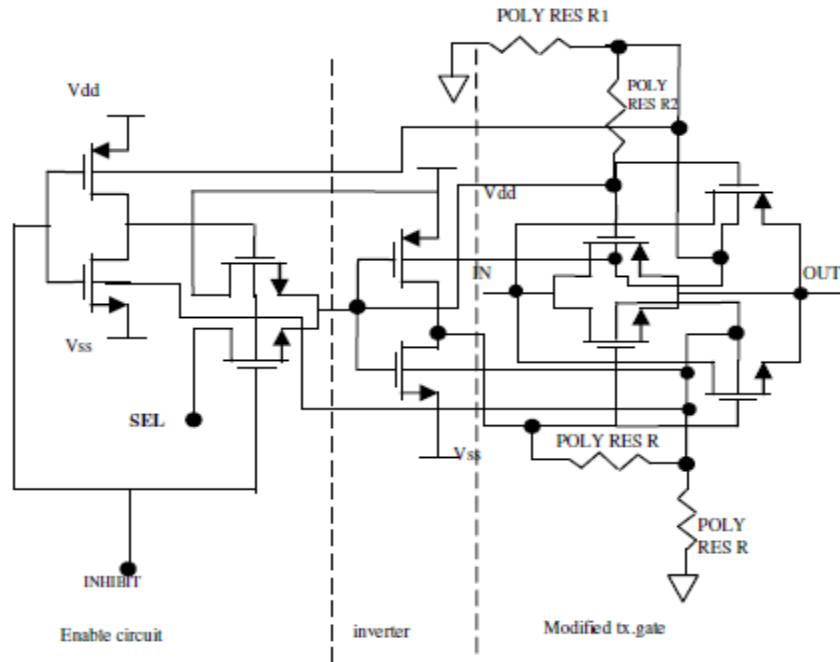


Fig: 3 DT MOS Single Channel Circuit

When the select signal (SEL) is a Logic 0, the complementary Logic 1 is applied to NMOS transistors to turn ON and pass the signal from IN to OUT. When the select signal (SEL) is a Logic 1, all transistors are turned OFF blocking the input signal. During the transition period from ON to OFF the output will be forced into a high-impedance state where the junction capacitance will be charged to few millivolts.

To overcome this drawback a PMOS transistor is used as a pass transistor between the ground and the output node. Whenever all the transistors are in OFF state then the PMOS transistor will be turned ON, forcing the output capacitor to discharge to ground.

An eight-channel loss less multiplexer has been designed using the modified circuit shown in Fig-3 for each channel. Three binary control inputs are used for selecting the channels. The inhibit input is used to turn the entire multiplexer ON or OFF.

The analog switches used had low leakage current in the order of Pico amperes, low ON resistance (32 ohms), high OFF resistance (10Mohms), low feed through capacitance in the order of fF were obtained. The select signals for each channel are generated from three binary control inputs using a 3 to 8 decoder circuit is shown in figure-4(a) and (b). The widths of the transistors are maintained in a ratio of 1:2 for NMOS to PMOS. The ON resistance R_{on} of the switch is

$$R_{on} = \frac{1}{g_{ds}} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_{Th})}$$

The value of the ON-resistance depends on the overdrive voltage, $V_{ov} = V_{gs} - V_{th}$ and on the aspect ratio, W/L through the transconductance parameter μC_{ox} . The ON resistance obtained is 32 ohms. The OFF resistance is 10Mohms

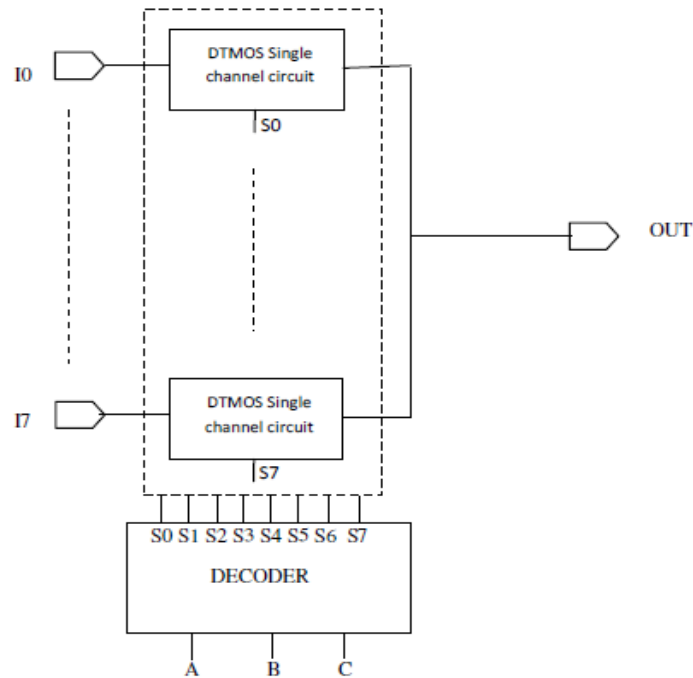


Fig: 4(a). block diagram of 8:1 mux with Decoder

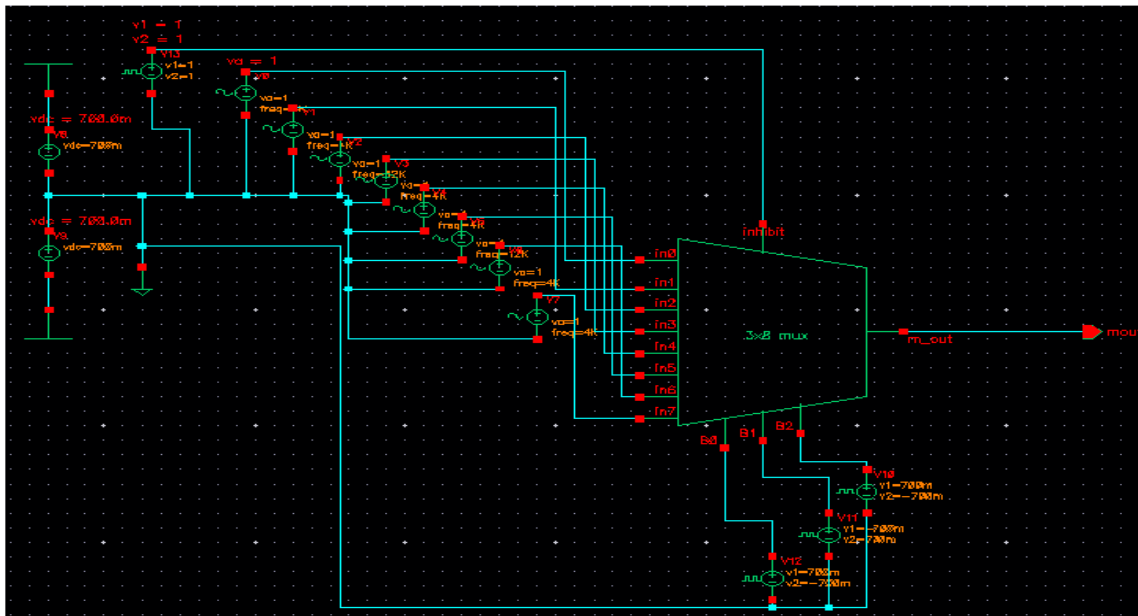


Fig:4(b). Schematic diagram of 8:1 multiplexer

The energy dissipation in the PMOS and NMOS devices can be written as the output switches from low to high

$$\text{For PMOS device} \quad E_P = \frac{1}{2} C_L V_{dd}^2$$

$$\text{For NMOS device} \quad E_N = \frac{1}{2} C_L V_{dd}^2$$

$$\text{The total power dissipation is written as} \quad E_T = E_P + E_N$$

$$= \frac{1}{2} C_L V_{dd}^2 + \frac{1}{2} C_L V_{dd}^2$$

$$\text{So the total power dissipation is } E_T = \frac{1}{2} C_L V_{dd}^2$$

4. RESULTS

The circuit is simulated by applying sinusoidal signals with an amplitude ranging from 1uV to maximum of 0.4V to each channel. The channels are selected by changing the input control signals of the decoder and the desired input is selected as shown in table-1

Table-1

INHIBIT	INPUTS	C	B	A	OUTPUT
L	X	X	X	X	L
H	I0	L	L	L	I0
H	I1	L	L	H	I1
H	I2	L	H	L	I2
H	I3	L	H	H	I3
H	I4	H	L	L	I4
H	I5	H	L	H	I5
H	I6	H	H	L	I6
H	I7	H	H	H	I7

The channel selection frequency is varied from DC to 1MHz. The output voltage is obtained without any distortion and the simulated results are shown in the figures. 5(a), 5(b) and 5(c).

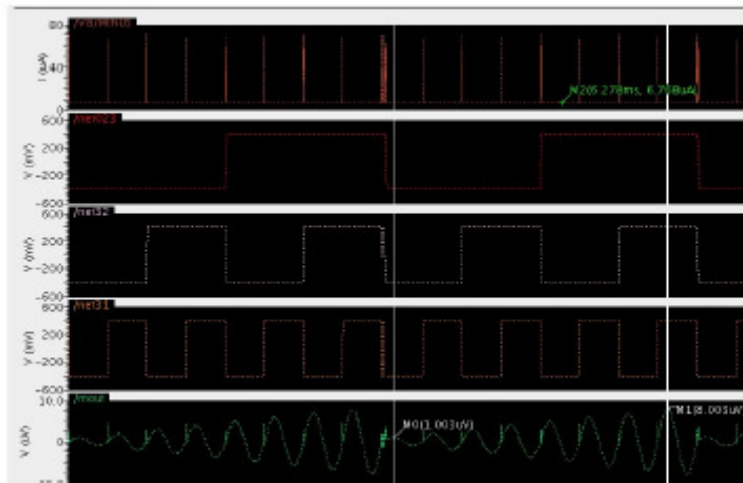


Fig: 5(a) simulated results with an amplitude of 1uV

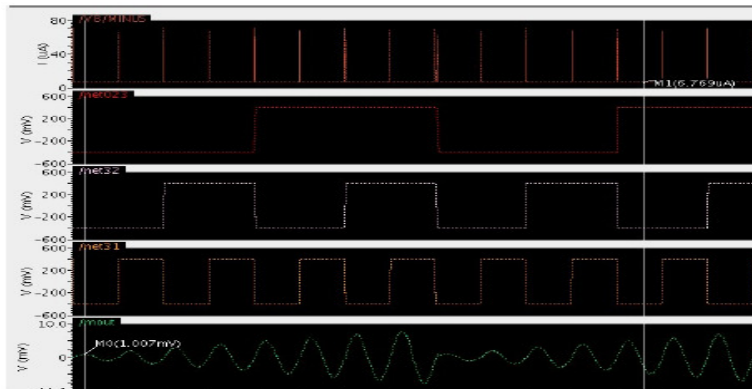


Fig: 5(b) simulated results with an amplitude of 1mV

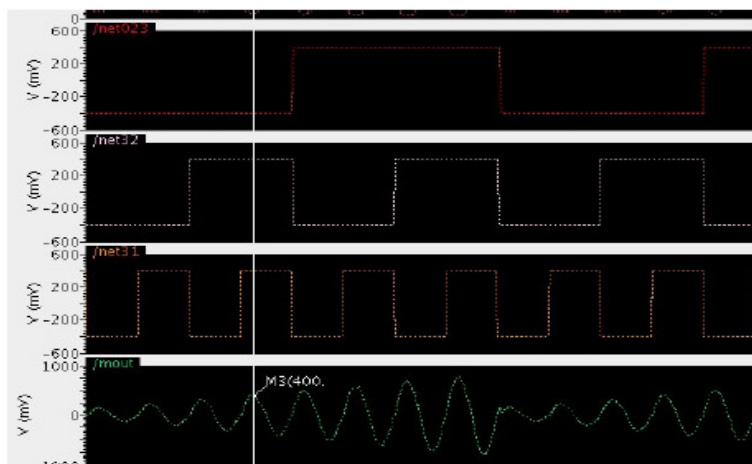


Fig: 5(c) simulated results with an amplitude of 100mV to 400mV

The dynamic power dissipation is measured at various switching frequencies ranging from DC to 1 MHz. the power calculated is 2.648uW up to a switching frequency of 300kHz. Above this frequency the power dissipation is increased and the graph is shown in Fig(6).

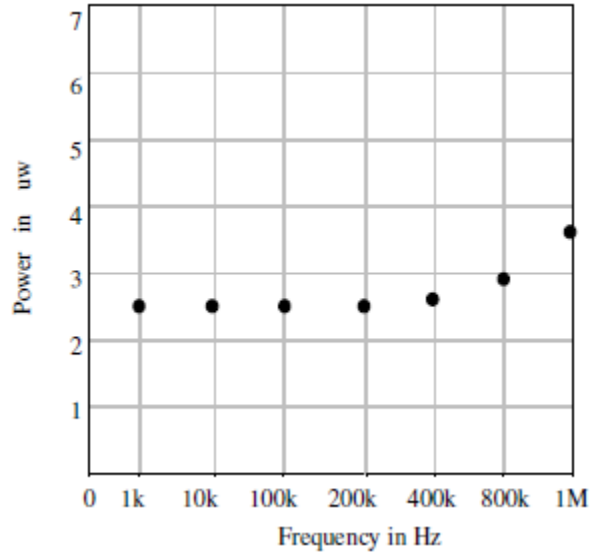


Fig: 6 switching frequency vs power dissipation

The multiplexer unit is tested by applying capacitive load. It is observed that the output followed the input without any distortion up to a load of 50nf. Above 50nf and up to 100nf the signal is distorted with maximum distortion above 100nf.

5. CONCLUSION

An eight channel, low power, high speed, lossless multiplexer is designed and simulated using 180nm CMOS technology. The proposed architecture operates at a low voltage of 0.4V and consumes only minimum power of 2.648uW with a switching frequency of 300 KHz. The circuit has been designed as a building block for a multi-channel Application Specific Integrated Circuit (ASIC) for recording ECG, EEG signals from human body. The number of channels can be extended by cascading.

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