A NEW EFFICIENT FPGA DESIGN OF RESIDUE-TO-BINARY CONVERTER

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ABSTRACT

In this paper, we introduce a new 6n bit Dynamic Range Moduli set { 2^{2n}, $2^{2n} + 1$, $2^{2n} – 1$} and then present its associated novel reverse converters. First, we simplify the Chinese Remainder Theorem in order to obtain an efficient reverse converter which is completely memory less and adder based. Next, we present a low complexity implementation that does not require the explicit use of modulo operation in the conversion process and we demonstrate that theoretically speaking it outperforms state of the art equivalent reverse converters. We also implemented the proposed converter and the best equivalent state of the art reverse converters on Xilinx Spartan 6 FPGA. The experimental results confirmed the theoretical evaluation. The FPGA synthesis results indicate that, on the average, our proposal is about 52.35% and 43.94% better in terms of conversion time and hardware resources respectively.

KEYWORDS

Dynamic Range, reverse converters, Field programmable gate arrays, Residue Arithmetic, Chinese Remainder Theorem

1. INTRODUCTION

The use of alternative number systems in the implementation of application specific Digital Signal Processing (DSP) systems has gained a remarkable importance in recent years. This is due to the carry propagation problem associated with the conventional number system such as the binary numbers. The attractive carry free properties of Residue Number System (RNS) makes it a suitable candidate. RNS is an integer system which has the potential for high speed and parallel computations. RNS is mostly applied in addition and multiplication dominated DSP applications such as Digital Filtering and Convolutions [1]. In RNS, arithmetic operations such addition, subtraction, and multiplication can be carried out independently and concurrently in several residue channels more efficiently than in the conventional binary system [2].

The difficult RNS arithmetic operations include: division, magnitude comparison, overflow detection, sign detection, moduli selection and reverse conversion. For a successful RNS implementation, moduli selection and reverse conversion are the most critical issues. Reverse conversion has become an important research topic as the solution to the other RNS arithmetic operations depend largely on conversion. In literature, moduli sets that have been presented are

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classified according to the number of channels or their lengths and their Dynamic Range (DR). Length-3 moduli sets such as $\{2^n, 2^n\text{-}1, 2^n\text{+}1\}$ [3], [4], [5], $\{ 2^n, 2^n\text{ -}1, 2^{n-1} - 1\}$ [6], [7], $\{ 2^n, 2^{n+1} - 1, 2^n - 1 \}$ [8], [9] have been investigated extensively. Subsequently, other moduli sets with larger DR have been introduced, examples of which are $\{ 2^{2n+1} – 1, 2^n, 2^n – 1 \}$ [10], $\{ 2^{2n}, 2^{2n+1} – 1, 2^n – 1 \}$ [11], $\{ 2^{2n+1} – 1, 2^{2n+1}, 2^{2n} – 1 \}$ [12] and $\{ 2^n, 2^{2n} – 1, 2^{2n} + 1\}$ [13].

Several reverse conversion techniques have been proposed based on either the Chinese Remainder Theorem (CRT) [14], [15], [16], or the Mixed Radix Conversion (MRC) [17]. The major CRT problem is the complex and slow modulo-M operation ($M = m_1m_2m_3...m_n$ being the system dynamic range, thus a rather large constant to deal with).

In this paper, we introduce a novel moduli set $\{ 2^{2n}, 2^{2n} + 1, 2^{2n} - 1\}$ by enhancing the modulus 2^n to 2^{2n} in $\{ 2^n, 2^{2n} + 1, 2^{2n} - 1 \}$ [13]. Next, we present an efficient reverse converter based on the CRT which results in efficient VLSI architecture design with high speed conversion and low cost hardware requirements. Theoretically, our proposal outperforms equivalent state of the art converters. We also implemented the proposed converter and the best equivalent state of the art converters on Xilinx Spartan 6 FPGA. The synthesis results are given in terms of the number of slices and input-to-output gate delays in nano seconds. The results indicate that, on the average, our proposal is about 52.35% and 43.94% better than existng equivalent state of the art in terms of conversion time and hardware resource utilization respectively.

The rest of the paper is structured as follows. Section 2 provides a brief background information on reverse conversion. In Section 3, the novel moduli set is introduced, and the associated reverse conversion algorithm is presented. The hardware implementation of the proposed algorithm is described in Section 4, and Section 5 evaluates the performance of the proposed scheme. Finally, the paper is concluded in Section 6.

RNS is defined in terms of a set of relatively prime moduli set $\{m_i\}_{i=1,k}$, such that $\gcd(m_i,m_j) = 1$ for $i \neq j$, where $\gcd(m_i,m_j)$ means the greatest common divisor of m_i and m_j, while $M = \prod_{i=1}^{k} m_i$, is the dynamic range. The residues of a decimal number X can be derived as $x_i = |X|_{mi}$ denotes X mod m_i operation.

The main methods for reverse conversion are based on the CRT, New CRT and MRC techniques. In this paper, we utilizes the CRT. Given a moduli set $\{m_i\}_{i=1,3}$, the residues (x_1, x_2, x_3) can be converted into the corresponding decimal number X using the CRT as follows [2] :

$$X = \left| \sum_{i=1}^{k} m_i \left| M_i^{-1} \right|_{m_i} x_i \right|_M \qquad (1)$$

Where $M = \prod_{i=1}^{k} m_i$, $M_i = \frac{M}{m_i}$ and M_i^{-1} is the multiplicative inverse of M_i with respect to (w.r.t) m_i

The complexity of Equation [1] is significantly reduced by using the proposed moduli set $\{ 2^{2n}, 2^{2n} + 1, 2^{2n} – 1 \}$.

2. NEW MODULI SET WITH PROPOSED REVERSE CONVERTER

For a given RNS moduli set to be legitimate, it is required that all the elements in the set to be co-prime. Thus, in order to prove that the proposed set can be utilized for the construction of valid RNS architecture, we have to demonstrate that the moduli 2^{2n}, 2^{2n} + 1 and 2^{2n} – 1 are pair-wise relatively prime.

Theorem 1. *The moduli* $2^{2n}, 2^{2n}+1$, *and* $2^{2n}-1$ *are pair-wise relatively prime numbers.*

Proof. :
Since $2^{2n}+1$, and $2^{2n}-1$ have been already shown to be relatively prime by [13], we only need to demonstrate that 2^{2n} is coprime to $2^{2n}+1$, and $2^{2n}-1$. From the Euclidean theorem, we have $gcd(a,b) = gcd(b,|a|_b)$. Therefore, $gcd(2^{2n}, 2^{2n}+1) = gcd(2^{2n}+1, \left|2^{2n}\right|_{2^{2n}+1}) = gcd(2^{2n}, -1) = 1$. Similarly, $gcd(2^{2n}, 2^{2n}-1) = gcd(2^{2n}-1, \left|2^{2n}\right|_{2^{2n}-1}) = gcd(2^{2n}, 1) = 1$. The numbers $2^{2n}, 2^{2n}+1$, and $2^{2n}-1$ are pairwise relatively prime because all the greatest common divisors are 1.

Theorem 2. *Given that the moduli set* $\{m_1, m_2, m_3\}$ *with* $m_1 = 2^{2n}$, $m_2 = 2^{2n}+1$, *and* $m_3 = 2^{2n}-1$ *the following holds true:*

$$\left|(m_2 m_3)^{-1}\right|_{m_1} = -1 \tag{2}$$

$$\left|(m_1 m_3)^{-1}\right|_{m_2} = -2^{2n-1} \tag{3}$$

$$\left|(m_1 m_2)^{-1}\right|_{m_3} = 2^{2n-1} \tag{4}$$

Proof. :
If it can demonstrated that $|(2^n+1)\times(2^n-1)\times -1|_{2^{2n}} = 1$, then -1 is the multiplicative inverse of $(2^n+1)\times(2^n-1)$ with respect to 2^{2n}: $\left|(2^{4n-1})\times -1\right|_{2^{2n}} = 1$. Similarly, $\left|(2^{2n})\times(2^{2n}-1)\times(-2^{2n-1})\right|_{2^{2n}+1} = \left|(2)\cdot(2^{4n-1})\right|_{2^{2n}+1} = 1$. Again $\left|(2^{2n})\times(2^{2n}+1)\times(2^{2n-1})\right|_{2^{2n}-1} = \left|(2)\cdot(2^{4n-1})\right|_{2^{2n}-1} = 1$.

The relation below is utilized in the subsequent theorem: Given the moduli set $\{m_1, m_2, m_3\}$ *with*$\mathrm{m}_1 = 2^{2n}$, $m_2 = 2^{2n}+1$, and $m_3 = 2^{2n}-1$, the relation below holds true:

$$m_2 m_3 = m_1^2 - 1 \tag{5}$$

Theorem 3. *Based on the moduli set* $\{2^{2n}, 2^{2n}+1, 2^{2n}-1\}$, *the RNS number* (x_1, x_2, x_3) *can be converted into its equivalent weighted number* X *by:*

$$X = m_1 \left\lfloor \frac{X}{m_1} \right\rfloor + x_1 \tag{6}$$

where,

$$\left\lfloor \frac{X}{m_1} \right\rfloor = \left| -m_1 x_1 - 2^{2n-1} m_3 x_2 + 2^{2n-1} m_2 x_3 \right|_{m_2 m_3} \tag{7}$$

Proof. :
From Equation (1), for $k = 3$, we obtain:

$$X = \left| M_1 \left| M_1^{-1} \right|_{m_1} x_1 + M_2 \left| M_2^{-1} \right|_{m_2} x_2 + M_3 \left| M_3^{-1} \right|_{m_3} x_3 \right|_{m_1 m_2 m_3} \tag{8}$$

Using Equations (2), (3), and (4) in the above equation, we have:

$$X = \left| -m_2 m_3 x_1 + m_1 m_3 (-2^{2n-1}) x_2 + m_1 m_2 (2^{2n-1}) x_3 \right|_{m_1 m_2 m_3} \tag{9}$$

Substituting Equation (5) into (9) we have:

$$X = \left| (m_1^2 - 1)(-x_1) + m_1 m_3 (-2^{2n-1}) x_2 + m_1 m_2 (2^{2n-1}) x_3 \right|_{m_1 m_2 m_3} \tag{10}$$

Dividing both sides of Equation (10) by m_1 and computing the floor value of both sides, we obtain:

$$\left\lfloor \frac{X}{m_1} \right\rfloor = \left| -m_1 x_1 - 2^{2n-1} m_3 x_2 + 2^{2n-1} m_2 x_3 \right|_{m_2 m_3} \tag{11}$$

Equation (11) can therefore be directly rewritten as:

$$\left\lfloor \frac{X}{2^{2n}} \right\rfloor = \left| -2^{2n} x_1 - (2^{2n-1})(2^{2n} - 1) x_2 + 2^{2n-1}(2^{2n} + 1) x_3 \right|_{m_2 m_3} \tag{12}$$

Following the basic integer divison definition in RNS, we finally have:

$$X = m_1 \left\lfloor \frac{X}{m_1} \right\rfloor + x_1 \tag{13}$$

$$= 2^{2n} \left\lfloor \frac{X}{2^{2n}} \right\rfloor + x_1 \tag{14}$$

In order to reduce the hardware complexity, we use the following properties to simplify Equation (12):

Property 1 : The multiplication of a residue number by 2^k in modulo $(2^P - 1)$ is computed by k bit circular left shifting

Property 2 : A negative number in modulo $(2^p - 1)$ is calculated by subtracting the number in question from $(2^p - 1)$. In binary representation, the ones complement of the number gives the result.

Let the residues (x_1, x_2, x_3) have binary representation as follows:

$$x_1 = (\underbrace{x_{1,2n-1}x_{1,2n-2}...x_{1,1}x_{1,0}}_{2n}) \tag{15}$$

$$x_2 = (\underbrace{x_{2,2n}x_{2,2n-1}...x_{2,1}x_{2,0}}_{2n+1}) \tag{16}$$

$$x_3 = (\underbrace{x_{3,2n-1}x_{3,2n-2}...x_{3,1}x_{3,0}}_{2n}) \tag{17}$$

Equation (12) can be directly rewritten as :

$$\left\lfloor \frac{X}{2^{2n}} \right\rfloor = |u_1 + u_2' + u_2'' + u_3'''|_{2^{4n}-1} \tag{18}$$

Where,

$$u_1 = \left|-2^{2n}x_1\right|_{2^{4n}-1} = \underbrace{\overline{x}_{1,2n-1}\overline{x}_{1,2n-2}...\overline{x}_{1,0}}_{2n}\underbrace{11...11}_{2n} \tag{19}$$

$$u_2 = \left|-2^{4n-1}x_2 + 2^{2n-1}x_2\right|_{2^{4n}-1} \tag{20}$$

$$u_2' = \left|-2^{4n-1}x_2\right|_{2^{4n}-1} = \overline{x}_{2,0}\underbrace{11...11}_{2n-1}\underbrace{\overline{x}_{2,2n}\overline{x}_{2,2n-1}...\overline{x}_{2,1}}_{2n} \tag{21}$$

$$u_2'' = \left|2^{2n-1}x_2\right|_{2^{4n}-1} = \underbrace{x_{2,2n}x_{2,2n-1}...x_{2,0}}_{2n+1}\underbrace{00...00}_{2n-1} \tag{22}$$

$$u_3 = \left|2^{4n-1}x_3 + 2^{2n-1}x_3\right|_{2^{4n}-1} \tag{23}$$

$$u_3' = \left|2^{4n-1}x_3\right|_{2^{4n}-1} = x_{3,0}\underbrace{00...00}_{2n}\underbrace{x_{3,2n-1}...x_{3,1}}_{2n-1} \tag{24}$$

$$u_3'' = \left|2^{2n-1}x_3\right|_{2^{4n}-1} = 0\underbrace{x_{3,2n-1}...x_{3,0}}_{2n}\underbrace{00...00}_{2n-1} \tag{25}$$

By considering Equation (24) and (25), it is clear that they can be manipulated to obtain u_3''' represented as:

$$u_3''' = x_{3,0}\underbrace{x_{3,2n-1}...x_{3,0}}_{2n}\underbrace{x_{3,2n-1}...x_{3,1}}_{2n-1} \tag{26}$$

3. HARDWARE REALIZATION

The hardware structure of the proposed reverse converter for the moduli set $\{2^{2n}, 2^{2n}+1, 2^{2n}-1\}$ is based on Equation (18) and (14). Figure 1 and 2 represents the block diagram of the proposed Cost Efficient (CE) and Speed Efficient (SE) converter respectively . In Equation (14), the parameters $u_1, u_2', u_2'',$ and u_3''' are added using two $4n$ bit Carry Save Adders (CSA) with end around carry to produce s_2 and c_2. Next, these must be added modulo $2^{4n}-1$ in order to obtain $\left\lfloor \frac{X}{m_1} \right\rfloor$ to achieve a CE converter. The final result, computed from Equation (14) is therefore obtained simply by a shift and a concatenation operation, which requires no additional hardware resouces. To achieve a SE converter, we speed up the addition process by utilizing anticipated computation. By this, we compute $s_2 + c_2$ for both $cin = 0$ and $cin = 1$ and then the right result is selected with a MUX. Again, the implementation of Equation (14) to obtain the final result requires no additional hardware.

For the sake of completeness, some of the Full Adders (FAs) are reduced to Half Adders (HAs) because some of the inputs of the CSA have constant values of 0's and 1's. It can be observed that our CE proposal utilizes $10nFA$ and $2nHA$ and a conversion time of $(8n+2)t_{FA}$, while the SE converter requires $10nFA$, $2nHA$ and t_{MUX}, with a delay of $(4n+2)t_{FA} + t_{MUX}$.

4. PERFORMANCE ANALYSIS

The performance of the proposed reverse converter is evaluated in terms of hardware cost and conversion term. In order to properly evaluate the performance of our proposal against state of the art, both theoretical and experimental analysis are performed.

4.1 Theoretical Evaluation

We compare our converter with state of the art converters presented in [18], [13], and [19]. It must be noted that in [18] and [13], the converters presented are for 5n bit DR moduli sets, while [19] is a 6n bit DR moduli set. The inclusion of [18] and [13] in the comparison is to demonstrate that, our converter can compete favourably with other existing state of the art 5n bit DR moduli sets and for the fact that our proposed moduli set is an improvement of [13]. The theoretical analysis is presented in Table [1]. From the table, it is seen clearly that our proposal outperforms the existing similar dynamic range state of the art converters in terms of area and delay.

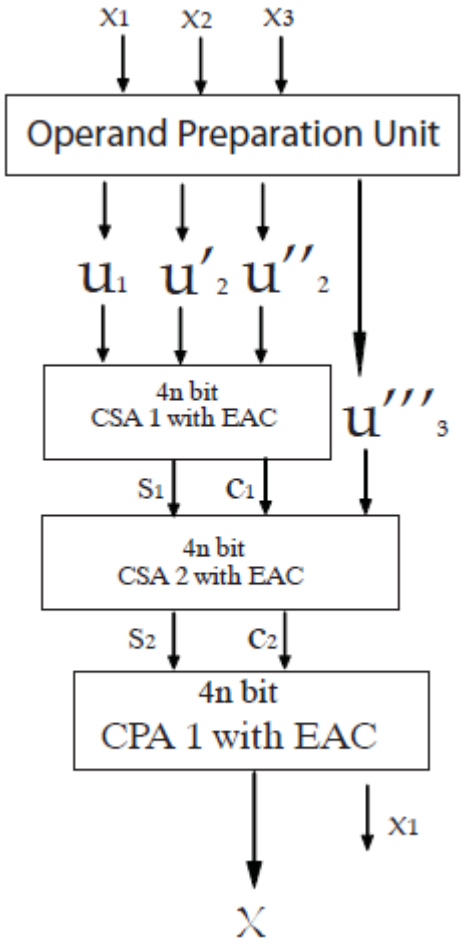

Fig 1. Proposed Cost Efficient Reverse Converter

For our CE converter, the delay is $(8n + 2)\ t_{FA}$ while that of [19] exhibits a delay of $(12n + 6)\ t_{FA.}$ To further simplify the area comparison, we assume that one FA is twice large as an HA, and the expressed the area cost for all the considered designs in terms of HA. It is therefore evident that our converter utilizes lesser area resources.

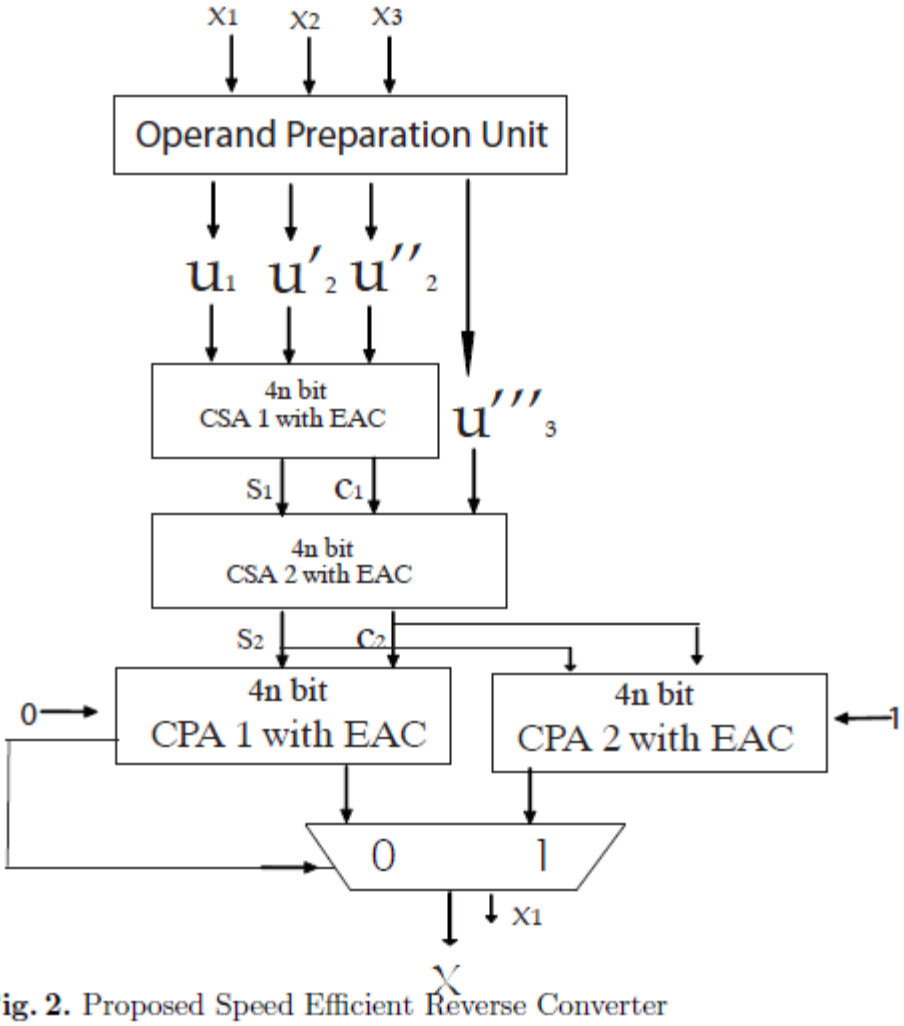

Fig. 2. Proposed Speed Efficient Reverse Converter

4.2 Experimental Evaluation

For the experimental assessment, the converters were described in VHDL and then implemented on Spartan 6 xc6slx45t-3fgg484 FPGA, with Xilinx ISE 14.3 for various dynamic range requirements. The performance is evaluated in terms of area measured according the number of slices and delay corresponding to the critical path in nanoseconds. Table 2 shows the synthesized results for the various values of n. To confirm the theoretical results, the experimental results clearly shows the superiority of our converter over the state of the arts. In comparison with the reverse converter presented by [19], the generated values strongly suggest that, on the average, our proposal is capable of performing 52.35% faster than the converter proposed by [19]. Also, in terms of area cost our converter exhibits a 43.94% reduction with respect to state of the art. Figures 3 and 4 presents the performance of our proposal against state of the art in terms of delay and area.

Table 1. Theoretical Area and Delay Comparison

Converter	13	18	19	Proposed Converters	
Moduli Set	$\{2^n, 2^{2n}-1, 2^{2n}+1\}$	$\{2^n-1, 2^n, 2^n+1, 2^{2n}+1\}$	$\{2^n-1, 2^n+1, 2^{2n}, 2^{2n+1}-1\}$	$\{2^{2n}, 2^{2n}+1, 2^{2n}-1\}\,(SE)$	$\{2^{2n}, 2^{2n}+1, 2^{2n}-1\}\,(CE)$
DR	$5n$	$5n$	$6n$	$6n$	$6n$
FA	$7n+1$	$11n+4$	$12n+2$	10	$10n$
HA	$n-1$	$9n-4$	$4n+1$	$2n$	$2n$
Area Cost in HA (Δ)	$15n+1$	$31n+4$	$28n+5$	$22n$	$22n$
MUX	–	–	–	1	–
Delay	$(8n+1)t_{FA}$	$(8n+3)t_{FA}$	$(12n+6)t_{FA}$	$(4n+2)t_{FA}+t_{MUX}$	$(8n+2)t_{FA}$

Table 2. Implementation Result : Area, Delay

Converter	18		19		Proposed Converter	
n	Delay	Area	Delay	Area	Delay	Area
2	18.202	54	26.650	72	15.541	36
4	22.020	107	37.011	141	17.189	71
6	26.074	157	43.637	209	20.870	113
8	24.507	210	42.755	275	22.909	152
10	26.983	270	51.522	351	24.396	197
12	26.647	327	51.892	426	24.508	238
14	27.640	386	56.011	498	25.749	286
16	28.392	440	57.778	563	26.286	324
18	29.724	489	61.110	635	27.422	358
20	29.971	546	59.663	713	27.656	402

5. CONCLUSIONS

In this paper we proposed a novel moduli set $\{2^{2n}, 2^{2n} + 1, 2^{2n} – 1\}$ with its associated reverse converter using the CRT. The moduli set is a 6n bit DR and therefore appropriate for applications requiring specifically 6n DR. We simplified the CRT to obtain an effective algorithm. Further, we reduced the resulting architecture in order to obtain a reverse converter that utilizes only two CSAs and a CPA. We performed both theoretical and experimental evaluation of our proposal. The theoretical analysis shows clearly the advantages of our moduli set and its associated reverse converter. This is confirmed by the experimental results. We described our scheme and those presented by [18] and [19] in VHDL and carried out the implementation on an FPGA using a wide range of values on n. The results indicate that on the average, our scheme is 52.35% faster than the converter proposed by [19] in terms of speed, while it exhibits a 43.94% reduction in area cost. Clearly, the results show that, our proposal outperforms the best known state of the art.

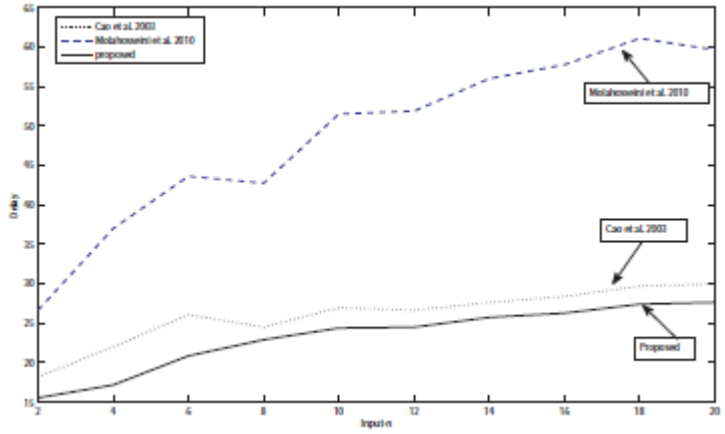

Fig. 3. The Delay Comparison of Converters

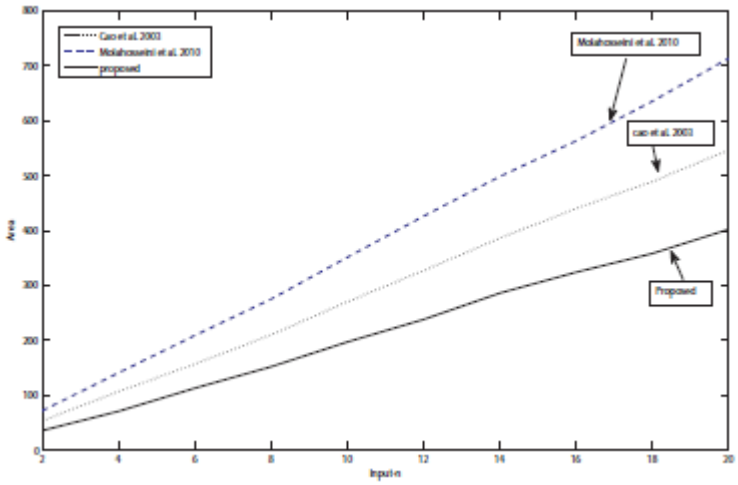

Fig. 4. The Area Comparison of Converters

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