A DIGITAL CALIBRATION ALGORITHM WITH VARIABLE-AMPLITUDE DITHERING FOR DOMAIN-EXTENDED PIPELINE ADCS

Ting Li[1] and Chao You[2]

[1]Department of Electrical and Computer Engineering,
North Dakota State University, Fargo, USA
[2]Information Engineering School, Nanchang University, Nanchang, China

ABSTRACT

The pseudorandom noise dither (PN dither) technique is used to measure domain-extended pipeline analog-to-digital converter (ADC) gain errors and to calibrate them digitally, while the digital error correction technique is used to correct the comparator offsets through the use of redundancy bits. However, both these techniques suffer from three disadvantages: slow convergence speed, deduction of the amplitude of the transmitting signal, and deduction of the redundancy space. A digital calibration algorithm with variable-amplitude dithering for domain-extended pipeline ADCs is used in this research to overcome these disadvantages. The proposed algorithm is implemented in a 12-bit, 100 MS/s sample-rate pipeline ADC. The simulation results illustrate both static and dynamic performance improvement after calibration. Moreover, the convergence speed is much faster.

KEYWORDS

Analog-to-digital Converter, Digital Calibration, Variable-amplitude Dithering

1. INTRODUCTION

The switched capacitor pipeline ADC is mainstream architecture in wireless communication and digital consumer products. The performance of the switched capacitor pipeline ADC is significantly limited by the linear errors due to comparator offsets, capacitor mismatches, and finite operational-amplifier gain. A trend in modern ADC design is to utilize digital background calibration to calibrate both capacitor mismatches and finite operational-amplifier gain [1] – [12]. In contrast, a 14-bit level performance without calibration has been achieved by carefully matching the capacitors, using high open-loop gain operational-amplifiers and a multi-bit first stage [13] [14]. Therefore, in order for a digital calibration to be useful, it should minimize the analog circuits as well as the reasonable convergence time. Fortunately, digital circuits have higher speeds and lower power consumption as compared to an analog counterpart [15].

Indeed, many digital calibration algorithms have been reported. For example, the parallel-ADC algorithm uses a high accuracy but slow ADC to calibrate the errors of a high speed ADC [16]. This architecture requires an extra ADC, which costs both more power consumption and chip area. On the other hand, the statistic-based algorithm [11] requires both a large memory to store statistic data and an extremely low convergence speed. However, in the dither-based algorithm [5, 6], the gain errors are modulated with a pseudorandom noise sequence (PN sequence) in the analog domain and the gain errors are demodulated in the digital domain in order to extract the

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errors from the processed input signal. In [12], the injection of dithers, together with the comparator offsets, makes the output voltage of the current stage exceed the input range of the following stage. This out-of-range input leads to a code loss. Two options are reported to prevent an ADC from a code loss. The first option is to reduce the amplitude of the input signal, which causes the transmitting signal's signal-to-noise ratio (SNR) to decrease [12]. The other option is to reduce the amplitude of the dither, which leads to a longer convergence time [17] [18].

To overcome these two conflicting issues, this paper introduces a variable-amplitude dither-based algorithm to calibrate gain errors for domain-extended ADC. The proposed algorithm ensures higher dither amplitude without reducing the amplitude of the input signal; therefore, the convergence speed is much faster without harming the SNR of the transmitting signal. A similar scheme is used in the traditional 1.5-bit/stage pipeline ADC to calibrate gain errors [9]. Moreover, the algorithm is used in domain-extended pipeline ADCs and results in more space for the comparator offsets.

This paper is organized as follows. The variable-amplitude dither-based digital background calibration algorithm is described in Section 2. The proposed algorithm to correct all linear errors is described in Section 3. Simulation results from the modelled 12-bit ADC are discussed in Section 4 and conclusions are presented in Section 5.

2. VARIABLE-AMPLITUDE DITHER-BASED DIGITAL BACKGROUND CALIBRATION ALGORITHM

Figure 1 shows the block diagram of a pipeline ADC using the traditional 1.5-bit/stage converter. The pipeline ADC consists of multiple cascaded stages. Figure 2 shows the configuration of the traditional 1.5-bit/stage ADC. Although the actual configuration is fully differential, the single-ended configuration is shown for simplicity. In each stage, the converter works on two phases. When Φ_1 is high, it works on sample phase with the input simultaneously sampled on both capacitors. In contrast, when Φ_2 is high, it works on amplification phase with the input quantized by the sub-ADC and the residue amplified to the full-scale of the next stage by a multiplying digital-to-analog converter (MDAC) [19].

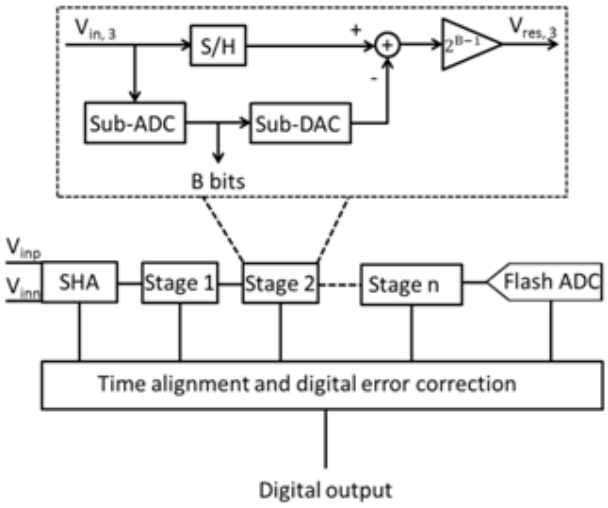


Figure 1. Pipeline ADC block diagram

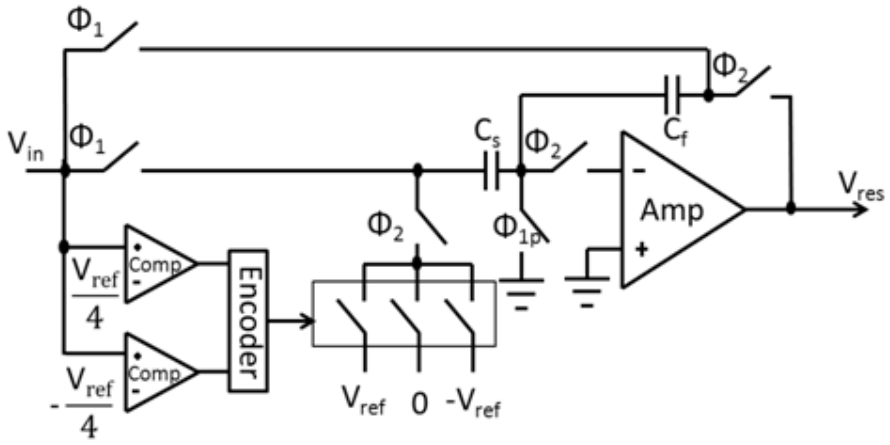


Figure 2. Single stage converter in two phases

The performance of an ADC is highly dependent on the amplifier residue, because the comparator offset can be corrected by the digital error correction technique using redundancy bits [20]. The two major non-idealities which affect the amplifier residue are finite open-loop gains and capacitor mismatches. The modelled feedback network is shown in Figure 3 with the real close-loop gain G as [21]

$$G = \frac{g}{1 + g\beta} \tag{1}$$

where g is the open-loop gain and β is the feedback factor.

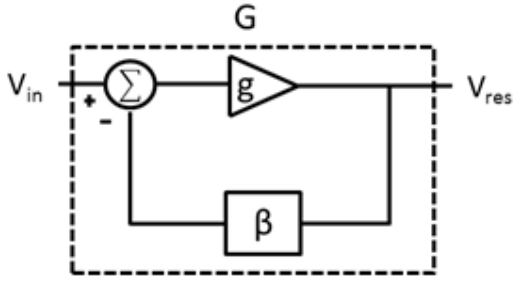


Figure 3. Feedback network of a signal stage converter

When the open-loop gain approaches infinity,

$$G|_{g\to\infty} = \frac{1}{\beta} = \frac{C_s}{C_f} \tag{2}$$

where C_s and C_f are sample-and-hold capacitors as shown in Figure 1. According to Franco [21], for a voltage-to-voltage converter, $\frac{1}{\beta}$ equals the close-loop gain of the converter when the amplifier is ideal.

In contrast to the ideal, the real close-loop gain G shown in Equation (1) can be factorized into

$$G = \frac{g}{1+g\beta} = \frac{1}{\beta}\frac{1}{1+\frac{1}{g\beta}} \tag{3}$$

The real gain G shown in Equation (3) helps find the real amplifier residue of the current stages

$$V_{res} = G\,(V_{in} - \frac{1}{2}V_{DAC}) \tag{4}$$

Subscribing Equations (2) and (3) into Equation (4) yields

$$V_{res} = \frac{1}{\beta}\frac{1}{1+\frac{1}{g\beta}}\left(V_{in} - \frac{1}{2}V_{DAC}\right) = \frac{C_s}{C_f}\frac{1}{1+\frac{C_f}{gC_s}}\,(V_{in} - \frac{1}{2}V_{DAC}) \tag{5}$$

Equation (5) takes both comparator mismatches and finite open-loop gain into consideration. Therefore, both non-ideal factors that affect the amplifier residue can be combined into one error, called the gain error. Thus, the real close-loop gain is

$$G_{real} = \frac{C_s}{C_f}\frac{1}{1+\frac{C_f}{gC_s}} \tag{6}$$

The equivalent model for a single stage ADC is shown in Figure 4.

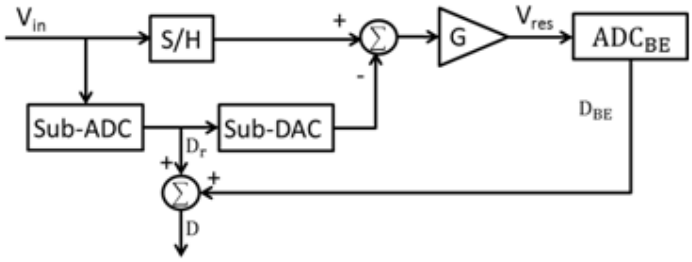


Figure 4. Modelled single stage converter

Wang, Hurst, & Lewis [4] present the expression for the output word in the real condition as

$$D = D_r + \frac{1}{G_{real}}D_{BE} \tag{7}$$

where G_{real} is the real close-loop gain, D_r is the real output code, and D_{BE} is the output code of the back-end ADC. The estimation of $m = \frac{1}{G_{real}}$ is m_e. Equation (7) can be rewritten as

$$D = D_r + m_e D_{BE} \tag{8}$$

$$D_{BE} = V_{res} = G_{real}\,(V_{in} - D_r) \tag{9}$$

Subscribing Equation (9) into Equation (8) yields

$$D = D_r + m_e\, G_{real}\,(V_{in} - D_r) = V_{in}\,(1 + e) - D_r e \tag{10}$$

in which

$$e = \frac{m_e - m}{m}. \tag{11}$$

e then, is the error coefficient in the estimate m_e of $m = \frac{1}{G_{real}}$. In order to extract the error coefficient e from Equation (11), one must use the following equation:

$$D_r = D_b + PN\,\Delta A\,, \tag{12}$$

where D_b is the output word of the sub-ADC without the injection of the PN sequence and ΔA is the amplitude of the PN sequence. $PN \in \{-1, 1\}$ represents pseudorandom noise sequence. Subscribing Equation (12) into Equation (10) yields

$$D = V_{in}\,(1 + e) - D_b e - PN\,\Delta A e. \tag{13}$$

If the PN sequence uncorrelated with the input signal, then correlating D with PN can get the error coefficient e. In order to fit the architecture used here, a new parameter is defined as

$$F(n) = D(n) - D_b(n) \tag{14}$$

where n is the number of conversion.

Because the Equations (10) and (12) include error coefficient e, the error coefficient e can then be extracted from Equation (14). Subscribing both Equation (10) and Equation (12) into Equation (14) yields

$$F(n) = (V_{in}(n) - D_b(n))(1 + e) - PN(n)\Delta A e. \tag{15}$$

Correlating F with PN will give an estimate of error coefficient e; Therefore, multiplying Equation (15) with PN yields

$$PN(n) \cdot F(n) = PN(n)(V_{in}(n) - D_b(n))(1 + e) - PN^2(n)\Delta A e \tag{16}$$

The next step is to calculate the average (represented by E[.]) with an infinite number of cumulative sums. Since $PN(n) \in \{-1, 1\}$, the first term in Equation (16) equals zero and yields

$$E[PN \cdot F] = -\Delta Ae \,. \tag{17}$$

As shown in Equation (17), the error coefficient e from the analog domain is extracted in the digital domain. Adopting the least mean square (LMS) iterative calculation, m_e keeps renewing until it approaches m. The LMS iterative is shown as

$$m_e(n) = m_e(n-1) + \mu PN(n-1)F(n-1) \tag{18}$$

where μ is the step size for LMS iterative. For a smaller step size, longer convergence time needed for an ADC to be stable. However, for a larger step size, larger stead-state errors existed for an ADC.

3. CALIBRATION WITH VARIABLE-AMPLITUDE DITHERING FOR DOMAIN-EXTENDED ARCHITECTURE

There are two constraints to the traditional technique. First, the dither amplitude constraint originates from the trade-off between the dither amplitude and the signal amplitude. The signal amplitude reduction leads to a decline of the SNR. Although a smaller dither amplitude makes the signal amplitude larger, the smaller dither amplitude also requires longer convergence time. Second, the redundancy space constraint results from the trade-off between the redundancy space and the total amplitudes of the signal and the dither. The total amplitudes of the signal and the dither reduction leads to either lower SNRs or longer convergence times. Although less redundancy space makes the amplitude of the signal plus dither larger, it leaves less redundancy to allow comparator offsets to be corrected.

A variable-amplitude dither used for domain-extended architecture is proposed to relieve both the dither amplitude constraint and the redundancy space constraint. The amplitude of the dither is variable according to the signal level. In this case, the amplitude of the dither is greatly increased without a reduction of the amplitude of the signal; therefore, the convergence speed is much faster without harming the SNR of the ADC. Moreover, the existence of more redundancy space in the domain-extended architecture allows for the comparator offsets within a certain range to be corrected.

The residue plot of a traditional 1.5-bit/stage ADC is shown in Figure 5 (a). The threshold voltages are $-\frac{1}{4}V_{ref}$ and $\frac{1}{4}V_{ref}$. The input range is from $-V_{ref}$ to V_{ref}. Since the output of the current stage is the input of the following stage of the pipeline ADC, the output range needs to be the same as the input range to avoid a code loss. Therefore, like the input range, the output range is also from $-V_{ref}$ to V_{ref}. In contrast, the modified residue plot of a domain-extended 1.5-bit/stage ADC is shown in Figure 5 (b). After two threshold voltages are added, the threshold voltages are $-\frac{3}{4}V_{ref}$, $-\frac{1}{4}V_{ref}$, $\frac{1}{4}V_{ref}$, and $\frac{3}{4}V_{ref}$. The input range is from $-\frac{5}{4}V_{ref}$ to $\frac{5}{4}V_{ref}$. Like in the traditional architecture, in order to prevent the ADC from a code loss in the modified architecture, the output range needs to be the same as the input range: from $-\frac{5}{4}V_{ref}$ to $\frac{5}{4}V_{ref}$.

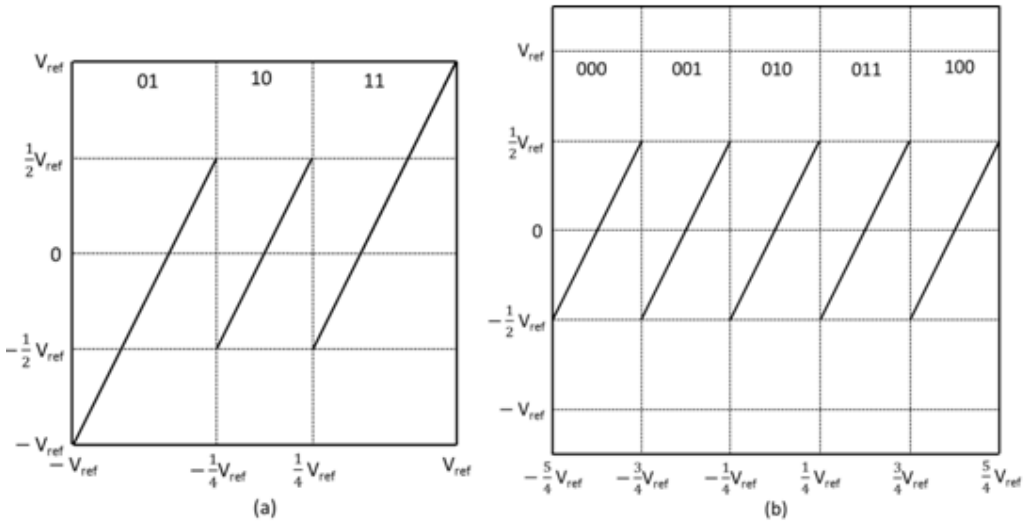


Figure 5. Residue plot of (a) a traditional 1.5-bit/stage ADC and (b) a domain-extended 1.5-bit/stage ADC

The domain-extended 1.5-bit/stage ADC allows for more space for comparator offsets, for higher amplitude of the signal, for higher amplitude of the dither, as compared to the traditional 1.5-bit/stage ADC. For domain-extended 1.5-bit/stage ADC, the total amplitudes of the signal and the dither can be set within the $-V_{ref}$ to V_{ref} range. Therefore, some space is available for comparator offsets. However, in contrast, the traditional 1.5-bit/stage ADC needs the total amplitudes of the signal and the dither to be set within the range of $-0.8V_{ref}$ to $0.8V_{ref}$ in order to have space for comparator offsets. The reduction of the total amplitudes of the signal and the dither results in either a decline of SNR or a slower convergence speed.

The residue plot of the domain-extended 1.5-bit/stage ADC with variable-amplitude dithering is shown in Figure 6 (a). The amplitude-variable dithers are injected between $-\frac{3}{4}V_{ref}$ to $-\frac{1}{4}V_{ref}$, and three more comparators with threshold voltages equal to $-\frac{5}{8}V_{ref}$, $-\frac{4}{8}V_{ref}$, and $-\frac{3}{8}V_{ref}$ are added. A dither amplitude is chosen from $-\frac{5}{4}V_{ref}$, $-\frac{4}{4}V_{ref}$, $-\frac{3}{4}V_{ref}$, $-\frac{2}{4}V_{ref}$, $\frac{2}{4}V_{ref}$, $\frac{3}{4}V_{ref}$, and $\frac{4}{4}V_{ref}$ depending on the PN value and the signal levels as shown in Figure 6(a). The total amplitudes of the signal and the dither are within $\pm V_{ref}$, and so have room for comparator redundancy. Therefore, the signal pulse dither between $-\frac{3}{4}V_{ref}$ and $-\frac{1}{4}V_{ref}$ is, in effect, a constant-amplitude dither of $\pm\frac{7}{8}V_{ref}$ with a small signal within the range of $\pm\frac{1}{8}V_{ref}$, as shown in Figure 6 (b). The actual signal stays unchanged, which means the SNR has not declined. The dither amplitude is greatly increased, which leads to a fast convergence speed.

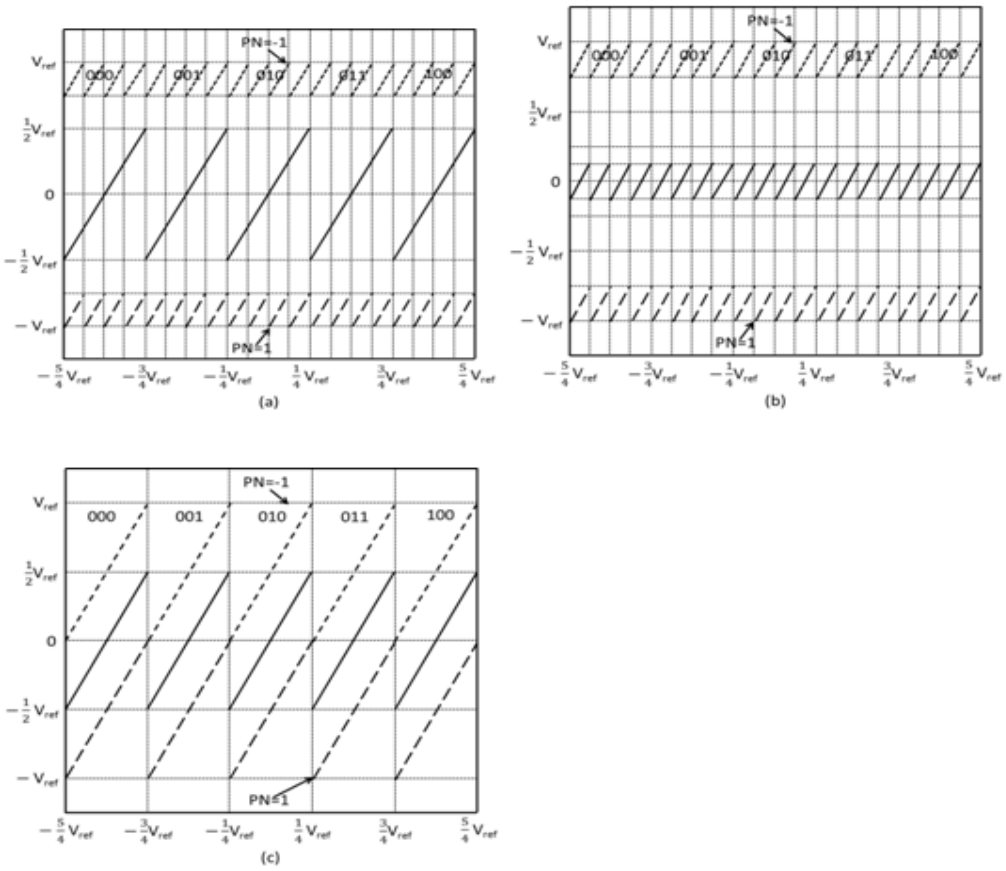


Figure 6. (a) Residue plot of the domain-extended 1.5-bit/stage ADC with variable-amplitude dithering, (b) equivalent constant-amplitude PN dithering of (a), and (c) residue plot of the domain-extended 1.5-bit/stage ADC with constant-amplitude dithering

However, for the domain-extended 1.5-bit/stage ADC with constant-amplitude dithering, the dither amplitude is only $\frac{1}{2}V_{ref}$ as shown in Figure 6 (c). As mentioned above, in the case of one signal level divided into four sub-levels, the dither amplitude is increased from $\frac{1}{2}V_{ref}$ to $\frac{7}{8}V_{ref}$ without reducing the signal amplitude. Therefore, the variable-amplitude dithering calibration allows higher amplitude of the dither without the decline of SNR.

In dither-based architecture shown in previous studies [9] [15], when the signal stays at a high level all the time, more dither cannot be added. Therefore, the error coefficient e cannot be extracted in the digital domain according to Equation (16), (17), and (18). This is because the first term of Equation (16) equals zero after an infinite number of cumulative sums and the average is calculated. The second term always equals zero because ΔA equals zero. Therefore, the LMS iterative is not applicable for this condition. This circumstance constrains the application. However, the proposed variable-amplitude dithering does not suffer from the limitation. The proposed variable-amplitude dithering also offers substantial savings in convergence times, even though the signal stays at high level at all times. This works because the signal stays at its highest level, the PN=-1, and the amplitude of the dither is $\frac{1}{2}V_{ref}$, which is the smallest dither amplitude in the proposed method.

These concepts are realized on the circuit level in the following concrete example. A MDAC works in two phases: the sample phase and the amplification phase. During the sample phase, the sample input signal is administered to all capacitors. Figure 7 shows how the MDAC works in the amplification phase with a signal range from $-\frac{3}{4}V_{ref}$ to $-\frac{1}{4}V_{ref}$. In this configuration, V_{ref} equals half of the power supply voltage V_{dd}. Variable-amplitude dithering is realized by adding three more comparators and splitting a capacitor into four capacitors, c_1, c_2, c_3, and c_4 with each capacitor valued at $\frac{c_f}{4}$. The amplitudes of the dithers, in all sub-levels of the main level from $-\frac{3}{4}V_{ref}$ to $-\frac{1}{4}V_{ref}$, are shown in Table 1. Dither injections are controlled through switches dependant on both the output of the encoder and the PN value. The following examples lay out the various permutations for the dither injections of the main level. To inject dither of $\frac{5}{4}V_{ref}$, c_1 is switched to $-V_{dd}$, and the other three capacitors are switched to $-V_{ref}$ for the signal range between $-\frac{3}{4}V_{ref} \sim -\frac{5}{8}V_{ref}$, if PN is -1. To inject dither of $-\frac{1}{2}V_{ref}$, both c_1 and c_2 are switched to V_{ref}, and the other two capacitors are switched to 0 for the signal range between $-\frac{3}{4}V_{ref} \sim -\frac{5}{8}V_{ref}$, if PN is 1. For the other main level: $-\frac{5}{4}V_{ref} \sim -\frac{3}{4}V_{ref}$ and $-\frac{1}{4}V_{ref} \sim \frac{5}{4}V_{ref}$, the dither injection method is similar as the main level: $-\frac{3}{4}V_{ref} \sim -\frac{1}{4}V_{ref}$.

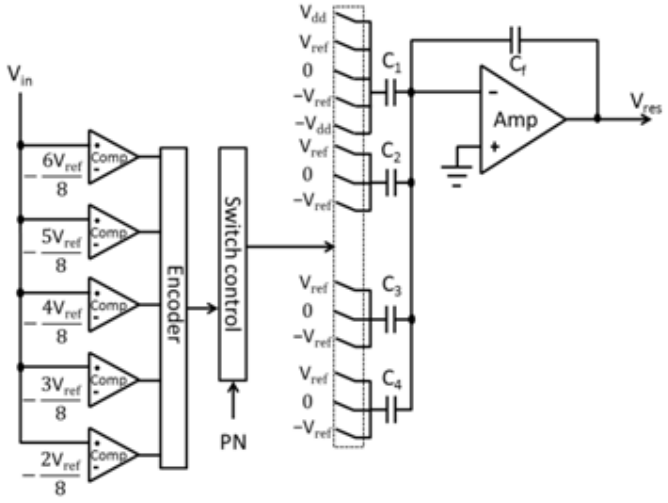


Figure 7. MDAC architecture in amplification phase with the signal range from $-\frac{3}{4}V_{ref}$ to $-\frac{1}{4}V_{ref}$

Table 1 Amplitude of the dithers in all sub-levels of the main level from $-\frac{3}{4}V_{ref}$ to $-\frac{1}{4}V_{ref}$

V_{in}		**Amplitude of dithers**	
Main level	**Sub-levels**	**PN=-1**	**PN=1**
$-\frac{3}{4}V_{ref} \sim -\frac{1}{4}V_{ref}$	$-\frac{3}{4}V_{ref} \sim -\frac{5}{8}V_{ref}$	$\frac{5}{4}V_{ref}$	$-\frac{1}{2}V_{ref}$
	$-\frac{5}{8}V_{ref} \sim -\frac{1}{2}V_{ref}$	V_{ref}	$-\frac{3}{4}V_{ref}$
	$-\frac{1}{2}V_{ref} \sim -\frac{3}{8}V_{ref}$	$\frac{3}{4}V_{ref}$	$-V_{ref}$
	$-\frac{3}{8}V_{ref} \sim -\frac{1}{4}V_{ref}$	$\frac{1}{2}V_{ref}$	$-\frac{5}{4}V_{ref}$

4. SIMULATION RESULTS

To illustrate the effectiveness of the digital calibration with the variable-amplitude dithering for the domain-extended architecture, a 12-bit pipeline ADC is simulated in Matlab. This ADC consists of ten 1.5-bit/stage converters followed by a 2-bit flash ADC with digital error correction, digital calibration, and PN sequence generation as shown in Figure 8. The gain errors and comparator offsets in all stages are chosen between 2% to 5%. The initial calibration coefficient m_e set to be its standard value, which is $\frac{1}{G} = 0.5$. Full-scale sinusoid is used as the test input. The linear gain calibration is applied to the first four stages, and the comparator offset corrections are applied to all 1.5-bit/stage converters.

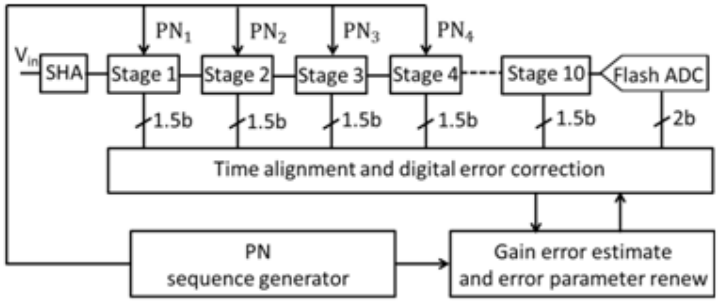


Figure 8. Block diagram of the system architecture

The convergence of the error coefficient $e = \frac{m_e - m}{m}$ for a 12-bit pipeline ADC using the proposed calibration with variable-amplitude dithering is shown in Figure 9. Convergence is reached after approximately 8×10^5 samples in this case. However, convergence is reached after approximately 4×10^6 samples in the calibration with constant-amplitude dithering [12]. At a conversion rate of 75 MS/s, the ADC using the proposed calibration with variable-amplitude dithering needs a time constant of approximately 2.2 ms, while the ADC using the calibration with constant-amplitude dithering needs a time constant of approximately 11 ms. With the increasing of ADC resolution, the LMS iterative step size μ needs to be reduced; therefore, the calibration time constant is increased accordingly. Appling the proposed calibration with variable-amplitude dithering to the high resolution ADCs can greatly reduce the convergence time.

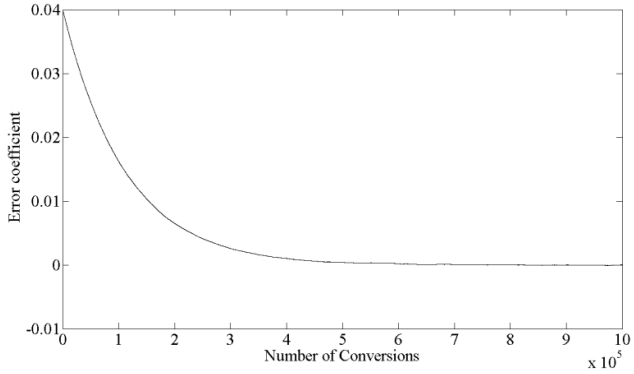
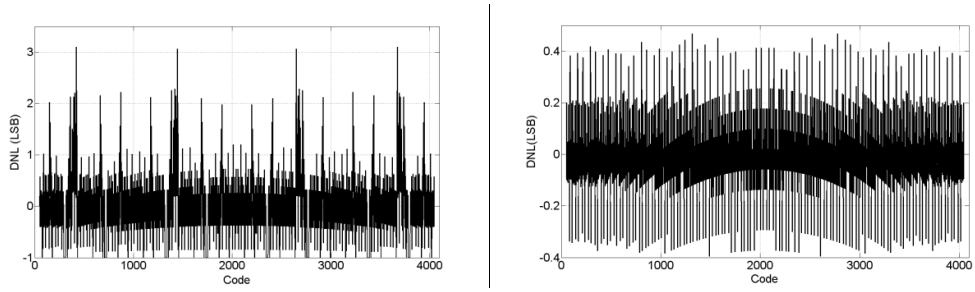


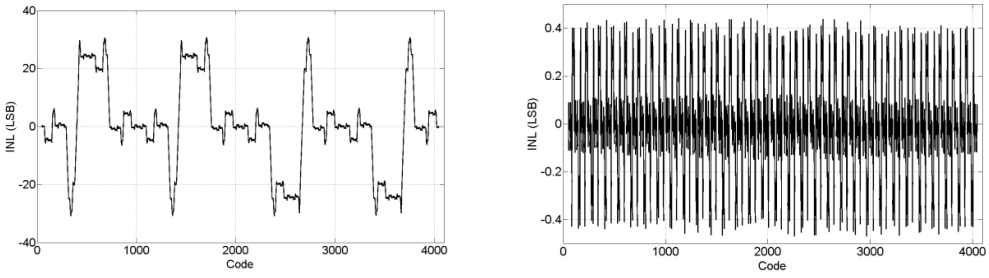
Figure 9. Convergence of the error coefficient

A full-scale sinusoidal input with low frequency is used to test the static performance. Figure 10 (a) and Figure 10 (b) show the differential nonlinearity (DNL), of a 12-bit pipeline ADC, without calibration and with calibration, respectively. The peak DNL is reduced from 3.1 LSB in the un-calibrated case to 0.5 LSB in the calibrated case. Figure 11 (a) and Figure 11 (b) show the integration nonlinearity without calibration and with calibration, respectively. The peak INL is reduced from 31 LSB in the un-calibrated case to 0.5 LSB in the calibrated case.



(a) (b)

Figure 10. 12-bit ADC DNL: (a) without calibration and (b) with calibration



(a) (b)

Figure 11. 12-bit ADC INL: (a) without calibration and (b) with calibration

A full-scale sinusoidal with an input frequency of 45 MHz and a sample-rate of 100 MS/s are used to test the dynamic performance. The output spectrum of the ADC without calibration is shown in Figure 12 (a). The spurious-free dynamic range (SFDR) in this un-calibrated case is 51 dB, while the SNR is only 40.4 dB, which corresponds to an effective number of bits (ENOB) of 6.4. Also, in this case, the total harmonic ratio (THD) is 51 dB. The output spectrum of the ADC with the proposed calibration is shown in Figure 12 (b). The tone is reduced, and the SFDR is 87.7 dB. Also the noise floor is lowered, which shows a 69.3 dB SNR with an ENOB of 11.2. The THD is 86.2 dB in the calibrated case. Table 2 shows the performance of the 12- bit ADC without calibration and with calibration.

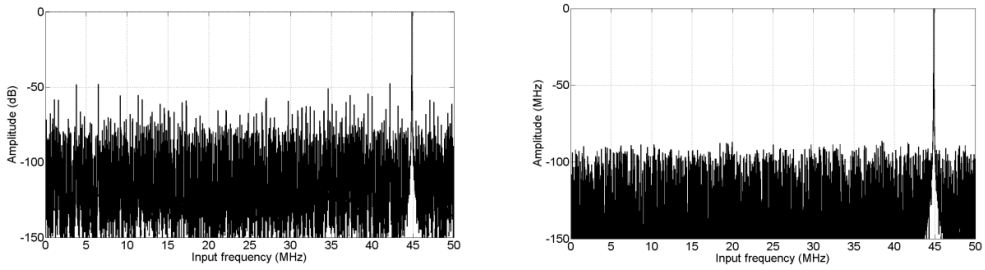


Figure 12. 12-bit ADC output spectrum: (a) without calibration and (b) with calibration

Table 2. Performance of a 12-bit ADC

Parameter	**Without calibration**	**With calibration**
Sample-rate(MS/s)	100	100
Resolution(bit)	12	12
DNL (LSB)	-1~3.1	-0.4~0.5
INL (LSB)	-31~30.8	-0.5~0.4
SFDR(dB)	51	87.7
SNR(dB)	40.4	69.3
THD(dB)	51	86.2
ENOB(bit)	6.4	11.2

5. CONCLUSION

A digital calibration with variable-amplitude dithering is applied to a domain-extended pipeline ADC. This technique allows for large average amplitude dither injections without scarifying the signal amplitude, which means fast convergence speed while keeping the SNR not changed. For the dither-based calibrations [9] [15], the calibrations cannot proceed if the signal stays at high level all the time. This constrain limits the application. The introduction of domain-extended architecture allows the digital calibration to proceed even though the signal stays at high level all the time. Also, the redundancy space plus the total amplitude of the signal and the dither is limited by the quantify range. The domain-extended architecture extends the quantify range, which results in higher SNR, faster convergence speed, or more redundancy space for the comparator offsets to be corrected. The simulated ADC demonstrates good dynamic and static performance within a practical time without paying significant penalty in the circuit complexity.

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AUTHORS

Ting Li received the B.S. degree and the M.S. degree from China University of Mining of Technology, Beijing, China, in 2008 and 2010 respectively. Since August 2010, she has been with North Dakota State University (NDSU), Fargo, North Dakota, USA, where she is working toward the Ph.D. degree in electrical engineering. From August 2010 to present, she worked with NDSU as a Teaching Assistant. Her doctoral research focuses on accuracy enhancement techniques in pipeline analog-to-digital converter design. Her current research interest include analog/mixed-signal behavioral simulation and analog/mixed-signal integrated-circuit design.

Chao You received the B.S. degree from Nankai University in 1999. He received the M.S. degree and the Ph.D. degree from Rensselaer Polytechnic Institute, Troy, New York, USA, in 2003 and 2005, respectively. From August 2005 to 2011, he worked with NDSU as an Assistant Professor. From 2011 to present, he worked with NDSU as an Associate Professor. He is also a Visiting Professor in Nanchang University, Nanchang, Jiangxi, China. His research is very large scale integration.