COST EFFECTIVE TEST METHODOLOGY USING PMU FOR AUTOMATED TEST EQUIPMENT SYSTEMS

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ABSTRACT

In this paper, test methodology using parametric measurement unit is proposed for Automated Test Equipment (ATE) systems using 600MHz Driver, Comparator, and Active load (DCL). ATE systems is a very important means to reduce the device test cost, and the systems should be able to test several modes to check the performance characteristics of the device. The proposed methodology provides four different types of test operation for DC and AC analysis of the Device-Under-Test(DUT). Along with the proposed methodology, the paper proposes ATE system integration methodology for cost effective ATE integration for high speed test. The measured test results using the proposed method and system turned out to be well within the target specifications with high accuracies.

KEYWORDS

Automated Test Equipment, ATE, DCL, Pin Parametric Unit, Test Methodology

1. INTRODUCTION

Automatic test equipment (ATE) systems play a key role in the manufacture of semiconductor devices including BJT and CMOS devices. More commonly called “testers”, the equipment allows manufacturers to test each device for engineering characterization and/or production validation. It is critical to guarantee every chip’s correct operation with an acceptable performance in the field for the continued success of the semiconductor device manufacturer. Unfortunately, it is possible to guarantee the correct function with an acceptable performance only after a costly test. In general, the test cost increases with the complexity of the device-under-test (DUT). Cost of test is one of the most important factors in deciding the type of tester. That is one of the reasons why cost effective ATE systems should be developed [1].

Much of the cost of a semiconductor tester is wrapped into the channel architecture. A channel may be thought of as the electronic resources in the tester that interface with one pin of the device-under-test (DUT). If the DUT pins require high performance and high accuracy test signals in order to adequately test the part, each channel may require a host of costly enabling features to achieve the performance. On the other hand, a channel architecture may be greatly simplified, and less costly, if the performance parameters are low [2].

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DOI : 10.5121/vlsic.2014.5102

Typically, as shown in Figure 1, the conventional channel architecture for a semiconductor tester includes AC test circuitry in the form of an AC driver in response to a pattern generator and DC test circuitry including a DC parametric measurement unit. Generally, the AC driver generates and drives AC test waveforms along a transmission line to a DUT, while the DC test circuitry forces a DC voltage or current to the DUT and performs various DC measurements. Usually, AC and DC tests are performed on the tester at separate times. The AC driver circuitry couples to the DUT via the transmission line with a complementary comparator circuit. The comparator circuit captures signals from the DUT that are generated in response to the AC driver waveforms. The captured signals are then compared to the expected signals to determine if the DUT is functioning as expected. The DC test circuitry includes a separate circuit known as a Per-pin Parametric Unit (PPMU). In general, the PPMU provides a force/measurement functionality for DC voltage and current testing of the DUT. The PPMU is typically a low cost circuit [3]–[5] due to the inherent DC characteristics.

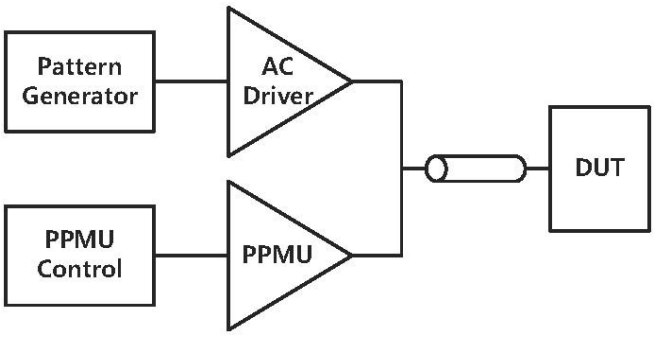

Figure 1. Conventional channel architecture for test equipment system

While this general architecture works well for the intended applications, the cost and size of the hardware to realize the separate AC and DC driver circuits is often prohibitive for very low-cost and low-performance testers. Therefore, it is necessary to develop a low-cost channel architecture for low-cost and low-performance testers. In [6], this paper proposes an integrated driver for AC driver and PPMU to address the cost issue and its architecture is shown in Figure 2.

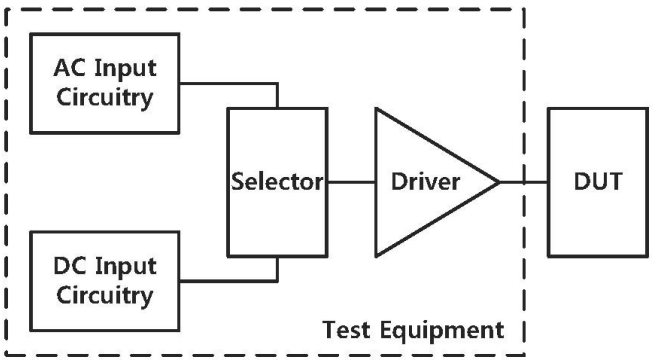

Figure 2. Test equipment system architecture having combined driver

In addition, the Driver, Comparator, Active Load (DCL) used to be discrete components in the past Automated Test Equipment (ATE) systems as shown in Figure 3. These discrete components were then assembled onto a circuit board referred to as the Pin Electronics (PE) board [7]. This approach was successful for many years. However, as IC processes became faster, interconnect capacitance and resistance on the PE board began to limit the accuracy of timing measurements

made by the comparator. Critical timing specifications such as rise and fall times and propagation delay were greatly affected due to the RC time constant of the board parasitics. To reduce the board parasitics, the Driver and Comparator were integrated onto the same IC. This was an acceptable solution for better performance for many years. However, the pressure to decrease the cost of the PE board motivated further integration. Overall, in order to support a variety of test mode and to integrate the circuit of ATE systems to decrease the cost, new test methodology using Parametric Measurement Unit (PMU) is required. This paper suggests a viable methodology along with a cost effective architecture of the PMU.

The remainder of this paper is organized as follows. Section 2 and Section 3 introduces modes of DC and AC operation of ATE systems for DUT, respectively. Section 4 explains the measurement of quiescent currents, and Section 5 describes the integration methodology of PMU followed by the conclusion in Section 6.

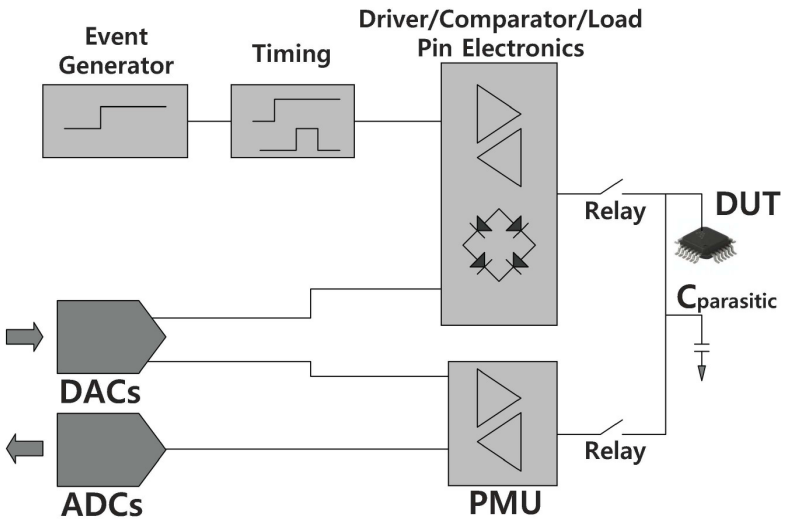

Figure 3. IC tester block diagram prior to PMU integration

2. DC OPERATION

The PMU in ATE systems should be able to supply high currents and voltages to charge capacitive loads and measure low currents and voltages, and the PMU can be controlled by the functional test pattern generator in the test system. Traditionally, there are four modes of operation for the test of DUT:

1) Force Voltage/Measure Current (FVMI)
2) Force Voltage/Measure Voltage (FVMV)
3) Force Current/Measure Voltage (FIMV)
4) Force Current/Measure Current (FIMI)

The PMU is capable of forcing and measuring positive and negative voltages and currents and it has all of the four modes in general.

The Force parameter is an input to the PMU which gets driven to the DUT and the Measure parameter is the output of the PMU as measured at the DUT. A typical application of the PMU in FVMI mode is to measure input bias current on a single DUT pin, where the PMU forces a

voltage onto the DUT pin and measures the corresponding current. A typical application of the PMU in FIMV mode is continuity testing of a DUT pin, where a current is forced into the pin that is being tested (while every other pin on the DUT is grounded) and the voltage at the pin is measured. Since all ICs have ESD protection, the measured voltage should be the diode drop of the corresponding ESD device.

It is useful for the PMU to have a wide dynamic range for a broad range of applications. Low current ranges are required when measuring leakage currents, and high current ranges are required for measuring low input resistances. Figure 4 shows a high level block diagram of a PMU architecture. The circuit consists of two operational amplifiers, an instrumentation amplifier, a variable sense resistor, and two sets of analog switches for selecting the force and measure parameters.

The most important DC specification is often the linearity of the forced and measured voltage and current. Therefore, this DC parameter is optimized in the design methodology that will be described in the rest of this paper. The only AC specification of importance is settling time as this determines how quickly the accurate DC measurements can be made. There is a fundamental trade-off between DC and AC performance in a PMU (or any other feedback system for that matter) such that higher DC accuracies require longer settling times. This is because higher accuracies require larger open loop gains of the op-amps which require more aggressive compensation to stabilize the loop. This additional compensation reduces the slew rate of the amplifiers which increases settling time. Therefore, a fundamental trade-off exists between DC linearity and AC settling time.

2.1. Measure Voltage

The design of the Measure Voltage function will be addressed first because it is the least complex mode of the PMU, and it is also part of the Force Voltage loop. It is desirable to have a higher degree of accuracy in Measure Voltage mode than in Force Voltage mode, as one would like to be able to accurately measure the voltage that they are forcing. The general specifications in Measure Voltage mode are listed in Table 1.

Table 1. Measure voltage specifications

Measure Voltage		
Specification	Target	Units
Output Range	± 5	V
Non-linearity	± 150	μV
CMRR	≥ 80	dB
PSRR	≥ 80	dB

In Measure Voltage mode the PMU acts as a voltage follower applying to the Measure Out pin as a buffered version of the DUT voltage. A diagram of the PMU in FIMV mode is shown in Figure 4. Measure Out and DUT are generally brought out as package pins, and V_{IN} can be generated by an on-chip Digital to Analog Converter (DAC) or be brought in by a package pin. In FIMV mode the Force I switch that connect InAmp with Force Amp is used to close the loop, and the Measure V switch is closed to select voltage as the measured parameter. In this example current range 1 is selected by closing the force and sense switches to the left of R_{S1}. Inspection of the feedback circuit yields the following expression for V_{MO}

$$V_{MO} = V_{DUT} \frac{a_2}{1 + a_2} \tag{1}$$

The linearity of the measured voltage V_{MO} is an important parameter as many testers only use a 2 point calibration algorithm to correct instrument errors. This allows the correction of any offset and first order gain errors of the PMU. Therefore, any higher order gain errors that the PMU introduces into the system will show up directly in the voltage measurement result. This non-linearity is caused by the change in the measure amps open loop gain as its output voltage is varied. This can be expressed quantitatively as [8]:

$$a_2(V_{MO}) = \begin{cases} a_{2m}\left[1-\left(\frac{V_{MO}}{V_{SAT}}\right)^2\right] & |V_{MO}| \le |V_{SAT}| \\ 0 & |V_{MO}| \ge |V_{SAT}| \end{cases}, \quad (2)$$

where V_{SAT} is the voltage at which the output of the measure amp saturates. For op amps designed to have a large input and output common mode range V_{SAT} is approximately 1.5V from the power supplies. From equation 2 it can be seen that as V_{MO} approaches V_{SAT} , a_2 approaches zero when $V_{MO} = 0$, a_2 is at its maximum value a_{2m}.

The open loop gain of an actual op-amp will become more non-linear than the model predicts as V_{MO} approaches V_{SAT}. However, if the circuit operates far enough away from this region, this equation will yield accurate results. To ensure this condition, this PMU uses ±8V power supplies for a ±5V output range. The minimum value of a_{2m} for a given Measure Voltage non-linearity can be determined by defining the overall circuit non-linearity as

$$INL_{V_{MO}} = V_{MO_{ideal}} - V_{MO_{model}} \quad (3)$$

where $V_{MOideal}$ assumes that a_2 is constant and equal to its maximum value a_{2m}. The modeled nonlinear measured voltage can be written by replacing a_2 in equation (1) with equation (2) for $|V_{MO}| \le |V_{SAT}|$ which gives

$$V_{MO_{model}} = V_{DUT}\frac{a_{2m}\left(1-\left(\frac{V_{MO}}{V_{SAT}}\right)^2\right)}{1+a_{2m}\left(1-\left(\frac{V_{MO}}{V_{SAT}}\right)^2\right)} \quad (4)$$

Substituting equation (4) into equation (7) and using the approximation of $V_{MO} \approx V_{DUT}$ gives

$$INL_{V_{MO}} = V_{DUT}\frac{a_{2m}\left(\frac{V_{DUT}}{V_{SAT}}\right)^2}{1+a_{2m}\left(2-\left(\frac{V_{DUT}}{V_{SAT}}\right)^2\right)+a_{2m}^2\left(1-\left(\frac{V_{DUT}}{V_{SAT}}\right)^2\right)} \quad (5)$$

This equation reaches its maximum value as V_{DUT} approaches V_{SAT}. Therefore, the maximum error will occur at the ends of the output voltage range. The minimum value of a_{2m} required for a given nonlinearity can be determined by rearranging equation (5) into polynomial form and solving for a_{2m}

$$0 = a_{2m}^2\left(\frac{INL_{V_{MO}}}{V_{DUT}}\left(1-\left(\frac{V_{DUT}}{V_{SAT}}\right)^2\right)\right)+a_{2m}\left(\frac{INL_{V_{MO}}}{V_{DUT}}\left(2-\left(\frac{V_{DUT}}{V_{SAT}}\right)^2\right)-\left(\frac{V_{DUT}}{V_{SAT}}\right)^2\right)+\frac{INL_{V_{MO}}}{V_{DUT}} \quad (6)$$

The minimum required value of a_{2m} for a specified INL, V_{SAT} and V_{DUT} can now be determined by solving the above equation for a_{2m}. Using a value of 5V for V_{DUT} and using $|V_{SAT}| = |V_{DD} - 1.5\text{V}| = |V_{SS} - 1.5\text{V}| = 6.5\text{V}$, an INL error of 150µV requires that $a_{2m} \geq 48.3kV/V$. Since the PMU cannot ascertain the difference between current from the DUT and input bias current of the Measure V amp, a CMOS input stage is used in the design of the Measure V amp. A two stage CMOS amplifier with a gain of 100kV/V is used to achieve sufficient margin. Figure 5 shows a plot of the simulated nonlinearity overlaid on the predicted non-linearity.

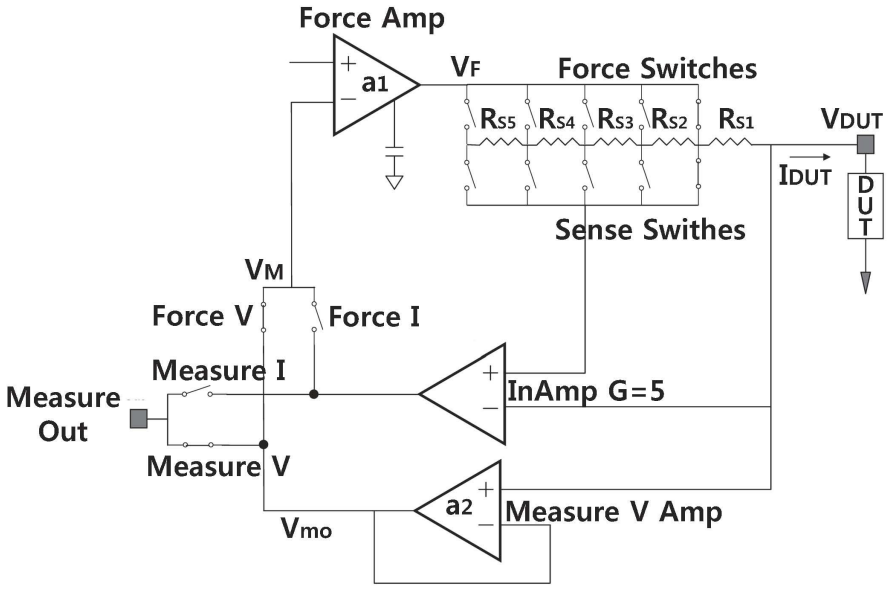

Figure 4. General PMU Block Diagram

2.2. Force Voltage

The function of the PMU in Force Voltage mode is to force an accurate voltage at the DUT pin. As in Measure Voltage mode, non-linearity, CMRR, and PSRR are the key DC parameters and the general specifications are listed in Table 2. In Force Voltage mode the PMU acts as a voltage follower applying to the DUT pin as a buffered version of the input voltage V_{IN}. A diagram of the PMU in Force Voltage mode is shown in Figure 4, where Force V switch is closed, Force I switch is opened, and Measure I & V switches are opened.

Table 2. Force Voltage DC specifications

Measure Voltage		
Specification	Target	Units
Output Range	± 5	V
Non-linearity	± 0.5	mV
CMRR	≥ 75	dB
PSRR	≥ 75	dB

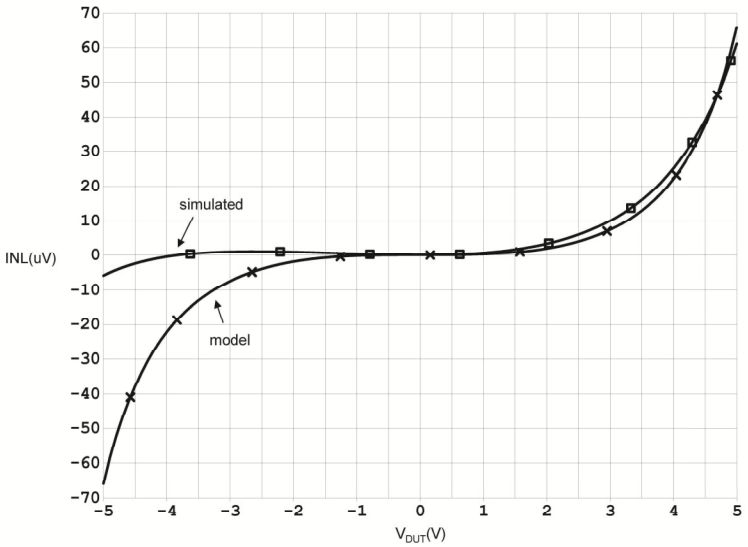

Figure 5. Simulated Amp and Model Non-linearity

The non-linearity in Force Voltage mode is due to the nonlinear gain of the force amp and measure amp with respect to their output voltages.

2.3. Measure Current

In Measure Current mode, the PMU can either force a voltage or current, and it can measure the resulting current. A typical application of FVMI mode is to measure the input bias current of a specific DUT pin, where the PMU forces a voltage to the DUT and measures the resulting current. Table 3 lists the targeted DC specifications in Measure Current mode. A diagram of the PMU in FVMI mode is shown in Figure 6.

Table 3. Measure current DC specifications

Measure Voltage		
Specification	Target	Units
Current Range 1	± 40	mA
Current Range 2	± 1	mA
Current Range 3	± 100	µA
Current Range 4	± 10	µA
Current Range 5	± 2	µA
Voltage Range	-5 to +5	V
Non-Linearity	± 0.001	%

2.4. Force Current

In Force Current mode, the Force V switch is open and the Force I switch is closed placing the InAmp inside the feedback path. Since the feedback is negative, the force amp will force the output of the InAmp to be approximately equal to the input voltage.

3. AC STABILIZATION

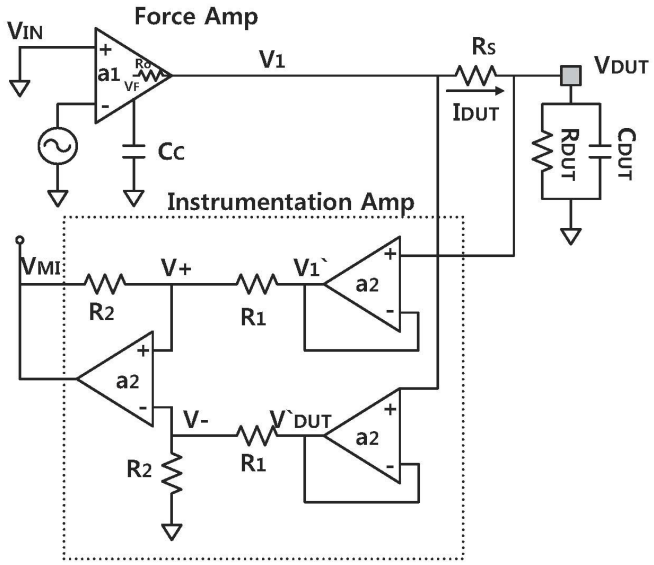

Figure 6. General PMU in FVMI mode

While the PMU is a DC measurement circuit, its output capacitance reduces the bandwidth of the test path. When the PMU is a separate IC from the Driver, Comparator and Load (DCL), a relay is used to isolate its capacitance from the test path and no care need be taken to minimize its output capacitance. The DCL specification, which is the most sensitive to the PMU's output capacitance, is the bandwidth of the comparators. The comparators are used to make 20/80 rise time measurement by setting the low threshold to the 20% value of the input signal, measuring the propagation delay, and then setting the high threshold to the 80% value of the input signal, and the measurement is repeated. The difference in the propagation delays is the rise time. Any rise time measurement will be affected by the rise time of the system used to measure the comparator. As shown in [9], assuming a Gaussian waveshape, a good approximation of the measured rise time is

$$t_{rise} = \sqrt{(t_{rise} measurement\ \ sys.)^2 + (t_{rise} signal)^2} \tag{7}$$

A measurement error of 5% is tolerable for most applications which gives

$$(1.05 t_{rise_{signal}})^2 = (t_{rise_{system}})^2 + (t_{rise_{signal}})^2 \tag{8}$$

Solving for $t_{rise_{system}}$ yields

$$t_{rise_{system}} = 0.32 t_{rise_{signal}} \tag{9}$$

Assuming a first order system, the 20/80 rise time of a signal and the bandwidth of that system are determined by the time constant of the system by the following relationships.

$$t_{20/80} = 1.4\tau \qquad (10)\,, \qquad f_{3dB} = \frac{1}{2\pi\tau} \qquad (11)$$

Solving for _ in equation (10) and substituting this into equation (11) gives

$$t_{20/80} = \frac{0.22}{f_{3dB}} \tag{12}$$

where f_{3dB} is the 3dB roll off of the system. Substituting equation (12) into equation (9) produces

$$f_{3dB}system = 3.12 * f_{3dB}signal \tag{13}$$

This implies that the bandwidth of the measurement system must be at least three times the bandwidth of the signal being measured to preserve a 5% tolerance on the measured rise and fall times. Since the comparator is expected to measure rise times of signals having a 600MHz bandwidth, its bandwidth must be 1.87GHz. The maximum allowable output capacitance of the PMU can now be obtained by observing Figure 7 and noting that the 3dB roll off of the system is determined by the time constant created by the total impedance seen by the input of the comparator (neglecting inductance).

$$f_{3dB}system = \frac{1}{2\pi R_{OUT} C_{OUT}} \tag{14}$$

where $C_{OUT} = C_{driver} + C_{load} + C_{PMU} + C_{comph} + C_{compl}$ and $R_{OUT} = 50\Omega \square 50\Omega = 25\Omega$.

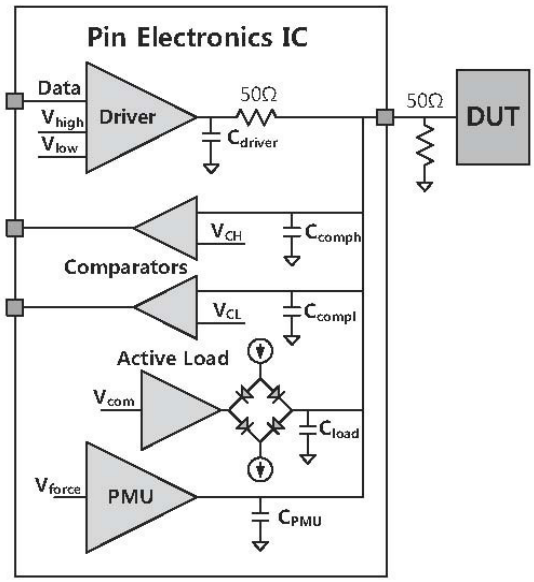

Figure 7. DCL bandwidth diagram

3.1. Measure Voltage

In Measure Voltage mode, the PMU can either force a current and measure the resulting voltage or force a voltage and measure the resulting voltage. The settling time in these modes will be dominated by the force loop due to the large capacitances that need to be driven at the DUT pin. Therefore, it is sufficient to merely stabilize the Measure Voltage loop without concerning its settling times. However, it is possible to have the PMU measure the voltage at the DUT pin while not forcing anything. This mode will be referred to as Force Nothing Measure Voltage (FNMV)

and a settling time of 1 μs will be targeted for this mode. A system will be stable if its phase is less than -180º when the magnitude of its loop gain $|T(s)|$ is unity and the difference between its phase and -180º is known as the phase margin, and it is expressed quantitatively as following.

$$PM = 180^{\circ} + \angle(|T(s)| = 1) \tag{15}$$

A circuit with 0_ phase margin will have an undamped response and will never settle to within 1% of its final value. As will be seen in Section 3.2, it is advantageous to have the measure amplifier approach a first order system, which will have a minimum phase margin of 90º. Gain margin is also a requirement for stability, and the gain margin of a system is defined as the gain of the system when the phase of the system is 180º. This can be expressed quantitatively as

$$GM = 0 - |T(s)|, \angle(|T(s)| = -180) \tag{16}$$

3.2. Force Voltage

In Force Voltage mode, the PMU will have to drive capacitive loads of up to 2nF making it much more difficult to stabilize than the Measure Voltage loop. Figure 8 shows a diagram of the circuit that will be used for stability analysis. Since the force amp will have to drive large capacitive loads, its open loop output resistance R_o must be taken into account. This is especially true in the higher current ranges as it appears in series with R_s.

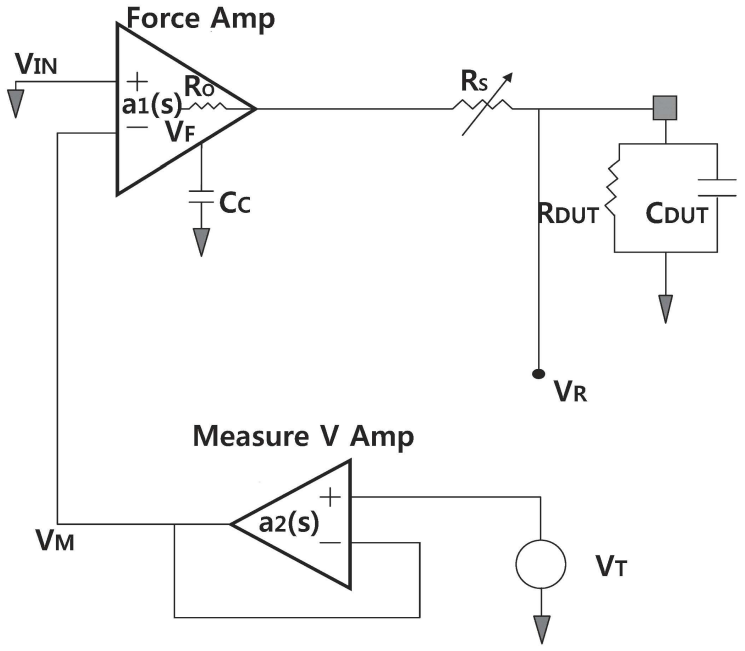

Figure 7. Force Voltage Loop Analysis

3.3. Measure Current

The settling time in measure current mode will be determined by either the time constant associated with R_s and C_{ff} expressed as $\tau = R_s C_{ff}$ or the slew rate of the force amp. This is due to the fact that the force amp output must rise or fall to accommodate the change in voltage across

the sense resistor. If $4.6\tau > \frac{\Delta V_{MI}}{SR_{force\ amp}} \frac{R_1}{R_2}$, then the settling time will always be determined by τ and the measure current output will settle to within 1% of its final value in 4.6τ .

3.4. Force Current

The PMU's stability in Force Current mode can be determined by analyzing Figure 6, where the loop is broken at the output of the instrumentation amplifier. Capacitor C_{ff} has been removed as it is not known whether it is necessary in Force Current operation.

3. MEASUREMENT OF QUIESCENT CURRENTS

In testing CMOS devices, the measurement of quiescent currents presents several problems. One problem is the length of test time required to measure the quiescent current (I_{DDQ}) of the power pin (VDD) for all the logic states of the CMOS device. Another problem is the long settling time associated with charging bypass-capacitance when low current ranges are used to measure leakage currents at the inputs of device under test (DUT) [10].

The IDD quiescent current (I_{DDQ}) of CMOS devices is measured at different logic states to determine if internal gates of the DUT have excessive leakage. Burn-in data has shown that gates with excessive leakage indicate potential reliability problems. I_{DDQ} measurements are used to detect CMOS devices that will have premature failures.

A CMOS DUT requires a high current (1mA to lA) during transients between logic states, but the CMOS device only requires a low current (10μA to l00μA) in a static or quiescent condition. A by-pass capacitor is also required to hold the VDD voltage stable during the high current transients between logic states.

To measure the I_{DDQ} of a DUT, the device power supply (DPS) must be capable of rapidly switching from a high current range to a low current range and measure to 1% accuracy. Conventional DPS's take from 5ms to 100ms depending on the by-pass capacitor selected. Conventional methods of switching the current ranges open or disrupt the voltage and/or current feedback of the DPS. This affects the output voltage of the DPS, which is also the voltage across the by-pass capacitor. The low current range resistor then has to charge the by-pass capacitor back to the programmed voltage. This causes a large time constant due to the current range selected charging the bypass capacitor. To eliminate this long time constant, a method of switching the current ranges without affecting the output voltage of the DPS is necessary.

Prior methods do not allow the functional test generator to directly control the timing of the current range switching or analog to digital conversion or comparison triggering. Conventional methods use driver and receiver test patterns to control the I_{DDQ} measurements. Special functional test patterns must be written when using a driver and receiver test patterns for I_{DDQ} current range switching measurement timing. To eliminate 65 special test patterns for I_{DDQ} measurement, the I_{DDQ} measurements must be supported by the functional test subsystem.

4. INTEGRATION METHODOLOGY

When the PMU is a separate IC from the Driver, Comparator, and Active Load (DCL), its output capacitance is isolated from the test path by a mechanical relay as shown in Figure 3.

In order to integrate the PMU onto the same IC as the DCL, its output capacitance must be minimized. In order to determine the maximum capacitance of the SF1 switch, the total

capacitance of the system must be determined. The total output capacitance of the PMU can be obtained by summing all of the individual capacitances of the devices tied to the DUT pin as shown in Figure 4.

$$C_{OUT} = C_{S_{ff}} + C_{sw} + C_{IA} + C_{MA} \tag{17}$$

where

$$C_{sw} = C_{eff_{S_{f1}}} + C_{eff_{S_{s1}}} + C_{eff_{S_{f2}}} + C_{eff_{S_{s2}}} + C_{eff_{S_{f3}}} + C_{eff_{S_{s3}}} + C_{eff_{S_{f4}}} + C_{eff_{S_{s4}}} + C_{eff_{S_{f5}}} + C_{eff_{S_{s5}}} \tag{18}$$

where C_{eff*} is the effective capacitance of each switch.

5. CONCLUSION

The methodology using PMU for ATE systems is presented. For reasonable automated test systems, the PMU should be an integral part of many ATE systems. Generally, four mode (FVMI, FVMV, FIMV and FIMI) are needed for ATE systems. Each mode can be explained as DC and AC analysis. As in any closed loop system, there is a trade-off between DC accuracy and settling times for AC analysis. This is because more accurate DC measurements require larger open loop gains, which in turn requires more compensation to stabilize the system. In addition, the measurement of quiescent currents is also important factor for ATE systems. For all of the necessary function, using PMU is an excellent way and inescapable solution. In order to use effective PMU with fast operation, total output capacitance should be considered. By considering the output capacitance, PMU can be integrated as one-chip with DCL for low cost. This paper proposes cost effective ATE integration methodology for high speed test, and this paper will be a good reference for future pin-electronics.

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