

BACKTRACK INPUT VECTOR ALGORITHM FOR LEAKAGE REDUCTION IN CMOS VLSI DIGITAL CIRCUIT DESIGN

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ABSTRACT

A new algorithm based on Input Vector Control (IVC) technique is proposed, which shifts logic gate of a circuit to its minimum leakage state, when device goes into its idle state. Leakage current in CMOS VLSI circuit has become a major constrain in a battery operated device for technology node below 90nm, as it drains the battery even when a circuit is in standby mode. Major concern is the leakage even in run time condition, here aim is to focus on run time leakage reduction technique of integrated Circuit. It is inherited by stacking effect when the series transistors are maximized in OFF state condition. This method is independent of process technology and does not require any additional power supply. This paper gives an optimized solution of input pattern determination of some small circuit to find minimum leakage vector considering promising and non-promising node which helps to reduce the time complexity of the algorithm. Proposed algorithm is simulated using HSPICE simulator for 2 input NAND gate and different standard logic cells and achieved 94.2% and 54.59 % average leakage power reduction for 2 input NAND cell and different logics respectively.

KEYWORDS

Active mode Leakage reduction, Standby mode, Minimum Leakage vector (MLV), Transistor Stacking

1. INTRODUCTION

As the world uses more and more mobile electronic products, controlling power consumption is the primary limiter of scaling semiconductor process technologies and adding features to integrated circuits. This power consumption is divided between active power ($P_{\text{active}} \sim CV^2f$), which is the power used while the product is performing its various functions, and leakage power ($P_{\text{leakage}} \sim IV$), which is the power consumed by unintended leakage that does not contribute to the IC's function.

Leakage power [1] has become a top concern for IC designers in deep submicron process technology nodes (65nm and below) because it has increased to 30-50% of the total IC power consumption. In addition, the leakage problem is worse than generally thought because the simple, traditional leakage power estimation of multiplying the average transistor leakage by the transistor width of the entire IC grossly underestimates the actual product leakage.

Leakage power is primarily the result of unwanted subthreshold current in the transistor channel when the transistor is turned off. This subthreshold-driven leakage power is strongly influenced by variations in the transistor threshold voltage V_T (the voltage applied to the gate electrode that

turns on the transistor). As technology and supply voltage scales down continuously it increases the leakage power dissipation of the logic circuit. Reduction in threshold voltage, channel length, and thickness of the gate oxide layer leads to an exponential increase in the leakage current. Leakage is an amalgamation of several current – subthreshold leakages, gate oxide leakage, and band-to-band tunneling leakage. It is a significant problem in portable battery-operated devices such as laptops, mobile phones, and other electronic gadgets etc. Primary goal is to avert battery life during standby mode of all portable logic devices. Standby mode is the mode in which no operation is performed by a device. In CMOS VLSI circuit design it is projected that subthreshold leakage can contribute as much as 42% of the total power in the 90nm process technology [21]. Several circuit-level techniques have been projected to minimize leakage power dissipation. Dual threshold voltage (DVT) [16] process uses devices with higher threshold voltage along non-critical paths only, which reduces the leakage during standby mode of devices. Multiple threshold CMOS (MTCMOS) [14], [13] uses a higher threshold voltage transistor in series with the low threshold voltage logic circuitry. This technique requires a sleep transistor with high threshold voltage [13]. All the above techniques are process technology dependent. Another drawback is area increase due to the use of a sleep transistor with the original circuit and the need to design a controller circuit which operates this kind of sleep transistor input signal. There is another option to choose such a technique which is independent of process technology variation. For this case one very well-known and effective technique known as IVC [3], [4], [5] is used during runtime of the device. It utilizes the stacking effect of the circuit where more off-transistors in series reduce the leakage. In logic circuit leakage is directly related to the input of the gate. It means among all possible combinations some input values give less leakage than others. Evaluation of such an algorithm is done here which finds the minimum leakage vector to reduce leakage power in standby mode.

2. MOTIVATION

As technology scales down, leakage power becomes the most dominating factor of total power. Table 1 shows the leakage and static power dissipation of a NAND2. Data obtained by simulation in Synopsys HSPICE using the 0.18µm TSMC model at 1.8V.

Table 1. Leakage power of NAND cell with all input patterns

Input	Leakage Power(W)	Leakage current (A)
00	2.42E-12	3.93E-12 [MLV]
01	2.61E-11	Worst : 1.81E-11
10	2.15E-11	1.41E-11
11	3.09E-11	2.44E-11 [WLS]

As can be seen from Table 1, shifting a logic gate to its minimum leakage vector (00 as in the case of NAND2 logic gate) can decrease leakage by about 6.2 times of the Worst leakage vector (WLS) (i.e. 11 as in the case of NAND2 logic gate) [2]. Actually every other logic gate input is dependent on the output of the gate either directly or indirectly followed to that gate. So, the leakage power and leakage current of the given logic circuit can be reduced without change in any process technology. It is concluded that an algorithm is required, able to find a vector that gives minimum leakage at a particular input vector as compared to all of its possible input combinations.

3. PREVIOUS WORK

Several techniques were proposed to get minimum leakage input vectors; the most of these are based on heuristics, so their results are not optimal. In [11], an Integer Linear Programming (ILP) is presented to compute an input vector that can be applied to the primary inputs of the circuit in standby mode in order to minimize leakage power. An appropriate linear relaxation to provide a lower bound on the integer optimum and then employ a technique called randomized rounding to round the solution to the linear relaxation, which is typically fractional, to an integer solution. The problem is formulated as ILP in two different ways. One scheme consists of relaxing the ILP formulation to obtain a lower bound on the minimum leakage power that is dissipated by the circuit. The linear relaxation of the first ILP formulation is shown theoretically to be of poor quality, while the relaxation to the second ILP formulation is shown to work much better in practice. ILP is not optimal and needs large runtime.

In [8], a random method based on heuristic to find the MLV is developed. The idea is to choose an independent vector randomly. This paper targets design where parts of the circuit are put in standby mode when not in use, which is becoming a common approach for low power design. Here a novel method is proposed that can be used during logic design to reduce the leakage power of CMOS circuits that use clock gating to reduce the dynamic power dissipation. Using minimal additional circuitry, it modifies the original logic design to force the combinational logic into a low leakage state during an idle period. To find such a low leakage state, they have developed an efficient algorithm that determines a good input vector using a sampling of random vectors. The size of sampling is determined a priori user-supplied quality measures. They have demonstrated this method on the ISCAS-89 benchmark circuits and shown leakage power reduction of up to 54%. This algorithm is poor and not optimal.

In [9], a genetic algorithm was recommended to overawe the problem of MLV Genetic algorithm has an exponential solution space concerning the number of primary inputs. In this algorithm, the chromosomes are represented by the input vectors, and calculation process of the circuit leakage current represents the fitness function. The algorithm selects the parents randomly to make crossover between them to produce the new children. At the end of the method, the parent with the least leakage current is chosen as the best vector. In general, Genetic Algorithm applications are not optimal and need exponential space complexity and large runtime.

In [12] a fast algorithm is proposed having the same concept of controllability, which is widely used for fault tolerance detection. In this algorithm, the controllability of each gate in the circuit is calculated. The algorithm eliminates the least cost nodes. The final situation is achieved by eliminating all the nodes in the list. The simulation results showed that the results vectors are among 5% of the best vector obtained from 100,000 random vectors, but it requires a large run time.

In [10], Presents graph based algorithms for estimating the maximum leakage power. These algorithm are pattern-independent and do not require simulation of the circuit. Instead the circuit structure and the logic functionality of the component in the circuit are used to create a constraint graph. The problem of estimating the maximum leakage power is then transformed to an optimization problem on the constraints graph. Efficient algorithms on the graph are used to estimate the maximum leakage power dissipated by a circuit comparison with exhaustive/long simulations for MCNC/ISCAS-85 benchmark circuit is presented to verify the accuracy of the method.

The work done till now is based mostly on heuristic approach [20], [7], [11], [17], [18], [19] and have large time complexity. So in next section we have proposed algorithm which is based on exact approach and is less time complex.

4. PROPOSED ALGORITHM

To achieve the maximum reduction of leakage power (essentially sub threshold and gate oxide leakage) for CMOS circuit in the idle state, the proposed algorithm combines the advantages of Input Vector Control algorithms and back track method.

Firstly it transforms the logic circuit into a graph and then uses Boolean logic and probability to discover least Sub-threshold leakage vector.

The Algorithm read the netlist, prepare the graph by representing transistors as nodes and the nets (interconnection) as edges of the graph. Figure1 shows the Graphical representation for NAND cell. In this graph a, b are the inputs and y is the output of NAND cell. VDD and GND represent the power supply and ground nodes.

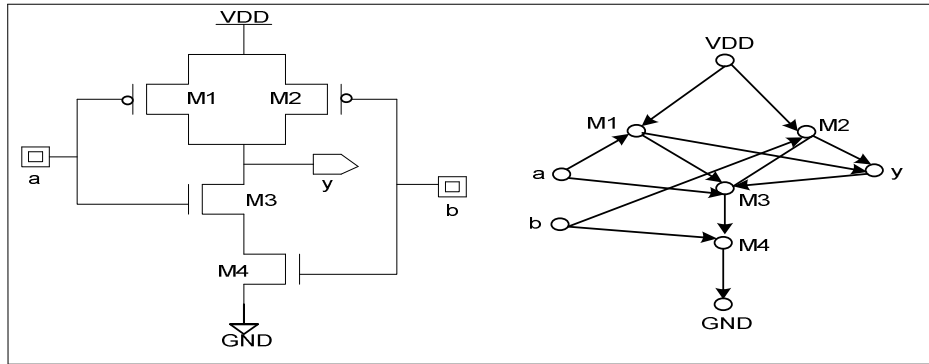


Figure1. Graphical representation of NAND cell

The algorithm runs on 2 principles (a) transistors is in OFF state and (b) The OFF transistor's drain to source terminal potential difference (i.e. V_{DS}) should be equal to the supply voltage (i.e. VDD). Above condition checks for every path of the graph and result is the sum of the entire OFF transistor in every path of the graph for a specific input combination. And the input vector which gives least leakage power sets as MLV of the given logic cell.

In the algorithm the NOTFV [N] array keeps the number of OFF transistor at a given input vector at a specific input combination. A function NOTF is called to find OFF state transistor in a graph. TleakV refers Transistor LEAKage Vector which gives the name of the transistor is in OFF state. In this algorithm OFF state transistor considered as a promising node and transistor is in ON state is non-promising. If two consecutive promising nodes in a single path are achieved, it back tracks the path and traverse to the next path for the same. Finally TleakV stores the total number of OFF transistors at a specific input pattern. It is a recursive process to check input until every combination of input is complete.

Pseudo code for the proposed algorithm:

1. Push the starting node (VDD). Set NOTFV [N] = 0; Temp = 0;
2. Repeat (3) and (4) until stack is not empty.

```

3. Process top node of stack N and
   Set Temp = NOTFV [N]
   Temp = NOTF [N] // CALL A FUNCTION
4. IF N = GND && NOTF [N] = 1
   Print last element TleakV [ ] AND RESET i = 0;
   POP the Stack and Go to Step 2
   Else IF NOTF [N] >1 then i--
   POP the stack Go to Step 2;
   Else
   POP stack
   Push on to stack all the neighbor of N
   SET NOTF [N] = Temp, for every neighbor go to Step 3
5. Exit

```

```

NOTF [N] //Called a Function to find OFF transistor
{
  If ((N == PMOS) && (INPUT == 1)) //OFF condition for PMOS
  {
    NOTFV [N] ==Temp + 1;
    TleakV[i] == N;
    i++;
    Return (NOTFV [N]);
  }
  ELSE If ((N == NMOS) && (INPUT == 0)) //OFF condition for NMOS
  {
    NOTFV [N] ==Temp + 1;
    TleakV[i] == N;
    i++;
    Return (NOTFV [N]);
  }
  ELSE
  {
    NOTFV [N] ==Temp; //When VDD or GND comes
    Return (NOTF [N]);
  }
}

```

5. SIMULATION RESULT

The proposed algorithm is simulated on HSPICE simulator by Synopsys for two inputs NAND cell and various cells also. A detailed simulation for the entire vector to get the minimum and maximum leakage input vector. This method is based on exact simulation of logic circuit TSMC 0.18um model library for NAND cell and BPTM model library for all different cells. It is found that the leakage behaviour of a circuit in different technologies (i.e. 180 130, 90, 65, 45 nanometre) model with all its input combinations is identical. The NAND logic output waveform is shown in Figure2. Leakage power for all combinations of inputs is shown in figure 3. Here the proposed algorithm identifies the condition of WLS vector as [11, 01] and MLV as [00] for NAND cell. Figure 4 gives the comparison of different logics on the basis of their power dissipation at WLS vector and MLV. Figure 5 results the number of OFF transistor found in their WLS vector and MLV. Figure 6, 7 both gives the leakage reduction percentage through this algorithm for NAND cell and Different logics respectively on the basis of leakage power in WLS vector and MLV.

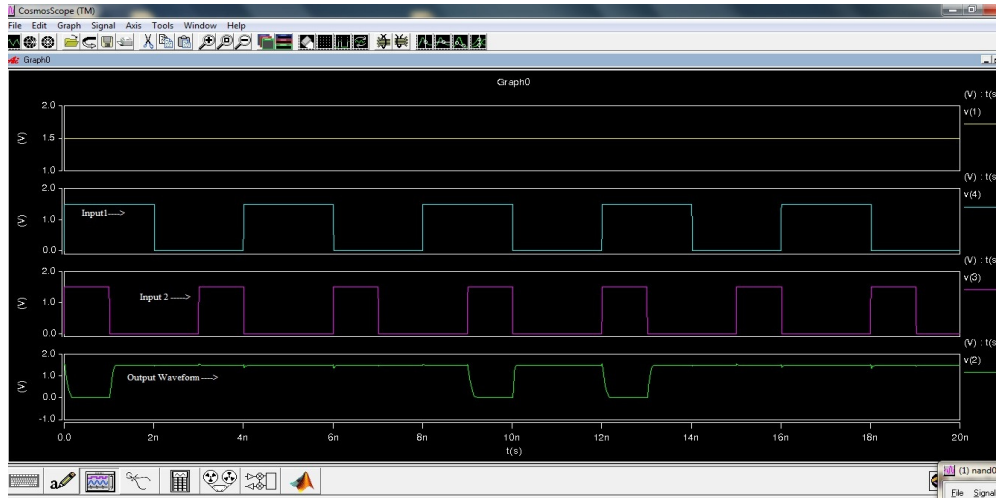


Figure 2. NAND logic waveform

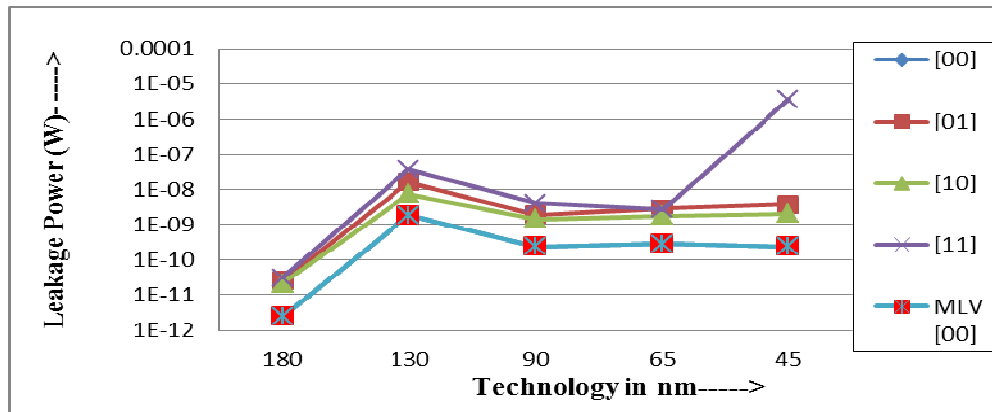


Figure 3. Leakage reduction in NAND2 cell by proposed algorithm

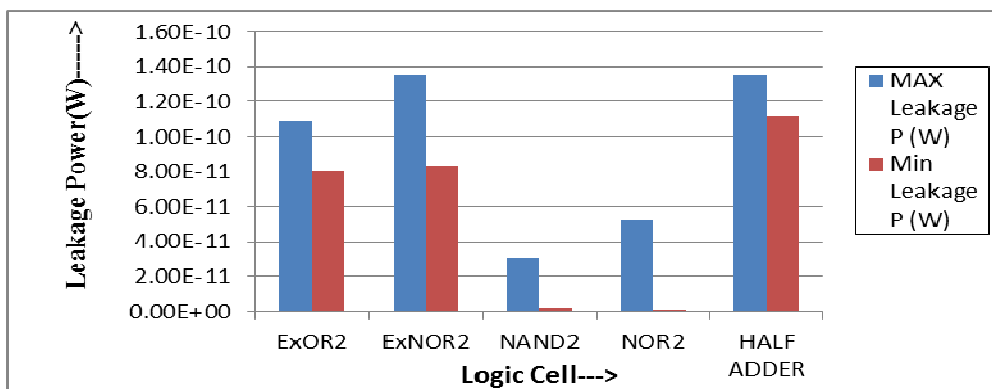


Figure 4. Comparison of leakage power with logics (NAND2, NOR2, EX-OR2, EX-NOR2, HALF ADDER)

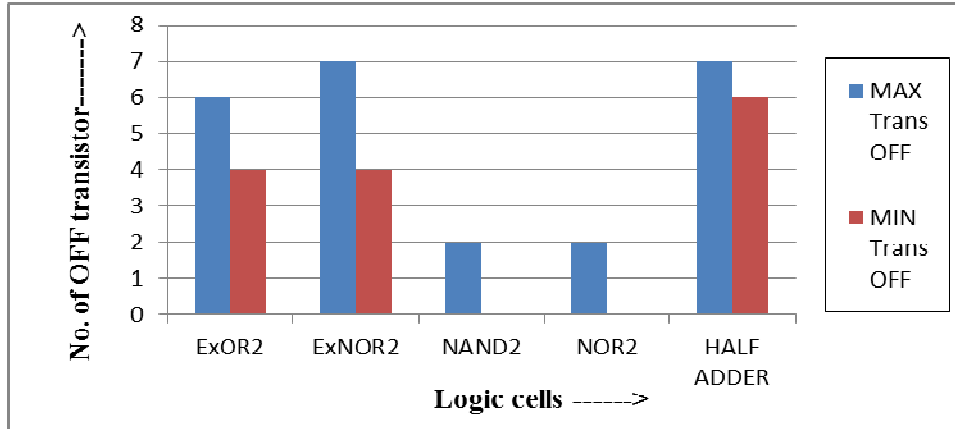


Figure 5. Comparison of OFF transistor in WLS and MLV by proposed algorithm with logics (NAND2, NOR2, EX-OR2, EX-NOR2, and HALF ADDER)

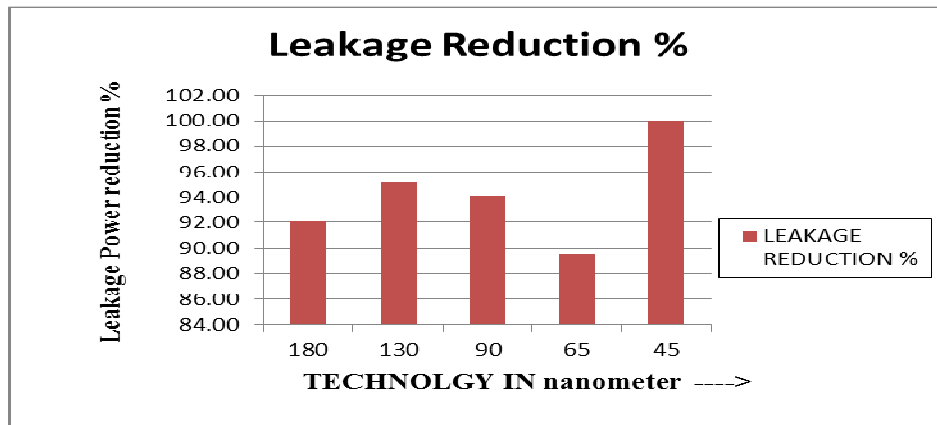


Figure 6. Leakage power reduction of NAND2 cell with different technology

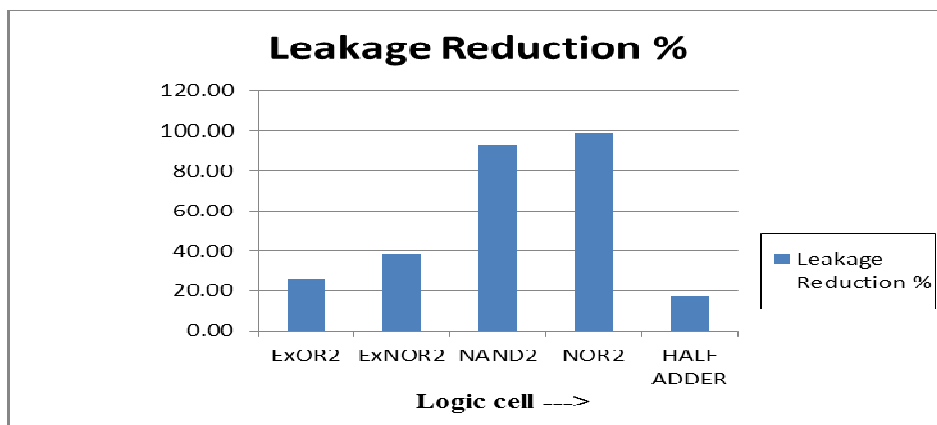


Figure 7. Leakage power reduction of various cells

6. CONCLUSIONS

The proposed Back track input vector algorithm is an efficient solution for finding MLV to minimize the leakage power of the given logic circuit. Leakage power reduction is achieved on logic circuits without any process technology modification. The time complexity of this algorithm is less due to use of promising and non-promising node conditions. It minimizes leakage power up to 94.2% at [00], 99.75% at [11], 26.03% at [00], 38.50% at [00, 11], and 17.6 % at [00, 11] for NAND2, NOR2, EXOR2, EXNOR2, and HALF ADDER respectively. Concluding this average leakage power reduction of 54.59 % is achieved for all logics which are quite significant for practical purposes. All the above mentioned logics are verified on HSPICE simulator.

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