A NOVEL APPROACH FOR LEAKAGE POWER REDUCTION TECHNIQUES IN 65NM TECHNOLOGIES

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ABSTRACT

The rapid progress in semiconductor technology have led the feature sizes of transistor to be shrunk there by evolution of Deep Sub-Micron (DSM) technology; there by the extremely complex functionality is enabled to be integrated on a single chip. In the growing market of mobile hand-held devices used all over the world today, the battery-powered electronic system forms the backbone. To maximize the battery life, the tremendous computational capacity of portable devices such as notebook computers, personal communication devices (mobile phones, pocket PCs, PDAs), hearing aids and implantable pacemakers has to be realized with very low power requirements. Leakage power consumption is one of the major technical problem in DSM in CMOS circuit design. A comprehensive study and analysis of various leakage power minimization techniques have been presented in this paper a novel Leakage reduction technique is developed in Cadence virtuoso in 65nm regim with the combination of stack with sleepy keeper approach with Low V_{th} & High V_{th} which reduces the Average Power with respect Basic Nand Gate 29.43%, 39.88%, Force Stack 56.98, 63.01%, sleep transistor with Low Vth & High Vth 13.90, 26.61% & 33.03%, 75.24% with respect to sleepy Keeper 93.70, 56.01% of Average Power is saved.

KEYWORDS

Leakage Power, High V_{th}, Low V_{th}, sleep transistor, Transistor stacking.

1. INTRODUCTION

Leakage power consumption is an important issue in DSM CMOS VLSI circuit. The main contribution of Power dissipation in CMOS circuit increases with the reduction of channel length, threshold voltage and gate oxide thickness.

The power dissipation of a logic gate is given by

$$P_{avg\ /gate} = P_{switching} + P_{short\ circuit} + P_{leakage} \qquad 1.1$$

Where $P_{switching}$ is the power dissipated due to charging and discharging of the circuit capacitances, P_{short} circuit is the power dissipated due to the short circuit between V_{dd} and ground during output transitions and $P_{leakage}$ is the power dissipated due to leakage current. The term, $P_{leakage}$, is dramatically increased with technology down scaling and increase in temperature, resulting in a reduction of leakage [2] immunity and robustness. Therefore, it is very vital to reduce the leakage power of dynamic logic gates.

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The organization of the paper is as follows: The section II, describes previous work which consist various types of leakage current and techniques to reduce the leakage current. Section III, presents the proposed sleepy keeper with stacking of the transistor with High V_{th} & Low V_{th} transistor using Cadence virtuoso EDA. Section IV presents simulation result using Cadence EDA. Finally the conclusion is presented in section V.

Table.I. Parameter values in 65nm Technology

Parameters	65nm	
Threshold voltage (V_{th0})	**-0.378**	PMOS
	0.429	NMOS
Channel doping concentration (NDEP)	**1.97e+18**	PMOS
	2.6e+18	NMOS
Low field mobility(μ_0)	**0.00548**	PMOS
	0.04861	NMOS
Source-drain junction depth (Xj)	**1.96e-08**	PMOS
	1.96e-08	NMOS
Electrical oxide thickness (t_{oxe})	**1.95e-09**	PMOS
	1.85e-09	NMOS
Physical oxide thickness (t_{oxp})	**1.2e-09**	PMOS
	1.2e-09	NMOS

2. PREVIOUS WORK

There are various types of Leakage current present in CMOS devices as we scale down the channel length some of the Leakage current present in CMOS are[5]

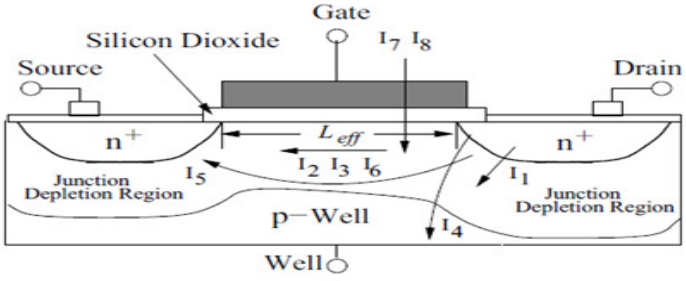

Fig.1. Leakage Mechanism in Short-Channel NMOS Transistor

I1= Reverse-bias p-n junction diode leakage current

I2 = Band-to-band tunneling current

I3 = Subthreshold leakage current

I4 = Gate Oxide tunneling current

I5 = Hot-carrier injection

I6 = Channel punch-through

I7 =Gate induced drain-leakage current

2.1 Leakage Power Reduction Technique

A. Sleep Mode Approach

Sleep approach is used for reduction of gate oxide and sub threshold leakage current in DSM technology[6]. Sleep approach is used to rail off the circuit from V_{dd} to ground, so we insert a PMOS transistor above pull up network and V_{dd} and NMOS transistor below pull down Network and GND[2]. During standby mode a sleep transistor turns off turn off and rail from V_{dd} and reduces the leakage current[3]. During active mode we ON the sleep transistor and direct connection of circuit with V_{dd}, so increase the performance of the circuit and Reduces the leakage power efficiently[2,9].

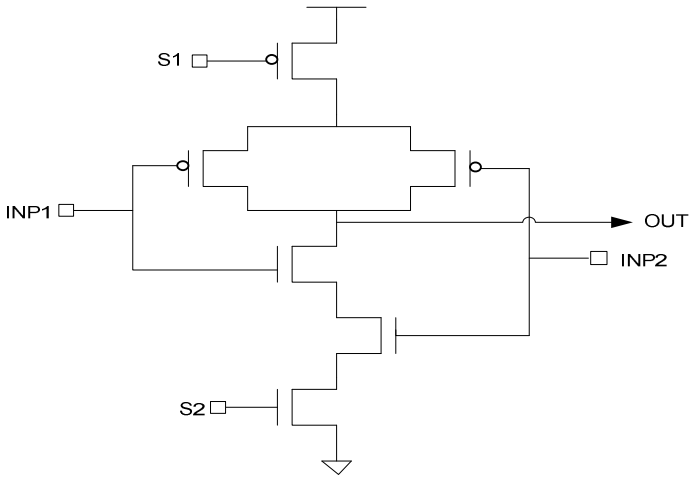

Fig.2. Sleep Approach NAND gate

B. Stack Approach

Force stack is another approach for further leakage reduction, in this approach we provide the stacking of the transistor, we divide pull up and pull down network into two half size[4].The dividing of the transistor will not affect the W/L ratio of the circuit, The W/L ratio of the circuit is maintained after dividing of the circuit[5]. For better Leakage saving we divide pull up PMOS network which provide the stacking of the transistor, same process of dividing is also done in pull down network serially as shown in Fig.3. . Hence suppression of sub threshold leakage current

and DIBL leakage and enhance the performance of the circuit by applying this approach in various circuit implementation[3-5].

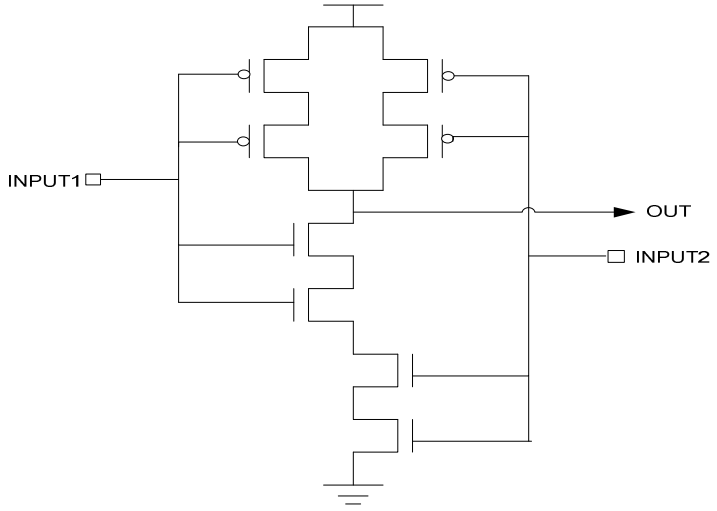

Fig.3. Stack Approach based 2 input NAND gate

C. Leakage Feedback Approach

Another Leakage reduction technique is leakage feedback approach; In this approach we use two parallel PMOS transistor above pull up network and V_{dd} [5-6]. To provide the inverting output of the circuit we connect inverter at the output, an inverter provides the proper logic feedback to both pull down NMOS(S') and pull up PMOS(S) sleep transistor as shown in Fig.4. This two transistor enhance the circuit performance and maintain the proper logic of the circuit during standby mode. In standby mode one of the transistor of parallel sleep transistor turn off both NMOS and PMOS, the output of the circuit is pass through inverter which keep ON one of the sleep transistor which is connected parallel by providing the proper feedback approach. Hence circuit is active in standby mode, we mitigate the various leakage current which flow during standby mode and increase the performance of the circuit.

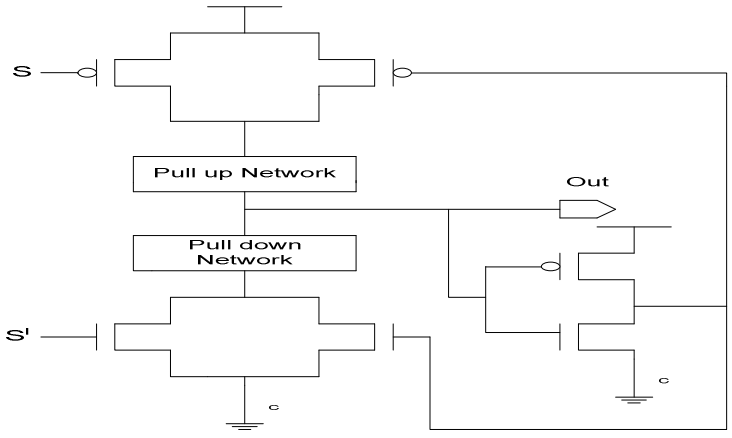

Fig.4. Leakage Feedback Approach

D. Sleepy Stack Approach

Combination of sleep transistor approach in active mode and stack approach in sleep mode forms a new leakage reduction approach is known as sleepy stack technique. The structure of sleepy stack technique is shown in fig.5. In this approach we divide the PMOS and NMOS sleep transistor with same width, into two half size of original single transistor, we add sleep transistor parallel to the two stack transistor of pull up and pull down network[5]. The stacking of the transistor reduces the leakage current during standby mode, Parallel connection sleep transistor turn ON by providing feedback approach during active mode S=0, S'=1, all the PMOS and NMOS sleep transistor turn ON, hence resistance of the circuit mitigate[6]. In sleep mode S=1, S'=0 both the PMOS and NMOS sleep transistor turn off, In stand by approach we suppress leakage current and maintain exact logic of the circuit with the combination of both the approach. We create ultra-low leakage power consumption during stand standby mode and increase the performance of the circuit by maintaining exact logic, with price of increasing area[4].

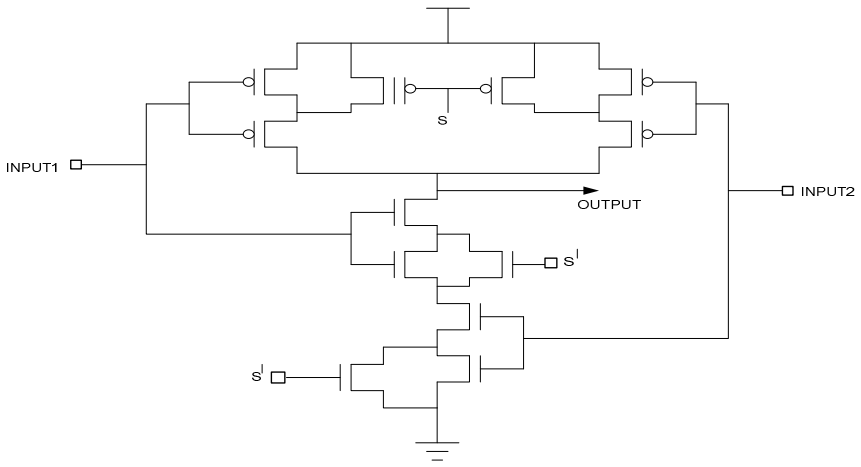

Fig.5. Sleepy Stack Approach based 2 input NAND gate

E. Sleepy Keeper Approach

Above all this approach the most efficient approach for leakage power reduction is the sleepy keeper approach. In this approach combination of PMOS and NMOS transistor which is connected paralleled inserted between pull up network and V_{dd} and pull down and GND, NMOS transistor of pull up sleep transistor connected PMOS pull down sleep transistor. As NMOS sleep transistor which rail off the path from V_{dd} to GND is connected to GND and PMOS transistor which is connected to V_{dd}, NMOS transistor is not turn ON that's why it will not efficiently pass V_{dd}, this problem can be overcome by maintaining output value "1" in sleep mode by connecting NMOS to V_{dd}. PMOS transistor which is connected to the pull up NMOS transistor and GND which is parallel to NMOS sleep transistor, to maintain output value equal to "0" in sleep mode. This approach reduces the leakage power efficiently and maintains the proper logic of the circuit with lesser area.

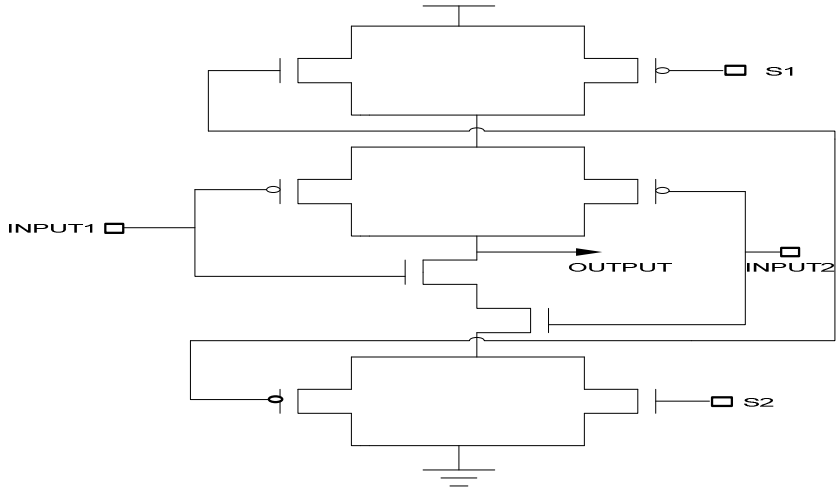

Fig.6. Sleepy keeper Approach based 2 input NAND gate

3. PROPOSED TECHNIQUE - Modified Sleepy Keeper with Stacking of the Transistor with High V_{th} & Low V_{th} Transistor.

In this section, we discuss the structure and operation of the proposed low-leakage-power design stack with sleepy keeper. The proposed circuit is compared with well-known previous approaches, i.e., Basic NAND Gate, Forced stacking, Sleep transistor with Low V_{th}, Sleep transistor with High V_{th} & Sleepy Keeper. Firstly we discuss the operation of proposed NAND gate circuit. In standby mode, both the sleep transistors of pull up and pull down network are off, i.e. transistor M1, M2 and Y1,Y2 are off. We do so by making S'=1and hence S=0. A working of the NAND gate is similar to then inverter we use four transistors two PMOS pull up and two NMOS pull down, the output of the NAND gate is one either input is Zero with different combination of the input vector. In proposed approach we incorporate the stack approach with sleepy keeper approach for mitigating the leakage power in the circuit and improve the performance of the circuit by applying unique technique for leakage reduction.

In Proposed approach we have taken two technique stack approach with sleepy keeper approach to reduce the leakage power consumption in the circuit. Here we use two NMOS in pull down network and two PMOS in pull up network, so as to provide the stacking of the transistor for further leakage reduction. To maintain the proper logic level "1" we insert NMOS transistor parallel to PMOS stacked transistor in pull up network, to connect sleep transistor to V_{dd} to the pull up network. In sleep mode, this NMOS transistor connects V_{dd} to the pull up network when sleep transistor cut off.

Similar action also repeat in pull down network the two NMOS transistor provide the stacking effect (Fig.7.). To maintain the value "0" in sleep mode a PMOS transistor connect parallel with two NMOS transistor. To maintain an output value to "0" PMOS transistor connected to GND in sleep mode. For Proper Logic NMOS connect to V_{dd} and PMOS connect to GND. The stacking of the transistor reduces the leakage power in proposed approach and enhances the performance of the circuit by maintaining proper logic of the circuit.

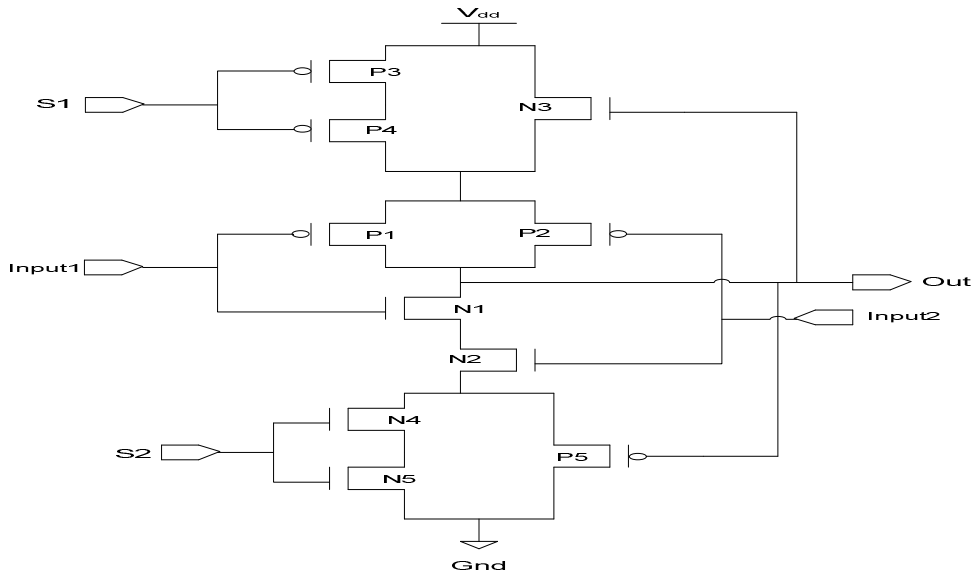

Fig.7. Proposed technique with Low V_{th} transistors

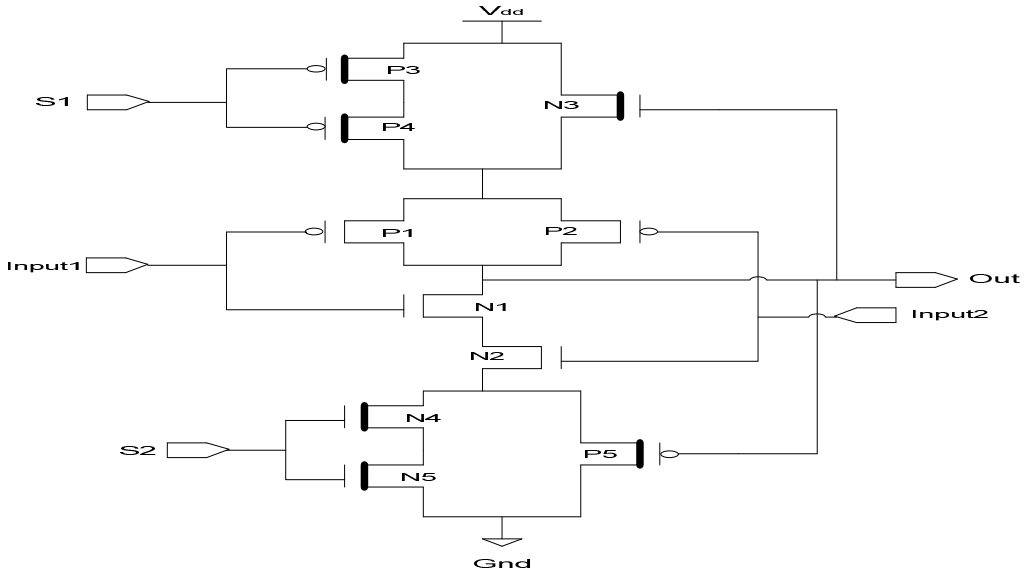

Fig.8. Proposed technique with high V_{th} transistors

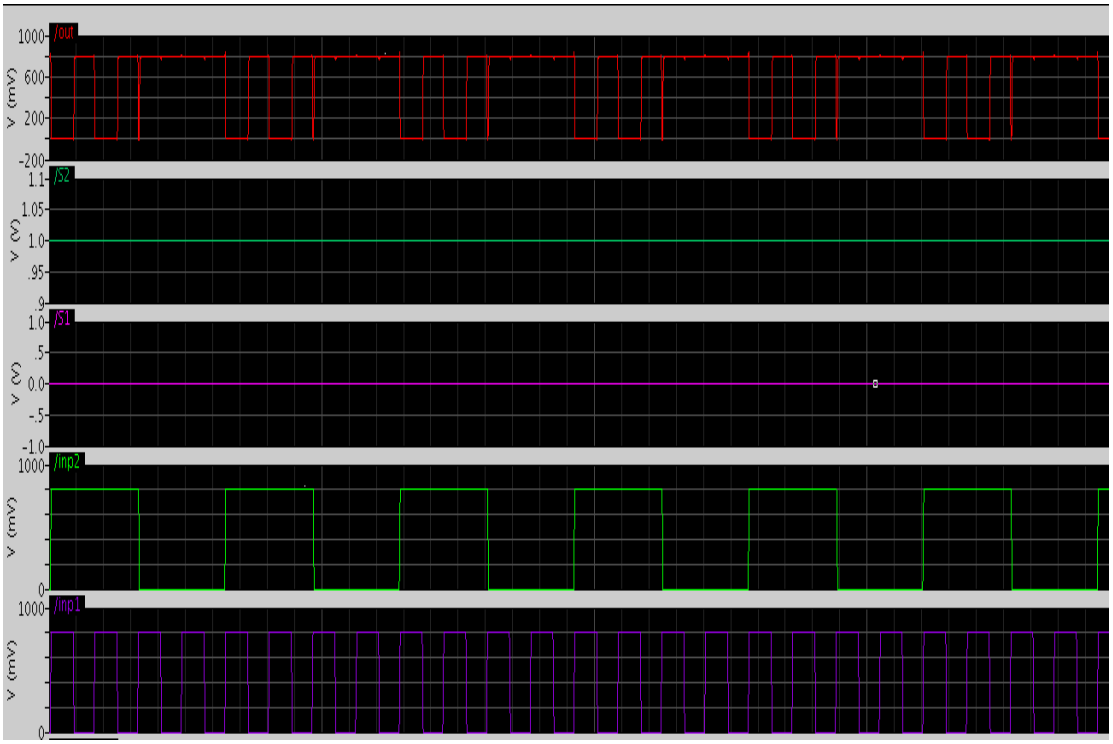

Fig.9. Output waveform of the proposed Circuit.

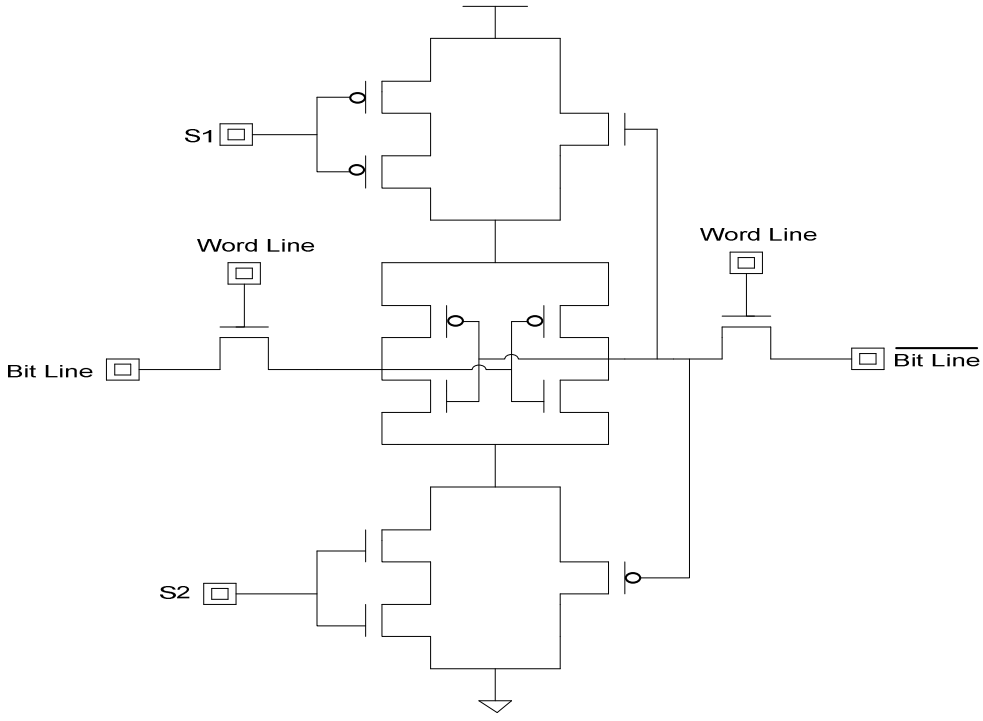

Fig.10. A SRAM cell in Proposed Approach

4. SIMULATION RESULTS

A 2 input NAND gate is simulated with leakage power reduction techniques sleep, forced stack, sleepy keeper and sleepy stack with DTCMOS. After analyzing the results in terms of average power consumption, static power consumption, delay and PDP we conclude that proposed circuit with DTCMOS is producing comparatively better results. All schematics are designed on Cadence virtuoso schematic editor and simulations are done on Cadence spectre simulator on 65nm technology and supply voltage of 1V. The circuits are simulated with high threshold and low threshold NMOS and PMOS transistors. The simulation wave form of the proposed circuit with NAND gate generates the proper Logic as shown in fig.8. and the Logic is further implemented in SRAM cell. Reduction of static Power with respect Basic Nand Gate 97.32%, 99.24%, Force Stack 63.61, 89.65%, sleep transistor with Low V_{th} & High V_{th} 45.84, 84.58% & 16.24%, 33.82% with respect to sleepy Keeper 29.91, 44.51% of static Power is saved.

Table.II. Comparison of Power, Delay, PDP & Static Power of sleep, forced stack, sleepy keeper and sleepy stack & Proposed Circuit with low V_{th} and high V_{th} NMOS and PMOS transistors.

Technique	**Average Power(uW)**	**Delay(ns)**	**Power Delay Product(PDP fs)**	**Static Power(ns)**
Base case NAND Gate	1.532	3.70	5.668	107.2
Forced stacking	2.49	9.76	24.30	7.869
Sleep Transistor with Low Vth	1.255	6.917	8.680	5.287
Sleep Transistor with High Vth	1.614	3.99	6.43	1.23
Sleepy Keeper	2.094	35.65	74.65	1.467
Proposed Circuit with Low Vth	1.081	.028	0.0302	1.032
Proposed Circuit with High Vth	.921	.081	.0746	.8149

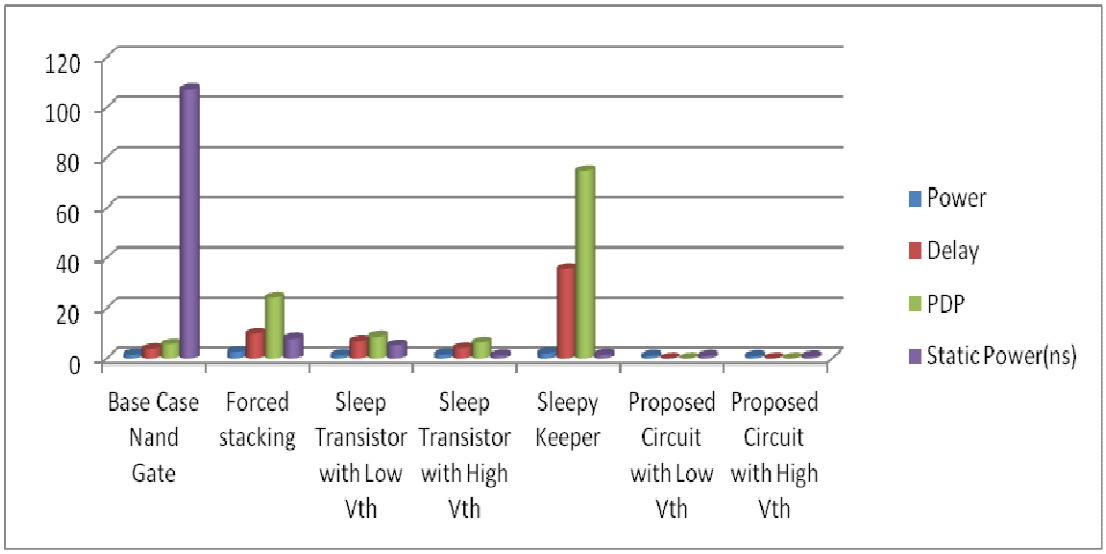

Fig.11. Comparison of Power, Delay, PDP & Static Power of sleep, forced stack, sleepy keeper and sleepy stack & Proposed Circuit with Low V_{th} & High V_{th} Transistor.

Table III. Comparison of SRAM Cell with proposed circuit with different Methods

Method	Static power(w)	Dynamic power(w)	Prop. Delay(s)	PDP
Base Case	93.03E-12	2.543E-6	15.11E-9	38.42E-15
Forced stacking	79.63E-12	1.869E-6	15.25E-9	28.50E-15
Sleepy Keeper	36.07E-12	2.356E-6	15.92E-9	37.50E-15
Sleepy Stack	18.90E-12	2.317E-6	15.16E-9	35.01E-15
Proposed Technique with SRAM	16.87E-12	1.107E-6	3.149E-9	3.46E-15

5. CONCLUSION

In nanometer scale CMOS technology, sub-threshold leakage power is compatible to dynamic power consumption, and thus handling leakage power is a great challenge. In this paper, we present a new circuit structure named "stacking with sleepy keeper Approach" to tackle the leakage problem. The Stacking with sleepy keeper Approach with DTCMOS has a combined structure of four well-known low-leakage techniques, which are the forced stack, sleep transistor techniques, DTCMOS. However, unlike the forced stack technique & the sleepy Keeper over technique can utilize high-V_{th} transistors without incurring large delay overhead. Also, unlike the sleep transistor technique, the combination of stack approach with sleepy keeper approach retain exact logic state and mitigate leakage power. In future new approach of leakage reduction technique at gate level and block level are expected to give more power saving than the existing approach at CMOS circuit level design.

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