COMPACT LOW-POWER HIGH SLEW-RATE CMOS BUFFER AMPLIFIER WITH POWER GATING TECHNIQUE

Ajay Yadav[1], Saurabh Khandelwal[2], Shyam Akashe[3]

[1]Research Scholar ITM, Gwalior, India
[2]Dept. Of ECE ITM, Gwalior, India
[3]Dept. of ECED ITM University, Gwalior India

ABSTRACT

A qualitative analysis of different parameters such as Phase noise, Slew rate and tranconductance by using power gating reduction technique is presented. The circuit achieves the large driving capability by employing simple comparators to sense the transients of the input to turn on the output stages, which are statically off in the stable state. The effect of the different number of transistors and their topologies on the phase noise and Slew rate is analyzed. Good agreement between qualitative and quantitative measurements is observed. Scope of reducing of Noise and avoidance of Leakage due to various sources is discussed.

KEYWORDS

Amplifier, buffer circuits, drains circuit, cascaded stages and source driver

1. INTRODUCTION

A buffer amplifier for higher driving capability with low static power is designed telescope-cascade based buffer amplifier for high resolution application in electronic display devices like TFT-LCD etc. [1] The buffer amplifier is best suited for electronic devices for achieving the fast speed capabilities, high resolution, and low power dissipation play a significant role for essentially determine the speed, resolution, voltage swing and power consumption of the buffer amplifier circuit [2]. A common mode rail to rail class-AB buffer amplifier use comparator circuit inside it to enhance the slewing capabilities with limited power consumption and it draw a very small quiescent current during static operation [3]. The capacitive load at the output of the circuit is responsible for reduced distortion for swing characteristics. In electronics, a comparator is a device that compares two voltages or currents and switches its output to indicate which is larger that is commonly used in analog to digital converters (ADCs) [4]. In the buffer constraints to increase the buffer space irrotically because the buffer depth is also increases with the maximum number of allowed circulation of the data in the buffer decreases. The power gating technique is most probably used to reduce the power consumption, low leakage, high speed and higher driving capability. The power gating technique is used to apply the reduction of power by using sleep transistor [6]. Power gating technique is a technique is used in integrated circuit design to reduce power consumption, by shutting off the flow of current to blocks of the circuit that are not currently in use. This technique is mostly used to reducing stand by or leakage power. Power gating uses low leakage PMOS transistors as header switches to shut off power supplies to parts of a design in standby or sleep mode. NMOS footer switches can also be used as sleep transistor. Inserting the sleep transistors splits the chip's power network into a permanent power network connected to the power supply and a virtual power network that drives the cells and can be turned off. Typically high V_t, sleep transistors are used for power gating, in a technique also known as

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multi threshold Cmos (MTCMOS). The sleep transistor sizing is important design parameters. Power gating has the benefit of enabling Iddq testing. In this paper, we present the benefits and costs of the power gating technique in terms of power, area, and performance. This technique is used for saving leakage leakage power by shutting off the idle blocks [7-8]. In this technique negative effects of power gating may overwhelm the potential gain and may make the technique not worth the efforts. Power gating techniques is also used for data retention means of storage, access, and encryption.

2. PROPOSED CIRCUIT AND OPERATION

2.1. Block Diagram

Figure Show the block diagram of the proposed two stage class AB buffer amplifier where C1and C2 are the current comparator which provide rail to rail input and output. MO1 and MO2 are the output complementary devices R_c represent the series resistors are mainly used for phase compensation at the output node. The load capacitance C_L is also connected to the output which is most portably used for swing characteristics of the output. The basic comparator circuit are used to swing the output at the lightest difference between its inputs but there are many variations where the output is designed to switch between two other voltage values also. The input may be tailored to make compares to an input voltage other than zero. The added comparators are used to reduce the power dissipation [10-11].

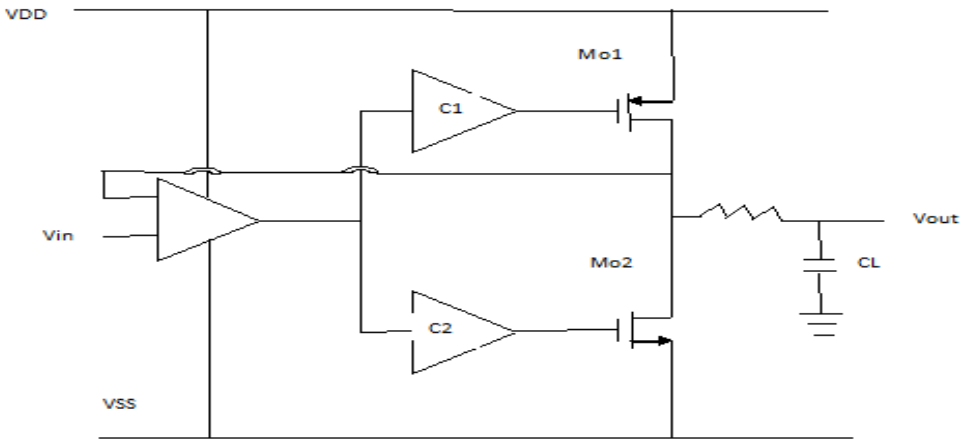

Figure1: Block diagram of buffer amplifier

2.2. Circuit Diagram

The transistor level implementation of the proposed output buffer is illustrated in figure below. In the given circuit V_{OUT} is connected to the inverting terminal Vin-, while the input signal is applied to the non-inverting terminal Vin+. The circuit are divided into three main parts. MB1 to MB6 represent a biasing network, M1 to M14 represent a rail to rail stacked mirror differential amplifier, MO1 to Mo2 represent a push pull output gain stages. $R_{c\ is}$ series resistance are used to show the connection between amplifier output and the load capacitor. Finally the buffer amplifier is capable of driving a wide range of load capacitance; phase compensation is performed by introducing a left half plane zero, which is produced by the load capacitance C_L [12]. The current buffers are mainly use frequency compensation technique. In current buffer amplifier the most popular common gate or cascode transistor topology used as a positive current buffer. To connect a capacitor across a high gain stage is the most significant compensation technique to improve the stability of the closed loop circuit. However to connect the capacitor in the output stage, a right half plane (RHP) zero is also created.

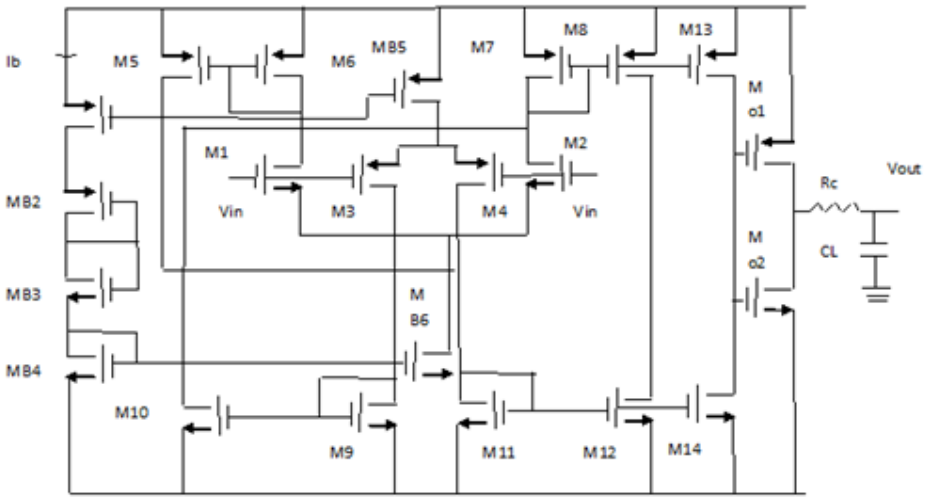

Figure2: Circuit schematic of the proposed two stage rail to rail buffer amplifier

The basic configuration scheme of the buffer amplifier with zero compensation technique is shown below [13-14]

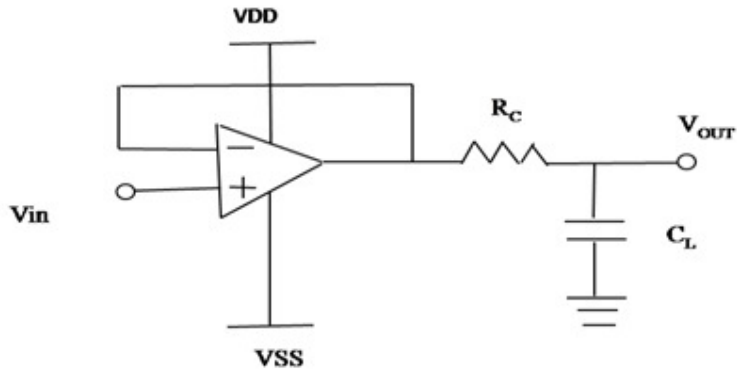

Figure3: Buffer amplifier with zero compensation technique

The most commonly used method is dominant pole compensation which is also called as lag compensation. In open loop response pole is placed at an appropriate low frequency to reduce the gain of the amplifier to one (0db) for a frequency at or just below the location of the next highest frequency pole. This result the difference between open loop output phase and the phase response of a feedback network having no reactive elements never fall below -180^o while the amplifier has a gain of one or more , ensuring stability.

3. SIMPLIFIER EQUIVALENT CIRCUIT REPRESENTATION OF THE PROPOSED OUTPUT DRIVING BUFFER

The simplified equivalent circuit of the proposed output buffer is depicted in figure below.

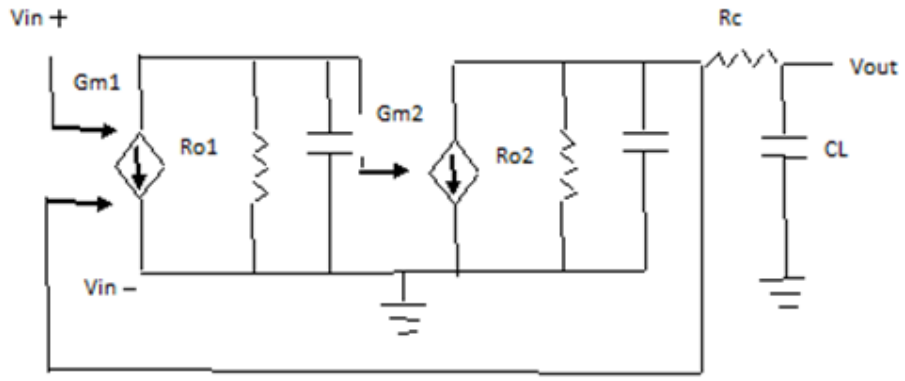

Figure4: Simplified equivalent circuit of the output driving buffer

Where gm1 and gm2 are the small signal tranconductance of the rail to rail stacked mirror differential amplifier and push pull output gain stages and Ro1and Ro2 represent the equivalent output resistances, Co1 and Co2 represent the output capacitances, whereas R_c represent the compensation resistor and C_L represent the equivalent capacitance of the LCD panel[15-16].

Assuming Ro1, Ro2 >> Rc and Co1, Co2 << C_L yields the following equations

$$A_V(S) = A_O \frac{1+\frac{S}{W_Z}}{\left(1+\frac{S}{W_{P1}}\right)\left(1+\frac{S}{W_{P2}}\right)\left(1+\frac{S}{W_{P3}}\right)} \quad (1)$$

Where Ao is the DC open loop gain is expressed by

$$A_0 = g_{m1} R_{01} g_{m2} R_{02} \quad (2)$$

While W_{P1} , W_{P2} and W_{P3} are the frequencies of the three amplifier real poles

$$W_{P1} = \frac{1}{(R_{02}+R_C)C_L} \approx \frac{1}{R_{02}C_L} \quad (3)$$

$$W_{P2} = \frac{1}{R_{01}C_{01}} \quad (4)$$

$$W_{P3} = \frac{1}{(R_{02}\|R_C)C_{02}} \approx \frac{1}{R_C C_{02}} \quad (5)$$

And W_Z is the frequency of the left-plane zero.

$$W_Z = \frac{1}{R_C C_L} \quad (6)$$

Here we represent W_{p3} is the third pole frequency; however the equivalent circuit has contain three poles, and its contribution to the amplifier transfer function is negligible. When we increase the value of R_c and C_L the phase margin is automatically increases.

4. DESIGN ASPECTS AND OPERATING PRINCIPAL

The differential pair circuit are designed to draw the static current value ηI_b, where I_b is the quiescent current which is supplied by the biasing network. The following relation is given below [17-18].

$$\eta = \frac{(W/L)_{MB5}}{(W/L)_{MB1}} = \frac{(W/L)_{MB6}}{(W/L)_{MB4}} \tag{7}$$

The above specification requires the following design condition to be fulfilled.

$$\frac{(W/L)_5}{(W/L)_7} = \frac{(W/L)_{10} - \Delta(W/L)}{(W/L)_{11}} \tag{8}$$

$$\frac{(W/L)_{14}}{(W/L)_{11}} = \frac{(W/L)_{13} \quad \Delta(W/L)}{(W/L)_7} \tag{9}$$

In quiescent state, no input signal is applied, current flowing in both input pair transistor are $\eta I_b/2$. Assuming M_5-M_6 and M_9-M_{10} are the current mirror image, While M_7 and M_{11}, draw the same static current ηI_b, in the output NMOS device MO2 would be pulled down towards V_{ss}. In PMOS device MO1 would pulled up towards Vdd. So we can say that at DC characteristics it consume no static power.

$$\Delta I_{13} = -g_{m1}\Delta V \frac{(W/L)_{13}}{(W/L)_7} \tag{10}$$

$$\Delta I_{14} = +g_{m1}\Delta V \frac{(W/L)_{14}}{(W/L)_{11}} \tag{11}$$

If ΔV is sufficiently large then we get the following expression

$$\Delta V > \frac{\eta I_B}{g_{m1}} \cdot \frac{\Delta(W/L)}{2(\frac{W}{L})_{13} - \Delta(W/L)} \tag{12}$$

$$\Delta I_8 = +g_{m1}|\Delta V \frac{(W/L)_8}{(W/L)_7} \tag{13}$$

$$\Delta I_{12} = -g_{m1}|\Delta V \frac{(W/L)_{12}}{(W/L)_{11}} \tag{14}$$

If the negative input step $\Delta V|$ is sufficiently large to get

$$\Delta V| > \frac{\eta I_B}{g_{m1}} \cdot \frac{\Delta(W/L)}{2(W/L)_{11} - \Delta(W/L)} \tag{15}$$

The power dissipated in the amplifier is of three types. The static power dissipation due to the dc bias current from the power supply of each transistor. The dynamic power dissipation due to the charging and discharging of the load capacitance and the direct path dissipation due to the current going through PMOS and NMOS transistor during transition.

The static energy dissipation for this circuit during a scanning period is expressed as

$$E_{static} = \frac{I_{bias} V_{DD}}{f_{scanning}} \tag{16}$$

Where I_{bias} is dc bias current, $f_{scanning}$ is the scanning frequency. So we can say that amplifier always consume static dissipation.

For dynamic power dissipation is expressed as

$$P_{charge} = (V_{DD} - V_o)I_L$$

$$= (V_{DD} - V_0)C_L\frac{dv_o}{dt} \quad (17)$$

The energy dissipated in PMOS is as

$$E_{charge} = \int_{V_L}^{V_H} P_{charge}dt$$

$$= C_L V_{DD}(V_H - V_L) - 1/2C_L(V_H{}^2 - V_L{}^2) \quad (18)$$

And then the $P_{discharge}$ is as

$$P_{discharge} = -V_0 I_L$$

$$= - V_0 C_L \frac{dv_0}{dt} \quad (19)$$

$$E_{discharge} - \int_{V_L}^{V_H} P_{discharge}\,dt$$

$$= 1/2C_L(V_H{}^2 - V_L{}^2) \quad (20)$$

5. POWER GATING TECHNIQUE

In such a circuit, the supply voltage is turned off during the standby mode by using a PMOS transistor or an NMOS transistor with proper switch sizing leakage power can be reduced by more than two orders of magnitude. Power gating technique is also used for optimizing power and delay. In active mode, the sleep transistor is on and the circuit functions as usual [19]. In standby mode, the switch transistor is turned off, which disconnects the logic gate from power or ground. The basic mechanism by which the switch transistor reduces the leakage current of the power gated logic transistors is the increased body effect [20].

A power gated semiconductor integrated circuit comprises:

i. Logic circuit to be power gated, said logic circuit having a virtual ground rail.

ii. Footer device disposed between said virtual ground rail and a ground rail for reducing power consumption of said logic circuit; and

iii. Virtual rail voltage clamp disposed electrically in parallel with said footer device for limiting the voltage at the virtual ground rail, the virtual rail voltage clamp comprising at least one NFET.

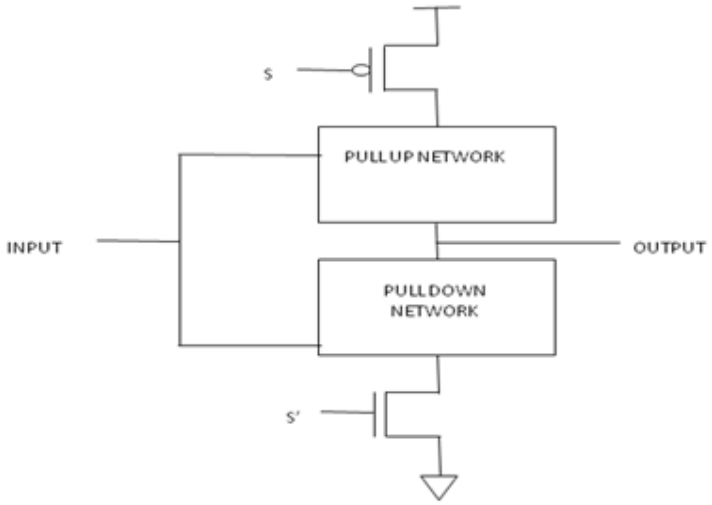

Figure5: The proposed power gating structure

6. MODELLING AND SIMULATION RESULTS

Figure show the Transient response curve of CMOS buffer amplifier circuit is shown in given below at 45 nm technology by cadence virtuoso tool.

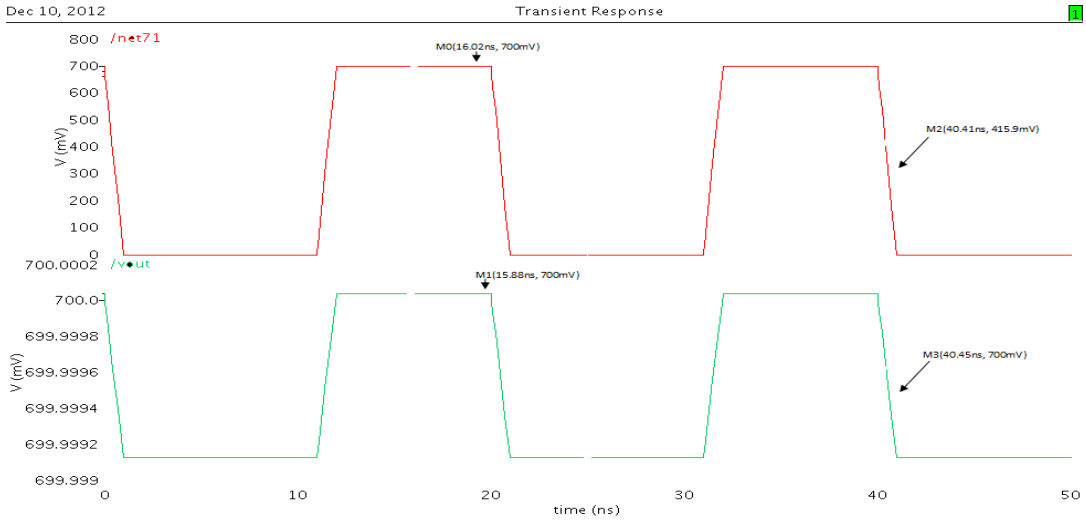

Figure6: Transient response curve of buffer amplifier

The graphical representation of reduced leakage current value by power gating reduction technique in which the value of reduced peak leakage current value 56.01nA is at 0.7v is shown in given below at 45 nm technology by cadence virtuoso tool.

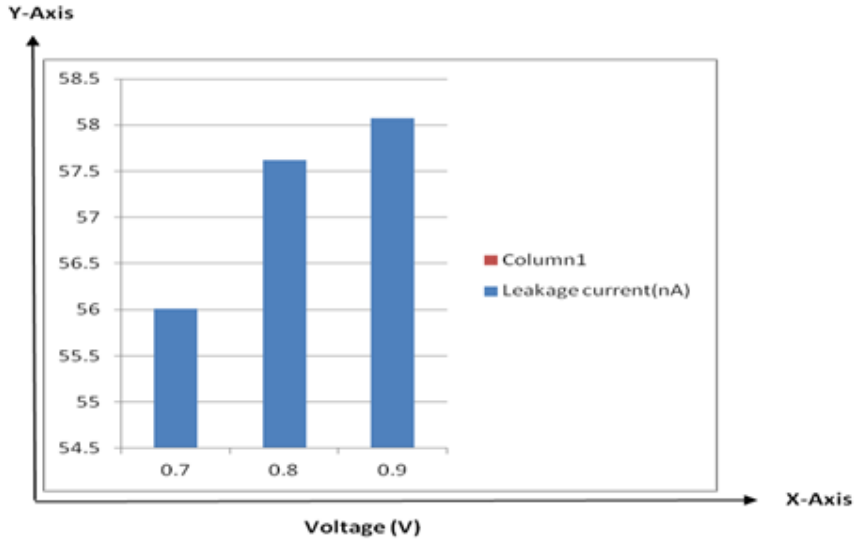

Figure7: Graphical representation of leakage current

Figure Show the Graphical representation of phase noise having a value of 56.01dbc/Hz by using Power gating technique at 45 nm technology by using cadence virtuoso tool.

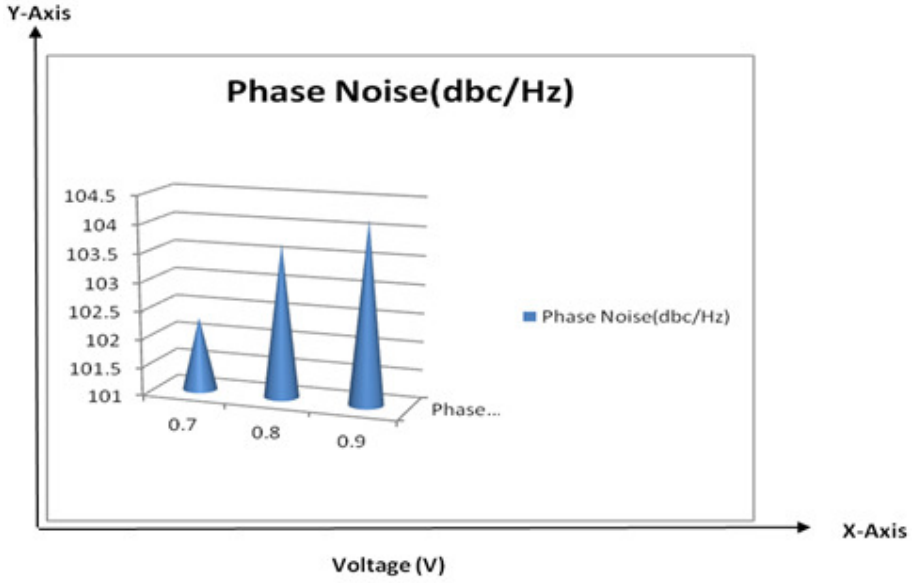

Figure8: Graphical representation of phase noise curve

Figure show the Graphical representation of Active power of peak value is 372.2pW by using Power gating technique to consume power for the maximum output at 45 nm technology is shown below by using cadence virtuoso tool.

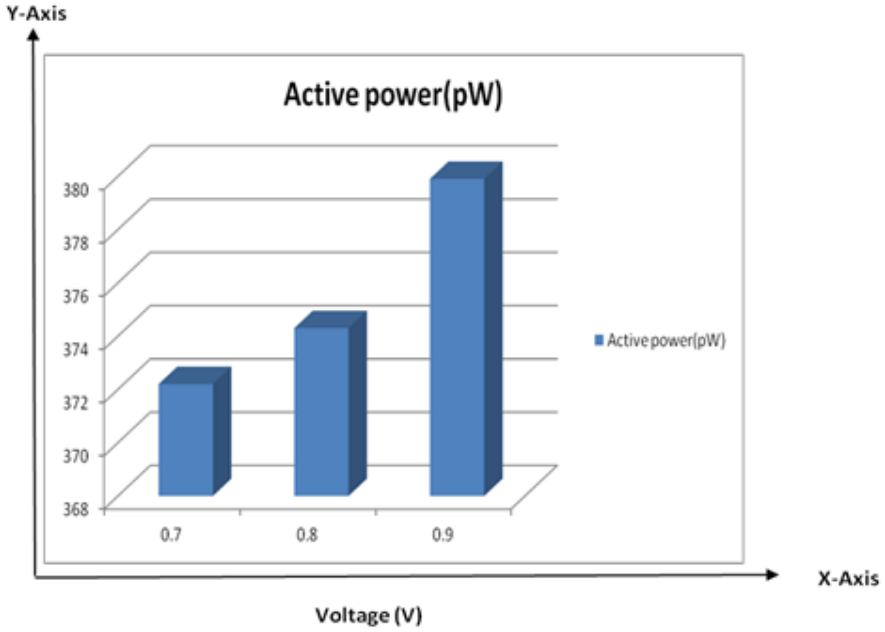

Figure9: Graphical representaion of active power waveform

Figure Show the pole zero response curve of having a value of -55.5db by using Power gating technique in the circuit at 45 nm technology by using cadence virtuoso tool.

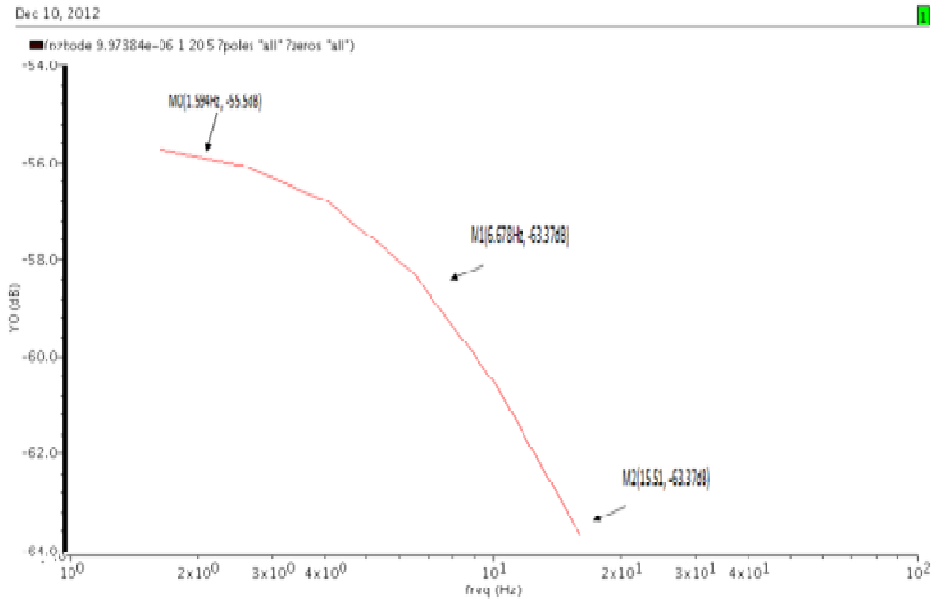

Figure10: Pole zero response curve of power gating technique

The slew rate is defined as a maximum rate of change of output voltage per unit of time and is expressed as volt per second and the tranconductance is the property certain electronic components. Conductance is the reciprocal of resistance; tranconductance is the ratio of the current change at the output port to the voltage change at the input port.

Figure Show the Graphical representation of Slew rate and Tranconductance by using Power gating technique having the maximum peak value is 15.96and 7.55 is shown in given below at 45 nm technology by using cadence virtuoso tool.

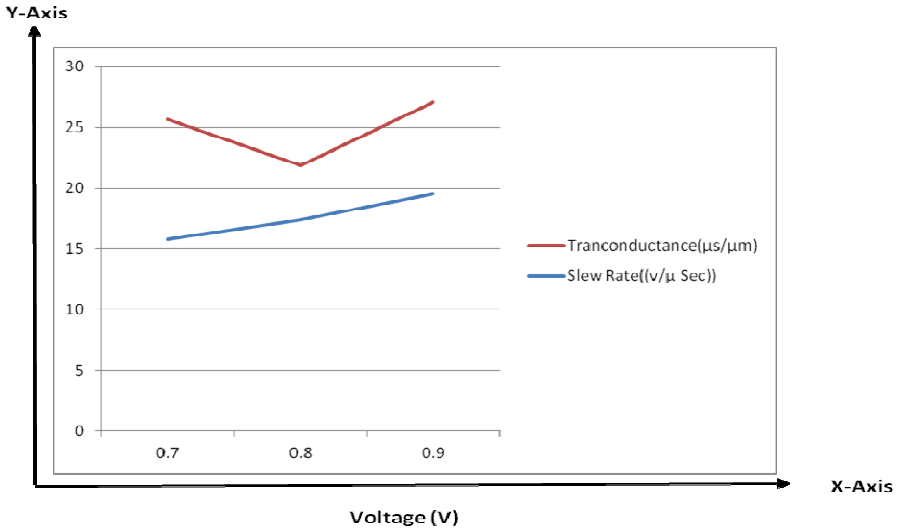

Figure11: Slew rate and tranconductance waveform

The table of different parameter is shown in table below

S.N	PARAMETERS	CONVENTIONAL TECHNIQUE	MTCMOS TECHNIQUE	POWER GATING
1.	Power(pW)	375.6	371.5	372.2
2.	Leakage current(nA)	56.66	55.96	56.01
3.	Tranconductance(µs/µm)	9.83	4.51	7.55
4.	Slew rate (V/µ sec.)	15.81	15.41	15.96

7. CONCLUSIONS

This paper presents a comparative analysis of different parameters at 45nm technology for getting a better high speed, large output swing, high performance and offer common mode rail to rail input range using power gating reduction technique. It consume low power, low leakage current and higher slew rate and tranconductance makes the amplifier circuit most suited for high resolution display viz. LCD and TFTs etc. As per simulation results applying power gating reduction technique reduced parameters are obtained. We observed noise 102.3db/Hz, low leakage 56.01nA and a better slew rate 6.56 (µs/µm) at 45 nm technology. The proposed output buffer circuit is best suitable for flat panel display.

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AUTHORS

Ajay Yadav was born on 29th June 1985. He completed his Bachelor of Engineering from S.R.I.T.S Datia, India. At present He is pursuing M. Tech in VLSI Design from ITM University, Gwalior India. His area of interest is Low power CMOS VLSI Design, Logic circuits.

Saurabh Khandelwal is born in Gwalior (India) on 10th May 1988. He did M-Tech (VLSI Design) from Rajiv Gandhi Technical University, Bhopal. He is presently pursuing Ph.D. from ITM University, Gwalior. Mr. Khandelwal has authored/co-authored numerous research papers. His research papers have been published in various peer reviewed National/International Journals including those enlisted in the Thomson Reuters List of Journals, and Conferences including 27th M.P. Young Scientist Congress.

Shyam Akashe was born in 22nd May 1976. He received his M.Tech from ITM, Gwalior in 2006. He is currently working as Associate Professor in Electronics Instrumentation Engineering Department of Institute of Technology Management, Gwalior. Currently, He has completed his Ph.D from Thapar University, Patiala on the topic of Low Power Memory Cell Design. His research interests are VLSI Design.