A LOW POWER FRONT END ANALOG MULTIPLEXING UNIT FOR 12 LEAD ECG SIGNAL ACQUISITION

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ABSTRACT

The design of CMOS analog circuitry for acquiring 12 lead ECG is presented. The existing methods employ separate multiplexers and associated circuitry for signal acquisition operating at typical voltage of ± 5V. The proposed system employs dynamic threshold logic to achieve low power, wide dynamic range good linearity with a supply voltage of 0.4V. The power dissipation obtained was 22.12µW. Utilizing the dynamic threshold logic the proposed circuitry is implemented with 0.18µm CMOS technology. This ECG signal processor is highly suitable for wearable applications of long term cardiac monitoring.

KEYWORDS

12 Lead ECG, Dynamic Threshold, dynamic range, Low power, analog multiplexer

1. INTRODUCTION

Electrocardiography (ECG) is the recording of heart's electrical activity by placing electrodes at specific points on the surface of the body. The electrical activity is produced by polarization and depolarization of the cell membrane during heart beat. These appear as tiny electrical signals on the skin which can be detected and amplified by the ECG. Electrocardiogram (ECG) is the electrical representation of the contractile activity of the heart over time, which can be easily recorded using noninvasive electrodes on the chest or limbs. Long-term recording and analysis of ECG is useful and necessary for those who suffer cardiovascular diseases, so that the patient and doctors can continuously monitor the status of cardiac activity. Some wearable ECG recording and monitoring devices are proposed. Some of them can realize multiple functions but with large size and power consumption [1], [2]. Some of them can be implemented in application-specific integrated circuits (ASIC) but with limited functions [3].

With technological improvement in CMOS design have triggered interest in designing the functional units of digital systems. The areas like high performance computing, Telecommunication etc. has demanded for the usage of integrated circuits which has been growing at a higher rate. With this trend the design of energy efficient VLSI system has become more important. In today's global scenario low power design has a emerged as an important

DOI : 10.5121/vlsic.2014.5306

theme. The requirement for low power has created a major shift in paradigm, where power dissipation is considered more important as performance and area.

Biomedical applications demands for portable devices which has triggered the development of CMOS analog multiplexer circuits. The battery life time should be maximum in these portable devices and hence require low power dissipation [4]. Specially, the multichannel recorders of portable devices are required to be operated at low supply voltage making the power consumption and supply voltage constriction a key factor in these designs [5]. However the threshold voltage of the Metal Oxide Semiconductor [MOSFET] do not scale down with supply voltage and this puts a limitation for the low voltage design[6].

The analog multiplexer plays an important role in biomedical applications such as MEA's [Multi Electrode Arrays] which are extensively used to record signals from the human body [7]. Designing analog multiplexer low voltage application is very challenging and trade off is obtained between switching frequency, signal losses and power consumption. Very little research has been reported for ultra low voltage applications. Even though many efforts were made to develop low power analog multiplexers, Multichannel electrode arrays consisting tens of electrodes have driven for the development of integrated circuits to record selected set of signals from the human body [8]. In a multichannel system transferring signals from each individual electrode to any data acquisition system through the cable would be very expensive and is not feasible technically. The most important block of such integrated circuit is analog multiplexer. The multiplexer will reduce the number of output data links.

The measurement sequence typically compromises reading of signals from multiple channels at high speed and to avoid loss of signal by means of multiplexer to a single output. In our design the multiplexer is built with a decoder and transmission gates. The signals in the form of physical variables like voltage and currents and which are continuous functions of time should be processed by analog systems. Processing of these variables must be carried out with high accuracy. The direct signal processing in high frequency applications and specific biomedical signal processing requires these analog circuits. With the advent of VLSI technology the usage of computers played a vital role in the areas of telecommunications, biomedical applications, robotics etc. In almost any complex integrated circuit the analog circuits are used together with digital circuits which are CMOS circuits. CMOS switches have great characteristics in which the MOS transistor in its ON states offers very low resistance typically less than 100 ohms with very low leakage current. The packaging density of CMOS technology in an ICis high and compatible with logic circuitry [9]. The transistor switching characteristics are well controlled with very low circuit leakage. The transistors can switch both positive and negative currents equally.

For reducing power consumption a common technique employed is to reduce the supply voltage, but reducing the supply voltage means lowering the performance. The problem of performance degradation can be eliminated by scaling the threshold voltage. As a result the static power consumption increases by lowering threshold voltage [11]-[12].

To improve MOSFET performance a standard CMOS architecture with constant substrate biasing technique can also be used. Indeed, the threshold voltage V¬T can be reduced and the device speed increases by forward body biasing. Whereas to control the off state leakage current for low power applications where static power dissipation is important factor [13] reverse body biasing can be used.

High speed integrated circuits tend to have higher leakage and hence reverse body bias can be applied to reduce leakage and frequency. Similarly slow speed circuits can utilize forward body bias to improve their speed at the cost of increase in leakage power.

Normally ECG is recorded as the voltage difference between two electrodes and is named as lead. In total ECG is recorded as 12-Leads by placing 10 electrodes on the body. Leads I, II and III are referred as Limb leads. Leads aVR, aVL and aVF are named as Derived Limb leads and V1 to V6 are named as chest leads. Standard 12 Lead ECG system is explained in table I given below.

Table:1. Various lead voltages, actual and derived.

Lead_I	LA-RA	Voltage difference left arm and right arm.
Lead_II	LL-RA	Voltage difference left leg and right arm.
Lead_III	LL-LA (Lead-II minus Lead-I)	Voltage difference left leg and left arm. It is usually a derived lead
V_W (Wilson central terminal)	1/3(LA+RA+LL)	This is used as a references terminal to record chest leads (V1-V6).
aVR	(Lead_I+Lead_II)/2	
aVL	Lead_I- (Lead_II)/2	
aVF	Lead_II- (Lead_I)/2	
V1	(Vc1-Vw)	
V2	(Vc2-Vw)	
V3	(Vc3-Vw)	
V4	(Vc4-Vw)	
V5	(Vc5-Vw)	
V6	(Vc6-Vw)	

This paper proposes a highly integrated multi lead ECG signal processing circuitry, which can achieve low power and small area hardware implementation. IN this work a CMOS integrated circuit for acquiring 12-Lead ECG signal is designed and implemented in 0.18µ Technology. This system was operated with 0.4 v supply voltage and achieved very low power dissipation.

2. DESIGN ASPECTS

An Analog switch is implemented by using transmission gate which will selectively block or pass a signal level from the input to the output. This analog switch is comprised of a pMOS transistor and nMOS transistor shown in fig:1

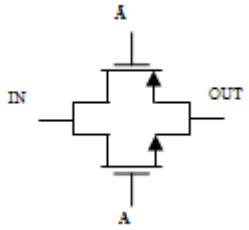

Fig: 1 Transmission gate

The gates of both the transistors are biased in a complementary manner so that both transistors are either ON or OFF and there will be drop in amplitude of the signal at the output. To overcome this problem and getting the original signal without any loss the transmission gate is modified by stacking the transistors as shown in Fig-2.

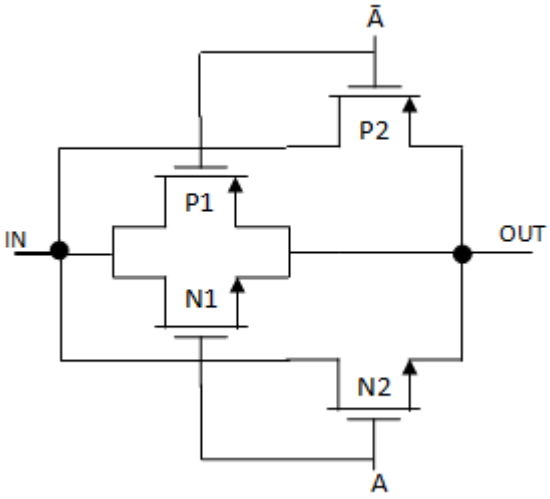

Fig: 2. Modified Transmission gate

The staging of transistors will improve the aspect ratio, performance and very low ON resistance and the circuit is shown in Fig 2. The width of transistors is maintained in the ratio 1:2 for NMOS to PMOS. Staging a transistor with two fingers will provide larger variation in the performance since the variation made to two finger is twice than that made to a single transistor.

The ON resistance R_{on} of the switch is

$$Ron = \frac{1}{g_{ds}} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_{Th})}$$

The overdrive voltage, $V_{ov} = V_{gs} - V_{th}$, the aspect ratio, W/L through the trans conductance parameter μCox will affect the value of the ON-resistance. The ON resistance obtained is 32 ohms and the OFF resistance is 10Mohms.

3. BODY BIASING

The voltage difference between the Transistors Source and the Bulk (V_{SB}) will effect the change in Transistor Threshold voltage V_T. Since V_{SB} effects V_T the bulk can be treated as second Gate that helps to identify how the transistor turns On and OFF.

Body effect refers to the change in the transistor threshold voltage (V_T) resulting from a voltage difference between the transistor source and body. Because the voltage difference between the source and body affects the V_T, the body can be thought of as a second gate that helps determine how the transistor turns ON and OFF. The strength of the body effect is usually quantified by the body coefficient γ (gamma). The threshold voltage of MOSFET is well known as,

$$V_{Th} = V_{Th0} + \gamma_B(\sqrt{2\phi_F + V_{SB}} - (\sqrt{2\phi_F})$$

where V_{SB} is the voltage between source and bulk, ϕ_F is the bulk Fermi- potential ,V_{Th0} is the threshold voltage when V_{SB}=0 and γ_B is the body-effect coefficient. Therefore varying threshold voltage Vth can be changed by varying V_{SB} which can form dynamic threshold voltage MOSFET (DTMOS). Normally, the source and body junction is either zero-biased or reverse-biased. Forward-body-biased MOSFETs can also be used on some circuit to improve performance with lower threshold voltage VTh [10]. This concept is utilized in designing the power analog multiplexer. The transistors are operated in strong inversion region by means of using 0.4 V forward body bias. The Modified transmission gate is shown in Fig-2.

The variety of body biasing techniques is enable by strong body effect and these techniques for effectively utilized in older generation. This body bias can be applied externally (external to the chip) or internally (in chip). The internal approach normally utilizes a charge pump circuit provide reverse body bias or potential divider to produce forward body bias. Reverse body bias for an n channel transistors increases the threshold voltage and makes the transistors both slow and less leakage. On the other hand forward body bias reduces the threshold voltage making the transistor fast and with more leakage. The polarities of the body bias are opposite for P channel transistor.

4. MULTIPLEXER DESIGN

In the past many designs of multiplexers are developed which are based on the concept of shift registers as described in[1].The chain of D-latches connected in series and are triggered with external clock synchronously form a shift registers. Each latch activates readout of one S&H cell. A major drawback of this circuit is clock feed through which produces glitches with every positive and negative clock edge. This drawback is eliminated in present multiplexer design.

Changing the body bias multiple times while in operation is termed as dynamic body bias. To optimize low power operations and to reduce temperature and aging effects as well as to make power management modes more effective the dynamic body bias technique can be utilized.

Consequently, dynamic body bias can be used to reduce temperature and aging effects as well as to make power management modes more effective at optimizing very low power operation.

The single channel circuit using dynamic body bias is designed as shown in fig-3, the bulk voltage for the NMOS and PMOS transistors calculated 200mV and 30mV respectively. This has reduced the threshold voltage to 0.3V in the proposed method. The required body bias is applied to the respective transistors by the select signal through potential dividers.

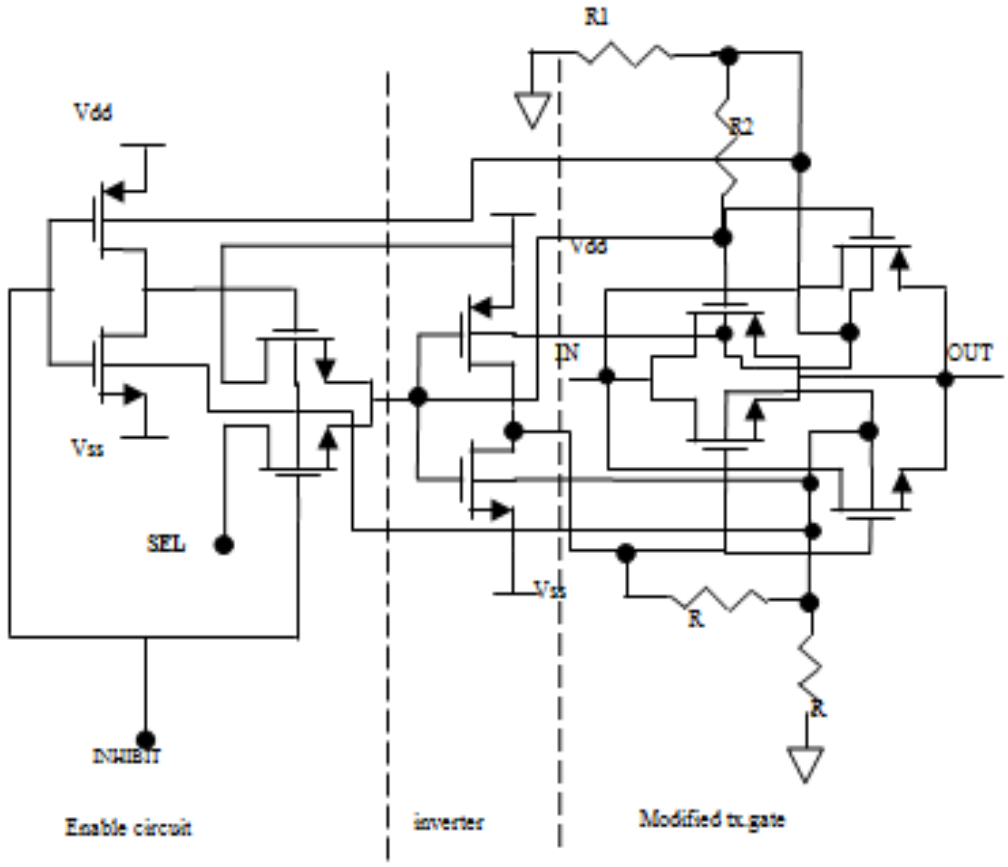

Fig: 3 DTMOS Single Channel Circuit

The input signal will be passed from IN to OUT all the transistors turns ON and this happens when the SEL at logic 0 and it's complementary is applied to NMOS transistor. The input signal will be blocked when all the transistors turned OFF and this happened when SEL signal is logic 1.The output will be forced into high impedance state while switching from ON to OFF and this causes the junction capacitance to charge to few mvolts.

This drawback is removed by a PMOS device utilized as pass transistor between output and ground forcing the junction capacitance to discharge to ground when all the transistors are in OFF state.An analog multiplexer having 8 channels was designed utilizing the circuit shown Fig.3 for each channel employing 3 binary signals for channel selection. An inhibit (INH) input is provided for switching the multiplexer ON and OFF.

Measurements made in 0.18µm technology showed leakage current pico Amps On resistance of 32ohms and OFF resistance of 10 Mohms and very low feed through capacitance. The analog switches used had low leakage current in the order of Pico amperes, low ON resistance(32 ohms), high OFF resistance(10Mohms), low feed through capacitance in the order of 'fF' were obtained.

5. SYSTEM DESIGN

The block diagram of the proposed multiplexing unit for processing 12 Lead ECG is shown Fig.(4). The different Lead signals of ECG are obtained from difference between two electrodes as given in Table-1. Accordingly the various electrode signals were given as inputs to the corresponding multiplexers. The channel select signals were generated by a 3-8 decoder as given in Table-2.

Table-2: Channel select signals generated by a 3-8 decoder

INHIBIT (INH) D	DECODER INPUTS C B A C B A	SELECTED OUTPUTS
L or 0	0 0 1 to 1 1 1	MUX1 & MUX2
H or 1	0 0 1 to 1 1 0	MUX1 & MUX3

MUX1 was designed with 7 channels and other two were designed with six channels each. When the INH (D) is LOW MUX1 and MUX2 are enabled and MUX3 will be disabled. Leads I,II,III, aV_R, aV_L and aV_F are produced by recording the difference between the outputs of MUX1 and MUX2 as decoder changes states. When the INH (D) goes HIGH the channel 7 of MUX1 which is the average of Leads I,II and III (Wilson central terminal) is continuously selected and along with this MUX2 will get disabled and MUX3 is enabled. As the decoder inputs changes each state the difference between MUX3 and MUX1 outputs were recorded as chest Leads (V_1-V_6).

A single 3-8 decoder is used to drive all the multiplexers for selecting each channel is shown in block diagram.

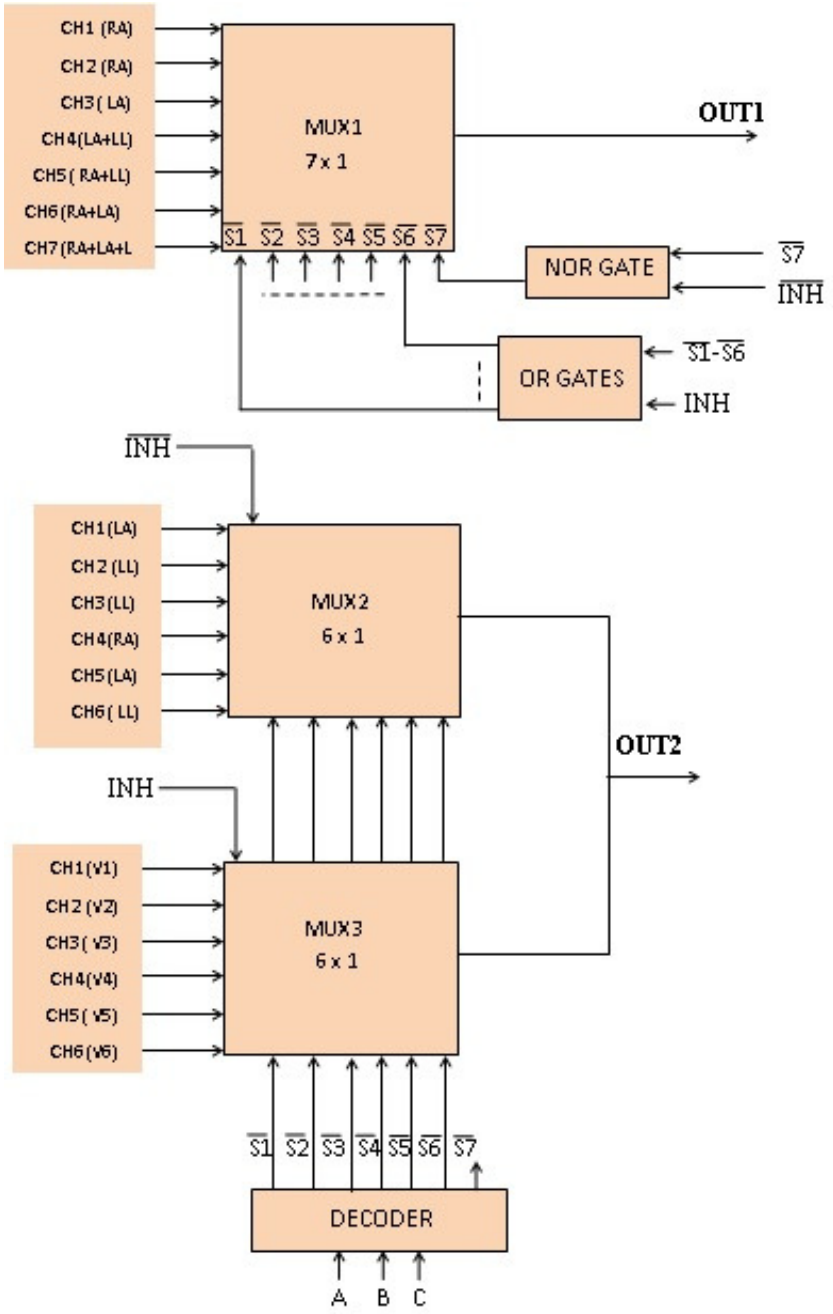

Fig:4 Block Diagram of the Proposed System

6. RESULTS

The circuit is tested by applying sinusoidal signals to each channel with amplitudes ranging from 1µv to 0.4V. The inputs for channel selection of the corresponding Multiplexers are simulated as outputs of a 4 bit binary counter with MSB bit acting as INH bit and the others as inputs to the decoder. The selection of MUX and corresponding channels is given in the Table 3 below.

Table:3. Channel selection of the corresponding multiplexer

INHIBIT	DECODER INPUTS C B A	MUX1 o/p	MUX2 o/p	MUX3o/p
0	0 0 1	CH1	CH1	-
0	0 1 0	CH2	CH2	-
0	0 1 1	CH3	CH3	-
0	1 0 0	CH4	CH4	-
0	1 0 1	CH5	CH5	-
0	1 1 0	CH6	CH6	-
1	0 0 1	CH7	-	CH1
1	0 1 0	CH7	-	CH2
1	0 1 1	CH7	-	CH3
1	1 0 0	CH7	-	CH4
1	1 0 1	CH7	-	CH5
1	1 1 0	CH7	-	CH6

The input dynamic range of the circuit is measured by applying input signals of amplitudes ranging from 1 µV to 7 µV , 1mV to 7 mV and 100mV to 400mV from channel 1 to 7 respectively. The multiplexer outputs are measured by selecting individual channels through decoder and the recorded waveforms are shown in Fig. 5.a, 5.b and 5.c

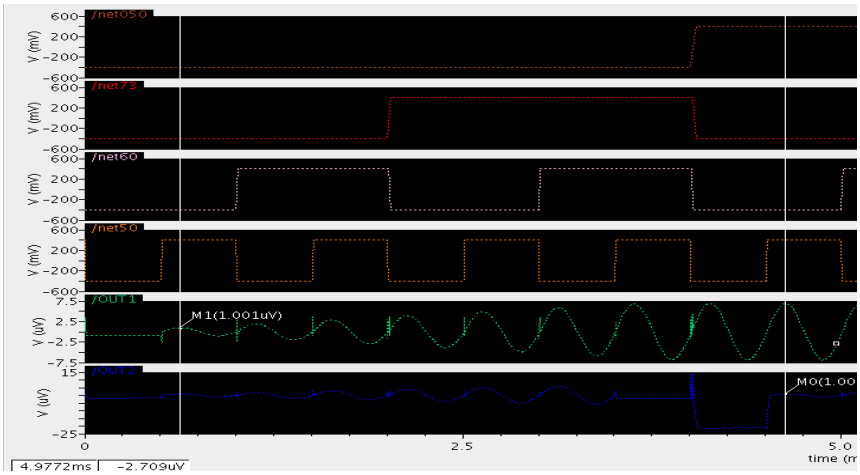

Fig: 5(a) simulated results with an amplitude of 1,2,3,4,5,6,7 µV for Ch-1 to Ch-7

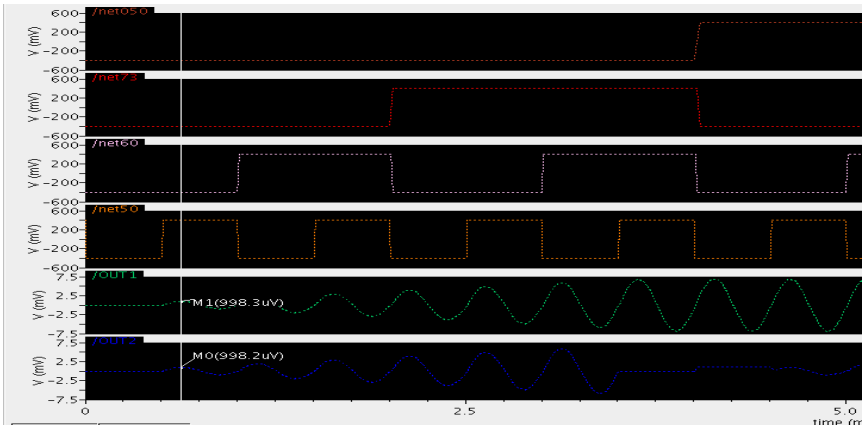

Fig :5(b) simulated results with an amplitude of 1, 2,3,4,5,6,7mV for Ch-1 to Ch-7

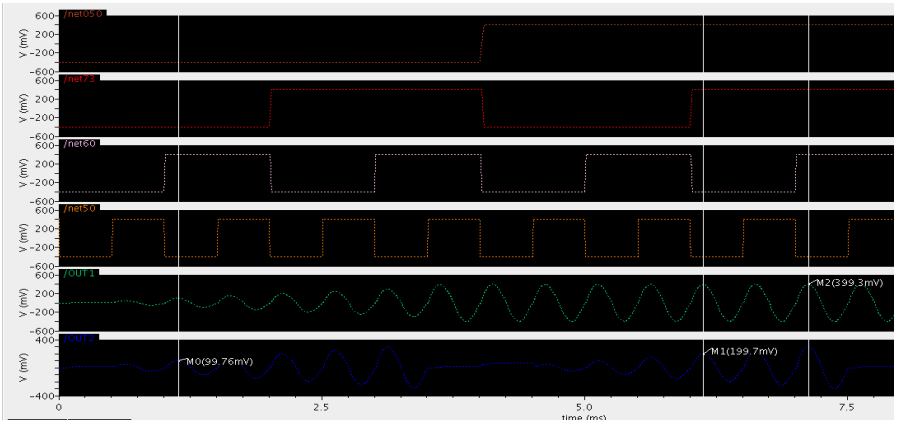

Fig: 5(c) simulated results with an amplitude of 100,150,200,250,300,350, 400mV for Ch-1 to Ch-7

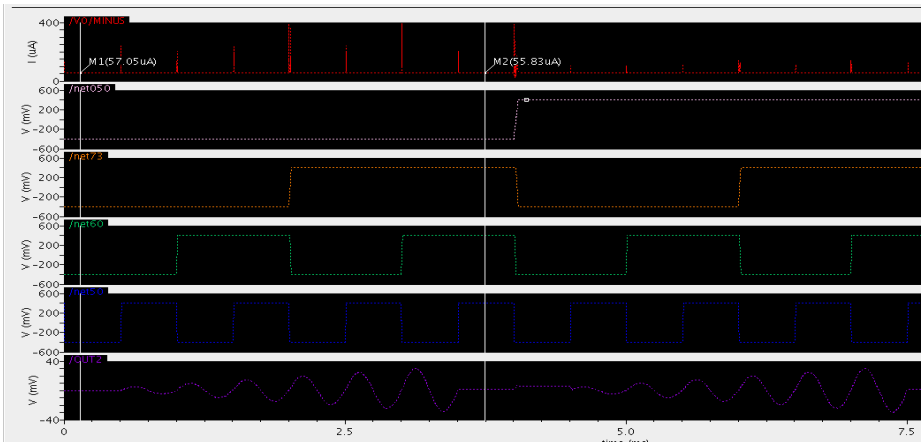

Fig: 5(d) simulated results with measured current

The channel selection frequency i.e, the decoder inputs are varied from as low as 1Hz to 1 KHz and the outputs are obtained without any distortion. The circuit has drawn a power of 22.12 µW as shown in Fig 5(d).

The dynamic power dissipation is measured at various switching frequencies ranging from DC to 1MHz and the graph is shown in Fig (6). The power consumed is 22.12µW up to a switching frequency of 300 kHZ. The power dissipation increased with the increase in frequency above 300KHz. 25.32 µW is dissipated at frequency of 1MHz

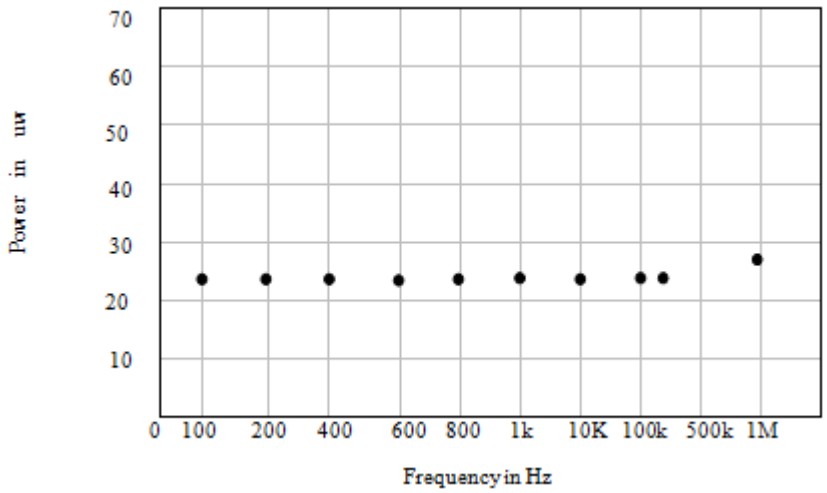

Fig: 6 switching frequency vs power dissipation

Despite the Shichman-Hodges model is a simplified first-order model suitable for long-channel transistors only, it suits the purpose to illustrate that *Vth* is non-linear dependent on the applied body biasing. The *Vth* reduces with FBB, and contrarily increases with RBB. *Vth* is strongly process dependent.

The results have been shown for the traditional process corner conditions, while they have been obtained through CADENCE SPECTRE SIMULATOR transistor model for the respective technology node to account for all short-channel effects. Observe that the actual value of Body Bias and its sensitivity to Drain current as strongly depends on the process corner: fast, typical, or slow.

Table: 4 PVT corner simulation of NMOS Transistor

VDD	SS MODEL			TT MODEL			FF MODEL		
Temp	-40^{0}C	27^{0}C	110^{0}C	-40^{0}C	27^{0}C	110^{0}C	-40^{0}C	27^{0}C	110^{0}C
0.9V	1.5V	1.43V	1.287V	1.3V	1.35V	1.38V	1.47V	1.43V	1.25V
0.8V	1.5V	1.35V	1.17V	1V	1V	1V	1.45V	1.33V	1.168V
0.7V	1.405V	1.26V	1.08V	1V	1V	1V	1.38V	1.25V	1.08V
0.6V	1.29V	1.165V	990 mv	1V	1V	959 mv	1.29V	1.148V	990 mV
0.5V	1.19V	1.07V	900 mV	992 mv	1V	880 mV	1.199V	1.05V	900 mV
0.4V	1.108V	963 mV	784.4 mV	1V	959 mV	800 mV	1.1V	960 mV	781.1mv
0.3V	1.01V	871.2mV	687.7 mV	991 mV	800 mV	678 mV	1.03V	870 mV	689.8 mV

Table: 5 PVT corner simulation of PMOS Transistor

VDD	SS MODEL			TT MODEL			FF MODEL		
Temp	-40^{0}C	27^{0}C	110^{0}C	-40^{0}C	27^{0}C	110^{0}C	-40^{0}C	27^{0}C	110^{0}C
0.9V	0	0	0	0	0	0	0	0	0
0.8V	63.1 mV	0	0	54 mV	0	0	56 mV	0	0
0.7V	150.9 mV	48.6 mV	0	162.8 mV	54.1 mV	0	162.3 mV	47.5 mV	0
0.6V	242 mV	130.5 mV	21.2 mV	261.2 mV	144 mV	22 mV	267.1 mV	154.9 mV	14.6 mV
0.5V	350 mV	227.7 mV	86 mV	343 mV	223 mV	86 mV	358.6 mV	242 mV	99.5 mV
0.4V	438.9 mV	311 mV	153.2 mV	441 mV	315.3 mV	158 mV	447.3 mV	331.9 mV	186 mV
0.3V	525mV	411 mV	259.1 mV	525 mV	411 mV	257 mV	552 mV	434 mV	285 mV

For the typical NMOS and PMOS device, maximum drain current is obtained with a bulk voltage of 959 mV and 315.3mV respectively as shown in Table 2&3 below. The charging / discharging of output and internal nodes will become slow as the forward biased source/drain junction leakage (Ijunc) opposes close-to – linearly increasing on current Ion. This degrades output high and low levels. Increasing the junction parasitic Capacitance, slows down the circuit.

7. CONCLUSIONS

A new approach for implementing an analog multiplexing unit for acquiring 12-Lead ECG from different electrode signals is designed and simulated in 0.18µm CMOS technology. The new topology uses dynamic body biasing reducing threshold voltage. However to operate the transistor in strong inversion mode a 0.4V supply is used. Measurement results show that the input signals are passed without any distortion upto a maximum switching frequency of 300 kHz and the power dissipation was 22.12µW. The inputs to a decoder are simulated as outputs from a 4-bit counter. The proposed method overcomes the disadvantages of many existing methods, by operating at low voltage and low power, thus it can be used in a system for long term monitoring of ECG.

ACKNOWLEDGEMENTS

The authors express their sincere thanks to Chairman Anurag Group of Institutions Dr. P. Rajeswar Reddy for all his support. They are indebted to Prof. K.S.R. Krishna Prasad, NIT Warangal for his valuable suggestions. They also express thanks to Prof. J.V. Sharma H.O.D ECE Dept. AGI, and The management of K. L. University Vijayawada

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