AN EFFICIENT MULTI RESOLUTION FILTER BANK BASED ON DA BASED MULTIPLICATION

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ABSTRACT

Multi-resolution filter bank (MRFB)-based on the fast filter bank design can be used for multiple resolution spectrum sensing. MRFB overcomes the constraint of fixed sensing resolution in spectrum sensors based on conventional discrete Fourier transform filter banks (DFTFB) without hardware re-implementation. Multipliers have a greater impact on complexity and performance of the design because a large number of constant multiplications are required in the multiplication of filter coefficients with the filter input. Modified multiplier architecture Distributed Arithmetic(DA) is used to improve the efficiency

KEYWORDS

Filter Bank, MRFB, Multipliers, DA Based Multiplication

1. INTRODUCTION

A filter bank is an array of band-pass filters that separates the input signal into multiple components. Signal processing systems needs more room to store data during the processing, transmission and reception. In order to reduce the data to be processed, save storage and lower the complexity, multi rate sampling techniques were introduced to achieve these goals. The conventional method for sensing the multiple bandwidth channels is to have a fixed sensing resolution using discrete Fourier transform filter banks (DFTFB), where resolution is fixed as per the bandwidth of the channel that has the smallest bandwidth among all the channels of multiple standards. This method will sense a wider bandwidth channel by adding together the smaller bands of fixed resolution. But when the input signal is having channels of varying bandwidths, the conventional method of fixed sensing using the smallest sensing resolution becomes complex as the method needs to utilize the most stringent specification for a relaxed bandwidth. This will increase the dynamic power and delay in obtaining the output. The proposed MRFB-based spectrum sensor can adapt to different sensing detection bandwidths for wideband spectrum sensing without hardware re-implementation.

The proposed MRFB for spectrum sensing is a low complexity filter design approach based on FFB [2], with variable sensing resolution.FFB is a low complexity filter bank [2], proposed as an alternative to DFTFBs. The FFB consists of several sub filters of lower order arranged in a tree fashion. The FFB makes use of a technique called as frequency response masking (FRM) [4]. The basic idea behind the FRM technique [4] is to compose the overall sharp transition-band filter

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using several wide transition-band sub filters. However, the reconfigurability potential of FFB is hardly exploited in literature. In the proposed MRFB architecture, we modify the FFB design, by incorporating reconfigurability to each of the sub filters for varying the sensing resolution in MR.

FFT provides the means to reduce the computational complexity of the DFT from order (N^2) to order ($N \log_2(N)$), it is often desirable to do FFT-based processing for DSP systems.

A. Dft Fb

DFB[7] consists of a set of filter banks as shown in the figure. The process of decomposition performed by the filter bank is called *analysis* (meaning analysis of the signal in terms of its components in each sub-band); the output of analysis is referred to as a sub band signal with as many sub bands as there are filters in the filter bank. The reconstruction process is called *synthesis*, meaning reconstitution of a complete signal resulting from the filtering process.

But the disadvantage of the DFB is that all the filter banks should be active for all the time and the resolution also should be maintained according to the smallest bandwidth.

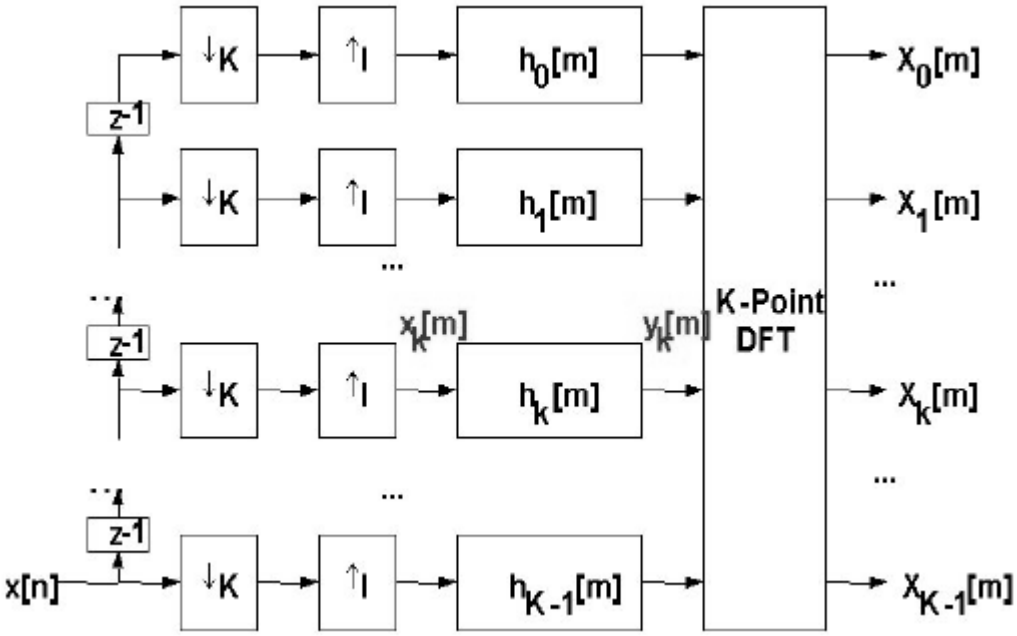


Fig. 1: Basic Block Diagram of a DFT based Filter Bank

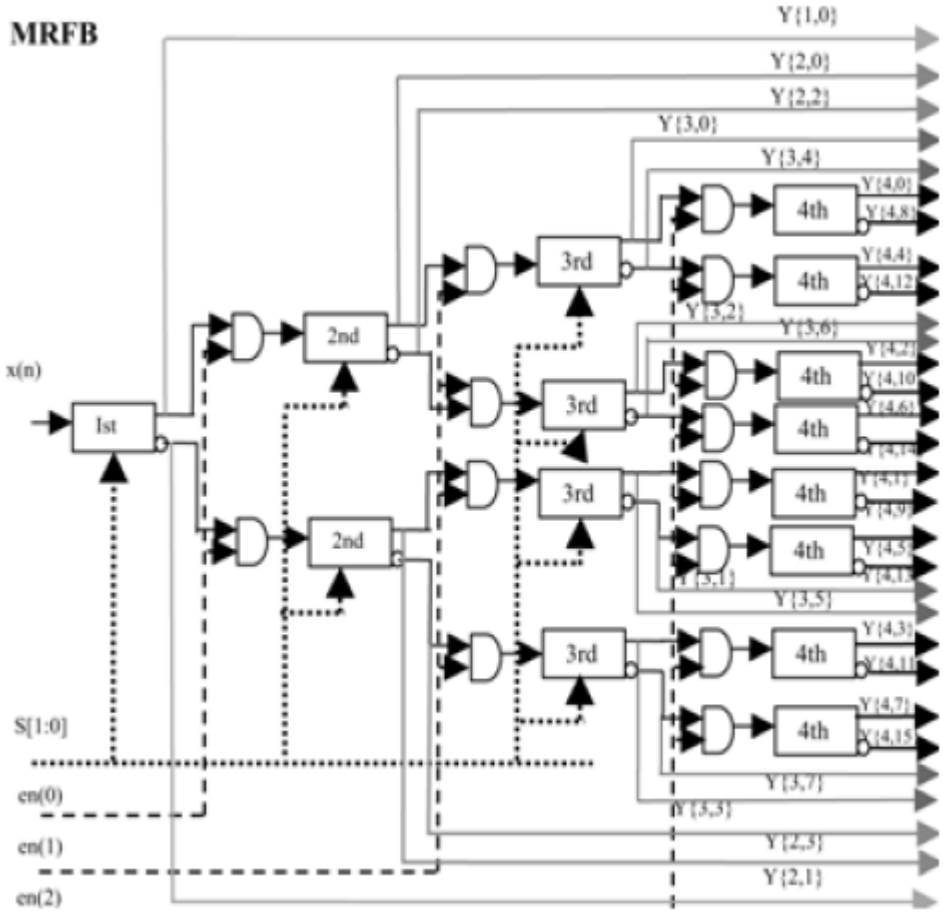


Fig. 2: MRFB Architecture

TABLE I
USING MRFB FOR RE-CONFIGURABILITY WITH SELECT(S) AND ENABLE(EN) SIGNALS

S[1:0]	En[0:2]	No. of Channels
11	111	16(BW=0.05)
10	110	4(BW=0.1)
01	100	2(BW=0.2)
00	000	1(BW=0.4)

B. Multi Resolution Filter

The FFB is suitable for the design of filter banks due to its reduced complexity [2]. The FFB follows a tree structure and it can be decomposed into several stages. For a k-stage FFB, we can realize 2^k channels. The sub filters $H_{ij}(z)$, where $j > 0$ are modulated versions of prototype filter and together they form the basic structure of FFB .Each stage is interpolated by a factor M and we can get both the original and complementary responses from each stage. A complementary filter can be obtained by subtracting the output of the (M+1) band response from a suitably delayed version of the input. If each of these (M+1) bands is masked using suitably designed

masking filters in k-1 stages, we can obtain 2^k channels. In this paper, reconfigurabilty is incorporated into FFB architecture so that the filter response can be changed by varying the interpolation value according to the resolution required in the spectrum sensor. Using the proposed spectrum sensor, the sensing resolution can also be changed using software reconfiguration.

Figure 2 shows an 8-channel MRFB architecture and Table I describe how channel bandwidth is modified with select (S) and enable signals (En).

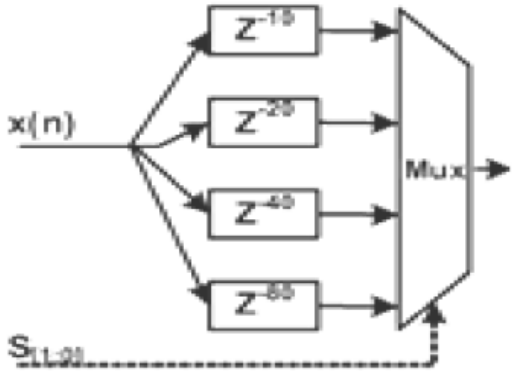


Fig. 3: Reconfigurable Filter Architecture for first stage

The length of the filters can be obtained from the expression (1).

$$N = \frac{-2\log_{10}(10*\delta_p*\delta_s)}{3(f_{sb}-f_{pb})} - 1 \quad (1)$$

The reconfigurable architecture for the first stage is shown in Fig 3. The FFB is realized in the form of a system of filters organized in a parallel tree structure.

2. MODIFIED MULTIPLIER ARCHITECTURE

Multipliers are one of the most important arithmetic units in filter banks. Due to their complex structure multipliers are the major source of power dissipation in such systems. The speed of multiplier also limits the system performance. With the advance of VLSI technology, the size of transistors becoming smaller and smaller, so that more number of transistors can be integrated into same silicon area to achieve high functionality density and performance. On the other hand higher transistor density also leads to higher power density. Various research works aiming at reducing the power consumption or the speed have been reported.

3. DISTRIBUTED ARITHMETIC BASED MULTIPLICATION

The multiplier block of the digital FIR filter in its transposed form involves the multiplication of filter coefficients with the filter input [11].

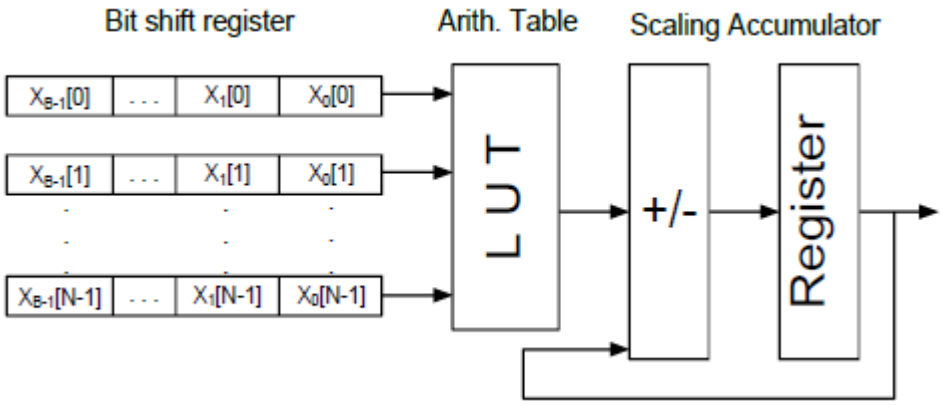


Fig. 4: DA Block Diagram

The multiplication of filter coefficients with the input data is generally implemented under a shift adds architecture where each constant multiplication is realized using addition/subtraction and shift operations in an MCM operation[12]. The basic idea is to replace all multiplications and additions by a table and a shifter-accumulator.

$$y = \langle c, x \rangle = \sum_{n=0}^{N-1} c[n]x[n] = c[0]x[0] + c[1]x[1] + \ldots + c[N-1]x[N-1] \tag{2}$$

$$y = \langle c, x \rangle = \sum_{b=0}^{B-1} 2^b \sum_{n=0}^{N-1} c[n] \times x_b[n] \tag{3}$$

DA relies on the fact that the filter coefficients are known, so multiplying c[n]x[n] becomes a multiplication with a constant.

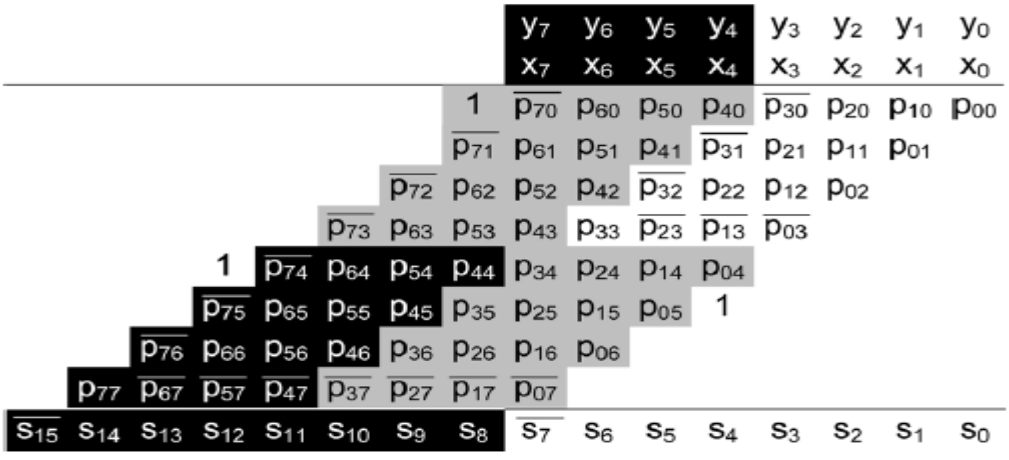


Fig. 5: Baugh Woolean Algorithm

4. SIMULATION AND COMPARISON RESULTS

The programs for 8 channel DFB, MRFB, Baugh Woolean Multiplier Based MRFB are designed using Verilog codes and each filter bank is compiled using Model SIM and simulated to verify their outputs and the simulation results are shown in Fig 6, 7, 8.The codes are synthesized in Cadence RTL compiler using typical libraries of TSMC 0.18 um technology and area and power analysis was done.

The table II shows the comparison of area, delay and power of the three different types of filter bank implementations. From the table II, the area and power of the proposed Modified multiplier Based MRFB is much less than that of the existing systems. Fig 6 and 7 shows the area and power comparisons of different filter bankss.

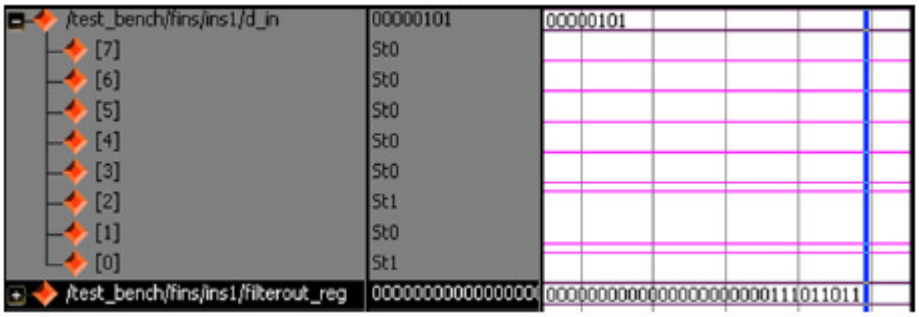


Fig. 6: Simulated Result for DFB

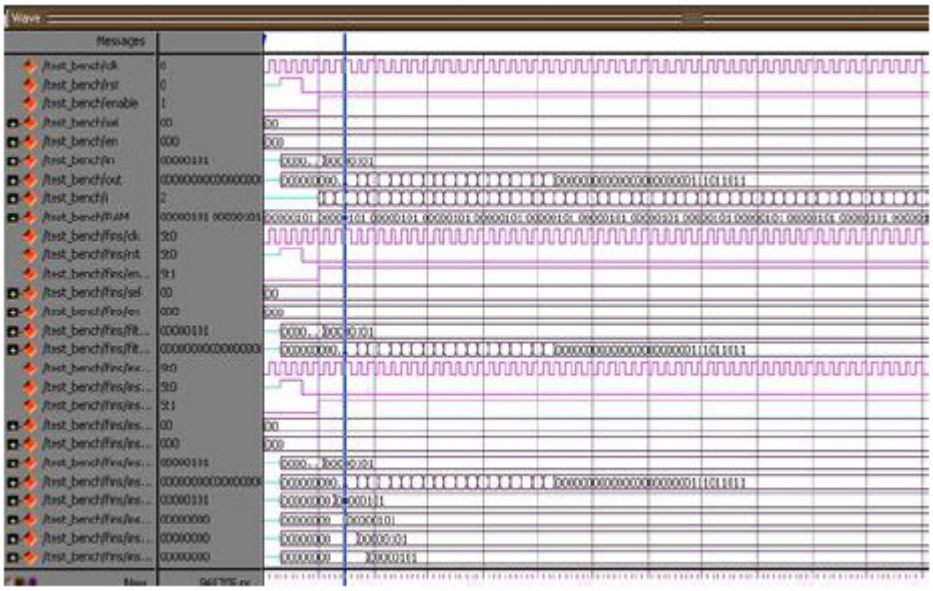


Fig. 7: Simulated Result for MRFB

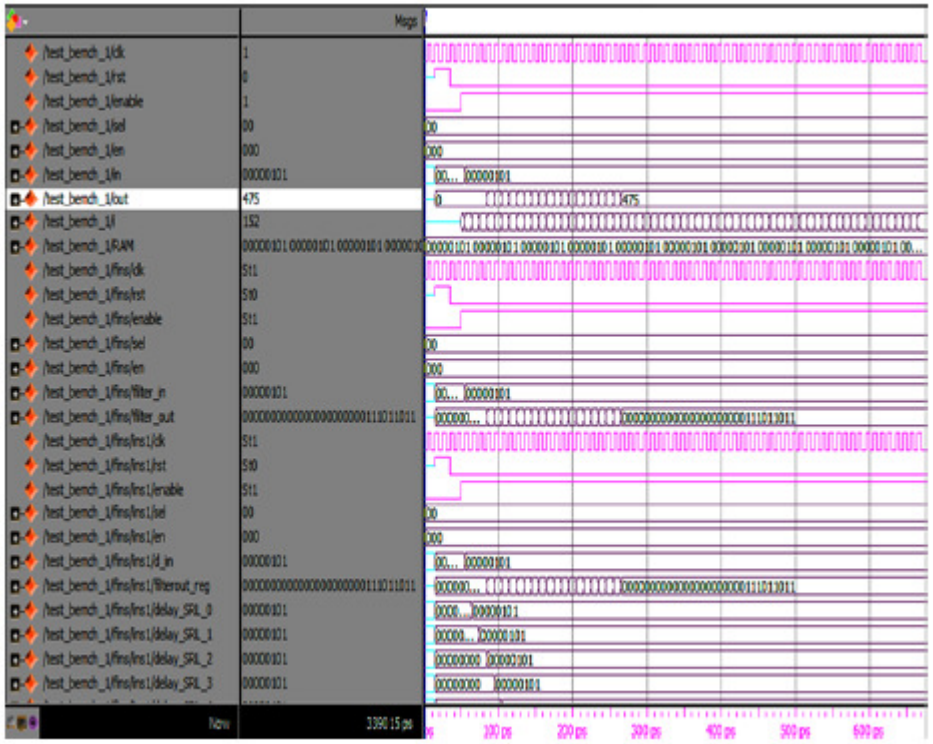
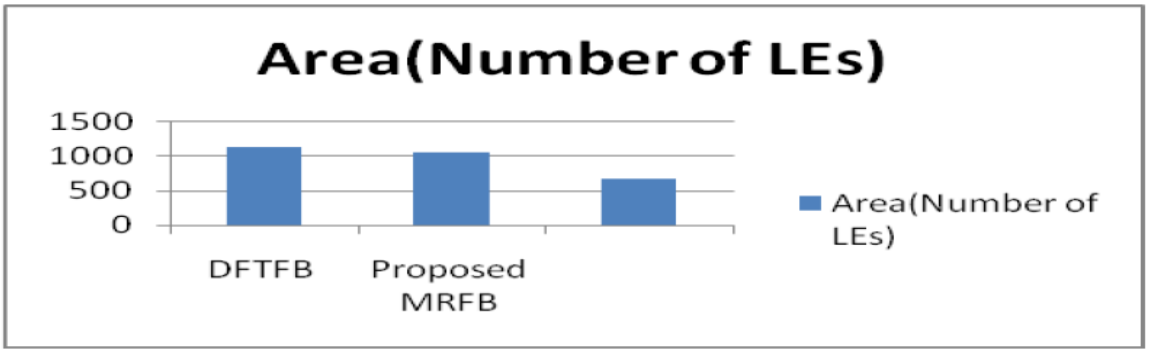
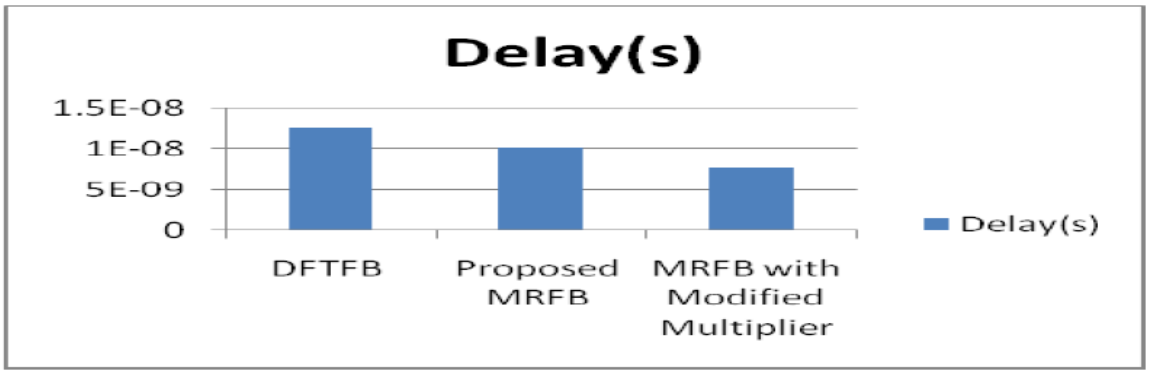


Fig. 8: Simulated Result for MRFB with modified multiplier





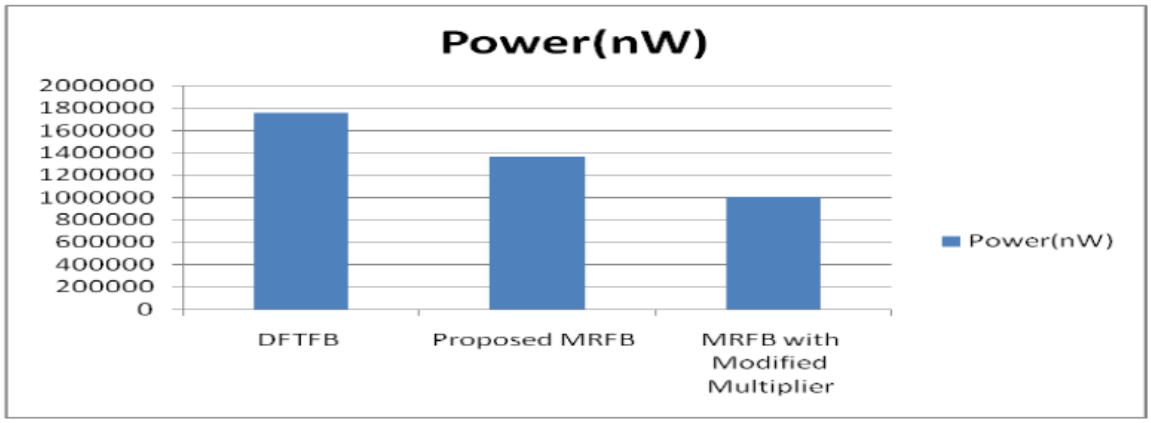


Fig. 9: Comparison plots of DFB, MRFB, Modified MRFB

TABLE II
COMPARISON OF AREA, DELAY AND POWER

	DFTFB	**Proposed MRFB**	**MRFB with Modified Multiplier**
Area (Number of Les)	1140	1052	670
Delay(s)	1.249531 x 10^-8	1.005126 x 10^-8	0.7620001x 10^-8
Power (nW)	1763211.53	1365499.92	1001491.02

In this paper, an efficient Multi Resolution Filter Bank is proposed by modifying the multiplier design based on Distributed Arithmetic .This can replace the multiplier which are more prominent in the convolution operations with shift and add mechanism. In this way, the transistor count can be reduced to a greater extend and hence the power. In the case of 8 bit MRFB the area has been reduced to 1052 from 1140 of DFB. In DA Based MRFB it is further reduced to 670. From the results it can be seen that the area, power and delay of the DA based MRFB is much less than that of DFB and the normal MRFB.

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