ANALYTICAL MODELING OF ELECTRIC FIELD DISTRIBUTION IN DUAL MATERIAL JUNCTIONLESS SURROUNDING GATE MOSFETS

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ABSTRACT

In this paper, electric field distribution of the junctionless dual material surrounding gate MOSFETs (JLDMSG) is developed. Junctionless is a device that has similar characteristics like junction based devices, but junctionless has a positive flatband voltage with zero electric field. In Surrounding gate MOSFETs gate material surrounds the channel in all direction , therefore it can overcome the short channel effects effectively than other devices. In this paper, surface potential and electric field distribution is modelled. The proposed surface potential model is compared with the existing central potential model. It is observed that the short channel effects (SCE) is reduced and the performance is better than the existing method.

KEYWORDS

JLDMSG (Junctionless dual material surrounding gate) MOSFETs, DIBL, Short channel effects (SCE).

1. INTRODUCTION

MOSFET devices can be broadly classified into junction based devices and junctionless devices.In this paper junctionless device characteristics has been analysed. MOSFET is a transistor used for amplifying and switching electronic signals. MOS device are used in ICs with high level of integration for reducing the current consumption. According to MOORE's law the number of transistor on integrated circuits doubles approximately every two years. This motivates IC fabrication with MOSFET devices.

The number of transistor in a IC can be increased by device miniaturization. Scaling of devices can be defined as reducing feature size that leads to better and faster performance and more gate per chip. Scaling of devices aims at increasing packing density, chip functionality, device current and speed of the machine. Nowadays IC scaling has reached nanometer size but still there arises the main problem that was faced during micro scale size which is defined as short channel effect. Short channel effect arises when control of the channel region by the gate is affected by the electric field lines propagating between source and drain. Some of the short channel effect [1] are

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Drain induced barrier lowering(DIBL) that happens when drain voltage is increased further at shorter channel length, the depletion region and body grows in size and extends to the gate and thus the potential barrier in the channel reduces, this causes changes in the threshold voltage. To overcome this, the electron gains a kinetic energy, but because of this excess energy the electron can enter the oxide region and makes oxide charging due to which the switching characteristics of the device get degraded.

Conventional MOSFET give rise to many short channel effects. This give rise to the multigate MOSFET which refers to a MOSFET that incorporates more than one gate into a single device. In multigate device, the channel is surrounded by several gates on multiple surfaces [2]. It thus provides a better electrical control over the channel, allowing more effective suppression of "off-state" leakage current. Multiple gates also allow enhanced current in the "on-state", also known as drive current. Multigate transistor also provide a better analog performance due to a higher intrinsic gain and lower channel length modulation [3].

As Multigate devices gave a route to the device miniaturization, it has made scaling of devices to reach aggressive performance. At this nanometer size, it becomes very hard to control the sharp source/drain junction from the device fabrication point of view. These challenges were overcome by the new evolved generation termed as junctionless devices. Junctionless is a device that have similar structure like conventional MOSFET but it is normally a ON device with homogeneous doping polarity across the source, drain and channel [4]. Junctionless Surrounding gate MOSFET provides a good performance as the gate material surrounds the channel at all the region. Junctionless is also treated as a device with high current drive since major carriers do not form a barrier to carrier scattering as in junction based devices [5]. Junctionless devices added low budget as it eliminates annealing and ion implantation in the fabrication process [6].

Junctionless is similar to conventional MOSFET but it has a difference in its operation. Classical MOSFET is considered as the OFF device whereas Junctionless is considered as the ON device. In the subthreshold region, the highly doped channel is fully depleted, and hence it can hold a large electric field [7]. By increasing gate voltage, electric field in the channel reduces until a neutral region is created in the centre of the channel. At this point, it is possible to define the threshold voltage, because bulk current starts to flow through the centre of the channel [8]. Then by further increasing the gate voltage, the depletion width reduces until a completely neutral channel is created. This occurs when the gate voltage equals the flat band voltage. At the onset of this condition, the bulk current reaches its maximum value. Thereafter, by increasing the gate voltage further, negative charges accumulate on the surfaces of the channel [9]. These charges result in a surface current, which is similar to the current in a standard n-type conventional MOSFET.

Junctionless dual material surrounding gate MOSFET has been proposed and its surface potential is modelled by using parabolic approximation method. This surface potential is compared with the central potential of the (JLDMSG) MOSFET.A cross sectional view of the Junctionless dual material surrounding gate (JLDMSG) MOSFET is shown in fig 1.

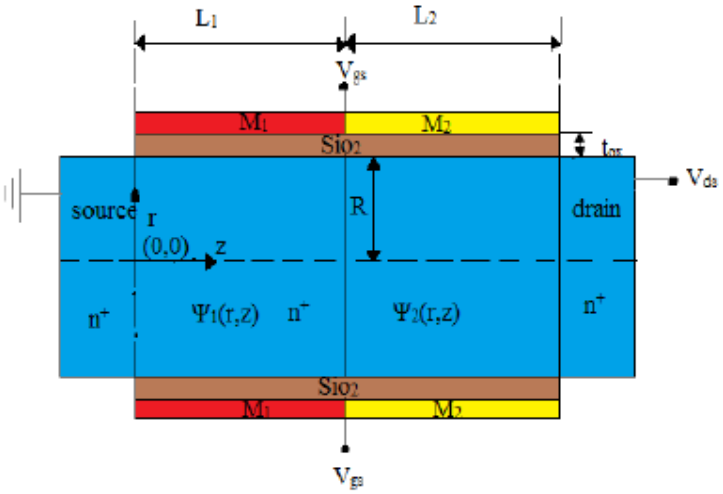

Figure 1. Cross sectional view of junctionless dual material surrounding gate MOSFET(JLDMSG)

In the gate structure the channel region has been divided into two parts. The length of the two metals M1 and M2 are L1 and L2 respectively. A cylindrical co-ordinate system is employed with the radial direction represented as r and a horizontal direction as z. The symmetry of the structure ensures that the potential has no variation with the angular in plane of the radial direction. Hence, a 2-D analysis is sufficient.

2. MODEL DERIVATION

The surface potential distribution in the silicon can be derived by solving 2D poisson's equation. The potential distribution across the two channel is defined as,

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial}{\partial r}\phi_i(r,j)\right)+\frac{\partial^2\phi_i(r,z)}{\partial z^2}=\frac{-qn_d}{\varepsilon_{si}} \qquad i=1,2 \ (1)$$

n_d is the channel doping density, it is assumed to be uniform for simplicity. Parabolic approach is used to define the potential across the surface and the solution is given as,

$$\phi_i(r,z)=c_1^i(z)+c_2^i(z)r+c_3^i(z)r^2 \qquad i=1,2 \ (2)$$

The total length of the gate is given as L1+L2. The metal M1 lies at the region $0 \le z \le L_1$, $0 \le r \le R$ and the metal M2 lies at the region $0 \le z \le L1 + L2$, $0 \le r \le R$. The boundary condition used to find the solutions are,

Electric flux between the silicon body and surrounding gate oxide must be continuous,

$$\frac{\partial \phi_i(z)}{\partial r}\Big|_{r=R} = \frac{c_{ox}(v_{gs} - v_{fbi} - \phi_s(z))}{\varepsilon_{si} t_{si}} \qquad \text{i=1,2 (3)}$$

Electric field at r=0 must be zero due to the symmetry of the channel potential along the r-direction,

$$\frac{\partial \phi_i(z)}{\partial r}\Big|_{r=0} = 0 \qquad \text{i=1,2 (4)}$$

Thus the potential distribution is given as,

$$\phi_i(z) = \phi_c(z) + \frac{c_{ox}(v_{gs} - v_{fbi} - \phi_s(z))}{\varepsilon_{si} t_{si}} r^2 \qquad \text{i=1,2 (5)}$$

Where Vfbi is the flat band voltage, ε_{si} is the permittivity of the silicon, t_{si} is the thickness of the silicon and c_{ox} is the capacitance of oxide per unit area. The flat band voltage is given as,

$$v_{fbi} = \phi_m^i - \phi_{si} \qquad (6)$$

Where ϕ_m^i is the work function of the metal surface M1 and M2. ϕ_{si} is the work function of the silicon and it is given as,

$$\phi_{si} = \chi_{si} + \frac{E_g}{2q} - \phi_f \qquad (7)$$

Where

$\phi_f = \frac{kT}{q} \ln\left(\frac{n_d}{n_i}\right)$ is the bulk potential, Eg is the silicon band gap and ni is the intrinsic concentration. It is assumed that the central potential and the surface potential must satisfy the following condition,

$$\phi_s^i(z) = \phi_c^i(z) + \frac{c_{ox} t_{si}(v_{gs} - v_{fbi} - \phi_s^i)}{4\varepsilon_{si}} \qquad \text{i=1,2 (8)}$$

By substituting equation (5) and (8) in (1) and by eliminating central potential, the differential equation for the surface potential can be expressed as,

$$\frac{\partial^2 \phi_s^i(z)}{\partial z^2} - \lambda^2 \phi_s^i(z) = \phi_{gi} \qquad \text{i=1,2 (9)}$$

Where

$\lambda^2 = \frac{4c_{ox}}{\varepsilon_{si} t_{si}}$ is the scaling factor and $\phi_{gi} = \frac{4(qn_d \varepsilon_{si} t_{si} - 4c_{ox}(v_{gs} - v_{fbi} - \varepsilon_{si})}{4\varepsilon_{si}^2 t_{si} + \varepsilon_{si} t_{si} c_{ox} - 4\varepsilon_{si} c_{ox}}$ i=1,2 (10)

The general solution of the ordinary differential equation in (9) can be expressed as,

$$\phi_s^i(z) = a_i e^{\lambda z} + b_i e^{-\lambda z} - \frac{\phi_{gi}}{\lambda^2} \qquad \text{i=1,2 (11)}$$

Where a_i and b_i are coefficients that are determined by the following boundary conditions [10], Surface potential at the interface of the two dissimilar metals is continuous

$$\phi_s^1(z, L_1) = \phi_s^2(z, L_1) \qquad (12)$$

Electric flux between two dissimilar metals is continuous

$$\frac{\partial \phi_s^1(z, z)}{\partial z}\Big|_{z = L_1} = \frac{\partial \phi_s^2(z, z)}{\partial z}\Big|_{z = L_1} \qquad (13)$$

The potential at the source end is

$$\phi_s^1(z, z = 0) = v_{bi} \qquad (14)$$

The potential at the drain end is

$$\phi_s^2(z, z = L_1 + L_2) = v_{bi} + v_{ds} \qquad (15)$$

With these boundary condition a_i and b_i are obtained as,

$$a_1 = \frac{2\lambda^2 v_{bi} + 2\lambda^2 v_{ds} - \phi_{g2} e^{\lambda L_2} + \phi_{g1} e^{\lambda L_2} + 2\phi_{g2} - 2\lambda^2 b_2 e^{-\lambda(L_1 + L_2)}}{2\lambda^2 e^{\lambda(L_1 + L_2)}} \qquad (16)$$

$$b_1 = v_{bi} + \frac{\phi_{g1}}{\lambda^2} - a_1 \qquad (17)$$

$$a_2 = \frac{v_{bi}\lambda^2 + v_{ds}\lambda^2 + \phi_{g2} - \lambda^2 b_2 e^{-\lambda(L_1+L_2)}}{\lambda^2 e^{\lambda(L_1+L_2)}} \tag{18}$$

$$b_2 = \frac{\begin{array}{l} 2\phi_{g2}e^{\lambda(L_1+L_2)} - 2\phi_{g1}e^{\lambda(L_1+L_2)} + 4\lambda^3 v_{bi}e^{\lambda L_2} + 4\lambda\phi_{g1}e^{\lambda L_2} - 4\lambda^3 v_{bi}e^{-\lambda L_1} - 4\lambda^3 v_{ds}e^{-\lambda L_1} \\ + 2\lambda\phi_{g2} - 2\lambda\phi_{g1} - 4\phi_{g2}\lambda e^{-\lambda L_1} \end{array}}{4\lambda^3 e^{-\lambda L_1} 2\sinh\lambda(L_1 + L_2)} \tag{19}$$

The electric field distribution of the junctionless dual material surrounding gate is obtained by differentiating equation (11) with respect to channel direction z and it is obtained as,

$$\frac{\partial \phi_s^1(z)}{\partial z} = \lambda a_1 e^{\lambda z} - \lambda b_1 e^{-\lambda z} \tag{20}$$

$$\frac{\partial \phi_s^2(z)}{\partial z} = \lambda a_2 e^{\lambda z} - \lambda b_2 e^{-\lambda z} \tag{21}$$

3. RESULT AND DISCUSSION

The analytical modelling of surface potential in junctionless dual material surrounding gate MOSFET is plotted for various parameter and it is compared with the central potential of the JLDMSG MOSFET[11]. The surface potential is defined as the electrostatic potential energy of surface confined charges between source and drain. Central potential is examined by considering a threshold at the middle of the channel region. Thus the surface potential plot is compared with the central potential and analysed its performance. The surface potential of a Junctionless dual material MOSFET surrounding gate is shown in Figure 2.

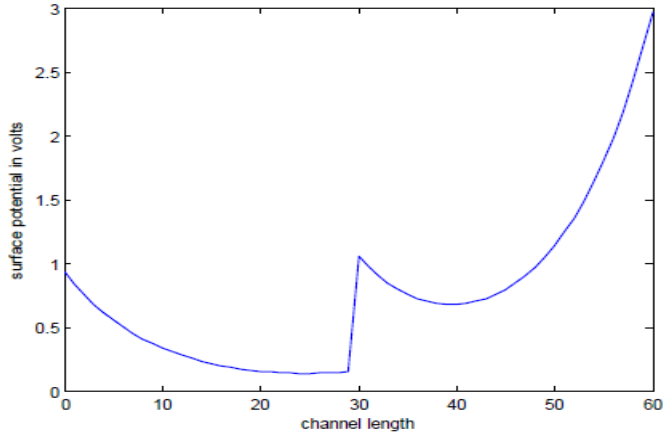

Figure 2. Surface potential versus channel length for JLDMSG MOSFET

From Figure 2.It is clear that surface potential of JLDMSG MOSFETs increases as the channel length increases. In this modelling, the length of the first metal L1 is 30nm and the length of the second metal L2 is 30nm. Thus the surface potential response has a step up at 30nm and then it gradually increases as the channel length increases. This infers that the SCE is reduced and the gate material at the drain side acts like a screening gate.

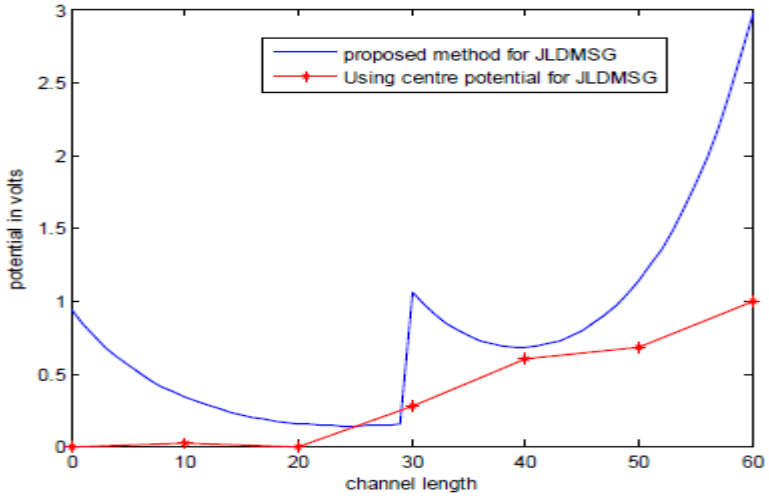

Figure 3. Comparison of the central potential and surface potential in JLDMSG MOSFET for different channel length

In Figure 3. The central potential method is compared with the surface potential of the proposed method for different channel length. The maximum potential at surface of the source and drain is 3v and the central potential is only approximately 1v. From this graph it is obvious that the surface potential is better compared to the central potential that is obtained by considering a virtual cathode at the middle of the channel.

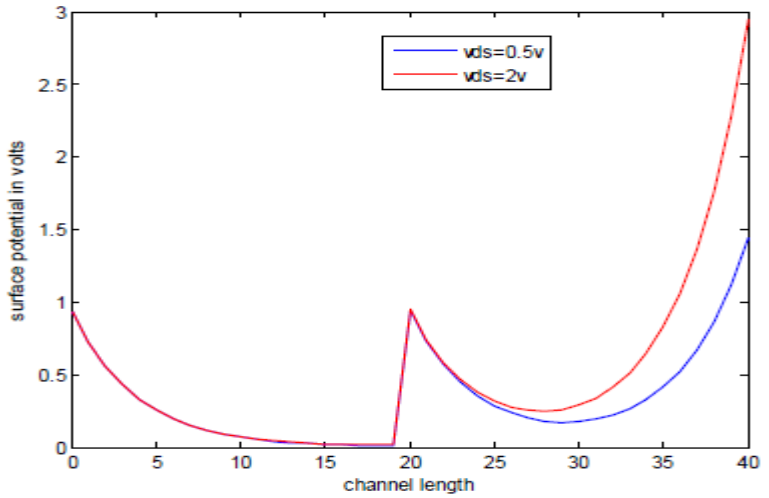

Figure 4. Surface potential of JLDMSG MOSFET versus channel length for different vds

In figure 4.The analytical model values of surface potential versus effective channel is plotted for different V_{ds} value. It is observed that V_{ds} is directly proportional to surface potential. For V_{ds} 0.5v the surface potential response is smaller compared to that obtained for the V_{ds} value 2v. When the drain to source voltage increases the surface potential variation in the drain side also increases.

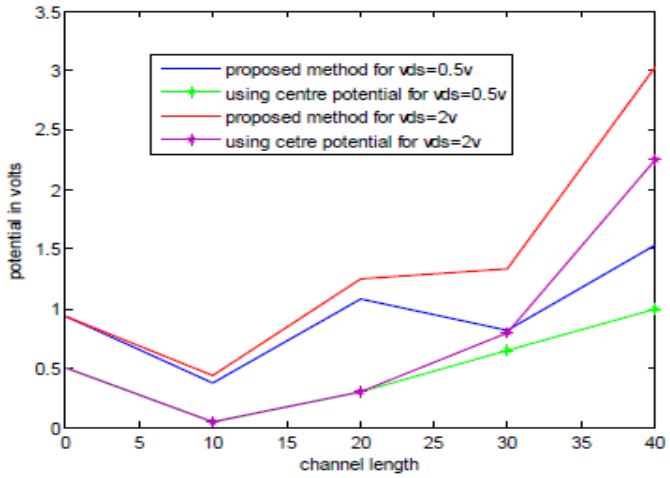

Figure 5. Comparision of the central potential and surface potential in JLDMSG MOSFET for different v_{ds} value

In figure 5. The central potential and surface potential is plotted for different v_{ds} value. It is observed that the surface potential is higher than the central potential for both the v_{ds} values. In this graph the total length of the channel is considered as 40nm. The potential changes are observed at every 10nm. Hence the proposed method shows better performance than the existing method.

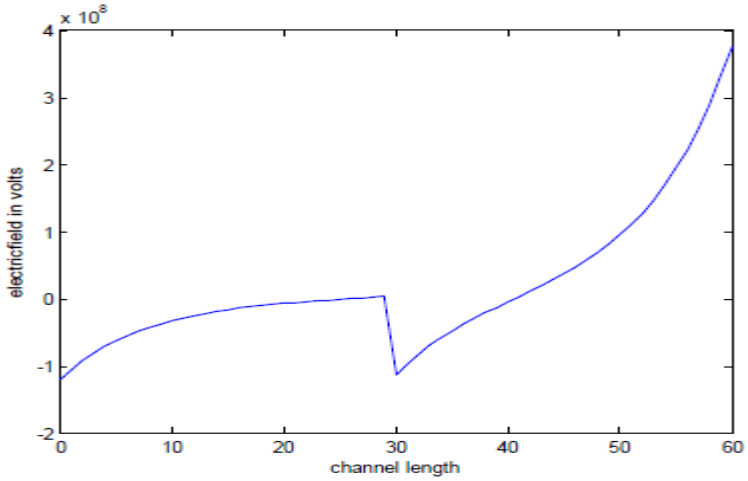

Figure 6. Electric field distribution of JLDMSG MOSFET versus channel length

In Figure 6.The electric field distribution is plotted against channel length. It is clearly observed that for dual material the electric field distribution shows a good step down at 30nm and then increase for the second metal. Thus the electric field of the dual material junctionless surrounding gate MOSFETs shows a good response with high values.

4. CONCLUSION

The Junctionless dual material Surrounding Gate (JLDMSG) MOSFETs show higher performance compared to Junction MOSFETs. The result compares the surface potential of the proposed method with the central potential method of the JLDMSG MOSFET .It is clear from the graph that surface potential of the proposed method is higher than the central potential method. The result also infers that the electric field produced in Junctionless MOSFET shows that it has reduced SCEs compared to other devices in the literature. It proves that there is a reduction in SCEs and DIBL and it is more advantageous than other devices especially Junction based devices.

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