A 20 Gb/s INJECTION-LOCKED CLOCK AND DATA RECOVERY CIRCUIT

Sara Jafarbeiki[1], Dr Khosrow Hajsadeghi[2] and Naeeme Modir[3]

[1,2]Department of Electrical Engineering, Sharif University of Technology, Tehran, Iran
[3]School of Electrical and Computer Engineering, University of Tehran, Tehran, Iran

ABSTRACT

This paper presents a 20 Gb/s injection-locked clock and data recovery (CDR) circuit for burst mode applications. Utilizing a half rate injection-locked oscillator (ILO) in the proposed CDR circuit leads to higher speed operation and lower power consumption. In addition, to accommodate process, voltage, and temperature (PVT) variations and to increase the lock range, a frequency locked loop is proposed to use in this circuit. The circuit is designed in 0.18 µm CMOS and the simulations for 2^7-1 pseudo random bit sequence (PRBS) show that the circuit consumes 55.3 mW at 20 Gb/s, while the recovered clock rms jitter is 1.1 ps.

KEYWORDS

Clock and data recovery, eye diagram, injection-locked, lock range, oscillator

1. INTRODUCTION

For the burst-mode applications such as passive optical network (PON) [1, 2], the CDR circuit in the receiver must lock to each burst data packet very quickly. In a PON system, the optical line termination (OLT) receives data packets from various optical network units (ONUs) and these data packets have different phase and amplitude, so immediate clock extraction and data retiming in the CDR circuit is necessary.

The conventional PLL-based CDR circuit requires a long sequence of bits to settle, hence is not suitable for burst-mode applications. Fast locking capability of open-loop CDR circuits [3]-[8] makes them attractive solutions for these applications. However, open loop CDRs suffer from limited frequency tracking range and high jitter transfer [9]. Jitter transfer is not a serious issue for applications where no repeater is required [3], hence, open-loop CDRs are appropriate for such applications.

In open-loop CDR circuits, a gated voltage-controlled oscillator (GVCO) [3]-[5] or an injection-locked oscillator (ILO) [6]-[8] can usually be used. GVCOs have higher phase noise than LC VCOs because of their ring structure. So, using GVCO, in general, leads the recovered clock showing larger jitter than using ILO. Also the operation speed of GVCOs is lower than ILOs [5]. An injection-locked oscillator uses an LC type VCO which has better phase noise and higher operation speed in comparison with ring oscillator.

A CDR circuit using injection-locking technique is described in [6], in which using two cascaded voltage-controlled LC oscillators as a full-rate CDR forces the use of an edge detector circuit. Both VCOs are injection-locked to the input data and the edge detector design needs high speed

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current mode logic (CML) XOR and delay buffer circuits. Also the reference PLL which is used to overcome the process, supply voltage, and temperature (PVT) variations consists of a VCO which must be an exact duplicate of the main VCOs, otherwise the PLL provides an inaccurate control voltage which is not suitable to use for main VCOs. In this paper, a high speed injection-locked CDR is proposed which has several advantages over current designs. Utilizing a novel injection-locked oscillator structure and using an appropriate injection method in the proposed CDR circuit leads to higher speed operation by eliminating the edge detector circuit and by sampling the data with a half rate clock. In addition, a new approach instead of a reference PLL is proposed to accommodate PVT variations which forces the free-running frequency of the ILO to track the data rate by adding or removing some of the utilized capacitors to the ILO structure. A 20 Gb/s open-loop CDR circuit is designed and simulated in 0.18 µm CMOS technology for burst-mode applications, which consumes less than 55.3 mW from a 1.8 V supply.

The rest of the paper is organized as follows. Section II describes the CDR topology and architecture. Section III presents the building blocks utilized in the circuit. Section IV describes the simulations and summarizes the results, and finally section V concludes the paper.

2. THE PROPOSED CDR

Figure. 1 shows the proposed CDR architecture. The circuit is composed of an injection-locked LC oscillator, a clock buffer and two retiming flip flops. In addition, to track the frequency of oscillator a divider chain, a frequency detector (FD), and a counter are used in this structure. Input data is injected to the ILO to provide an aligned clock. The recovered clock is applied to a clock buffer which in turn drives two flip flops in the decision circuit to recover the data.

As the injection locking technique has narrow locking range, the ILO may not lock to the frequency of the incoming data stream if it is not properly controlled. Furthermore, the PVT variations may also cause ILO to lose lock. In the proposed architecture a frequency locked loop is used to compensate for these problems. The clock frequency is divided by 40 and then applied to a frequency detector as shown in Fig. 1. In the frequency detector, this signal is compared to a reference frequency of 250 MHz. The frequency detector produces an output based on whether $f_{ref} > f_{divider}$ or not. This signal is then applied to a counter as to determine up or down counting. The frequency detector circuit also produces another signal whose frequency is dependent on the difference between f_{ref} and $f_{divider}$. This signal is applied to the counter as its clock and it determines the speed of counting. Thus, counter can count up or down depending on the frequency of ILO in comparison to the reference frequency and then add some capacitors to ILO or remove them from it. The counter does this through the control of a few switches which are connected to the capacitors. By using this method the lock range of the circuit is increased considerably.

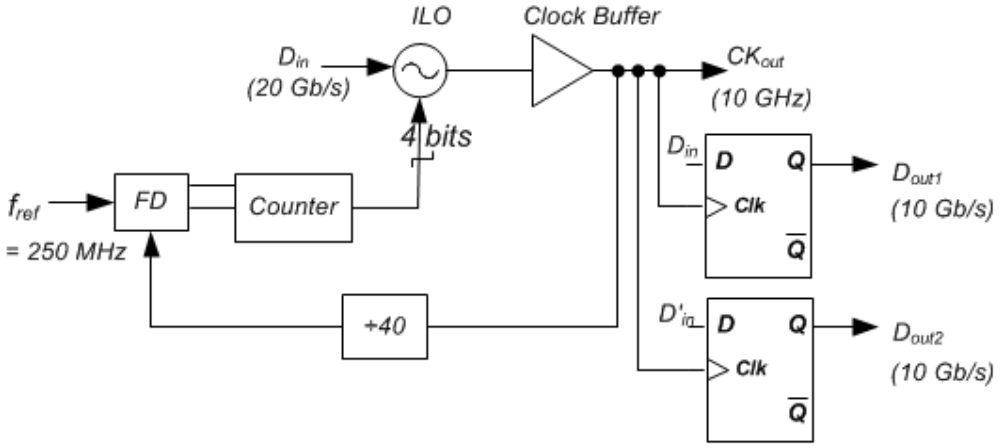
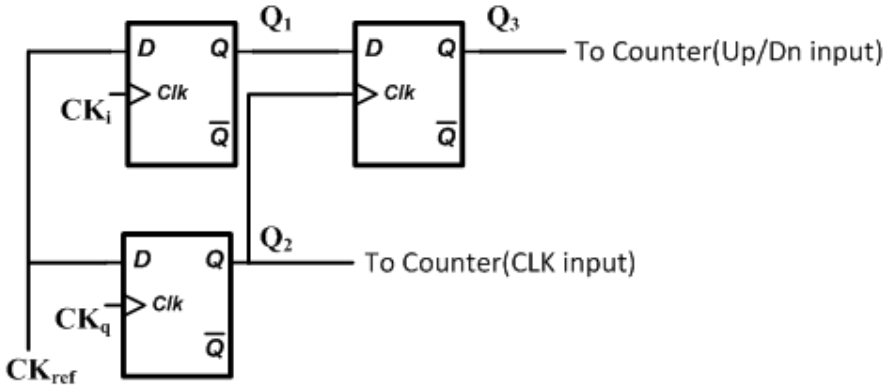


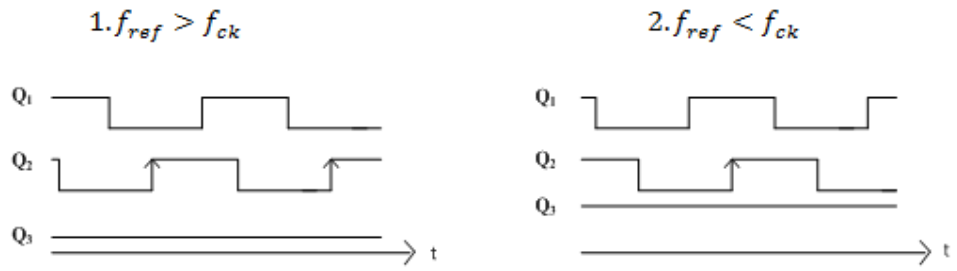
Figure. 1 The Proposed CDR Architecture

2.1. Frequency tracking

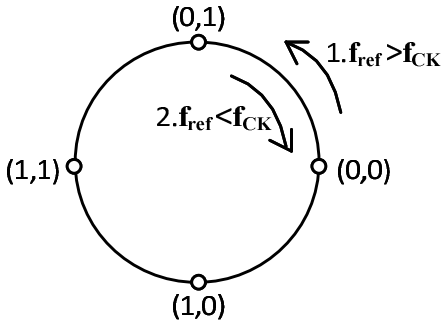
As locking range of the ILO is narrow, a frequency locked loop (FLL) is required to set the oscillator frequency in the locking range. We propose a method to track the oscillator frequency and bring it within the appropriate range. The proposed FLL uses a divider chain, a frequency detector and an up/down counter. The output frequency of the oscillator is divided by 40 and then is applied to a frequency detector. The frequency detector circuit is shown in Figure. 2 which is a rotational frequency detector circuit [10]. It compares the divider output frequency with a reference frequency of 250 MHz and produces an up/down signal and a clock for the counter. In this circuit the ILO output clock which is composed of CK_i and CK_q, are sampled by the reference clock, producing two outputs Q_1 and Q_2. Leading or lagging of Q_1 from Q_2 shows the polarity of the frequency error (fig. 2(b)). The FD's output, Q_3, is applied to the counter and forces the counter to count up or down depending on the frequency error's polarity. Fig. 2(c) shows the states of Q_1 and Q_2, where the sign of beat frequency is indicated by the rotating direction.



(a)



(b)



(c)

Figure. 2 (a) Frequency detector circuit. (b) FD operation. (c) States of (Q_1, Q_2) [10]

3. BUILDING BLOCKS

3.1. ILO

Fig. 3 shows the designed super harmonic injection-locked LC oscillator which is used as a half rate CDR circuit in this paper. In this structure the data is injected into the ILO directly, instead of applying it to an edge detector. The M1 and M2 create an incident current at the rising and falling edge of the data, respectively. As a result, at every edge of the data the differential output of the oscillator will be shorted. The main advantages of this structure are low power consumption and the reduction of the maximum operational frequency to half of the other state of the art structures in the literature.

As mentioned before, capacitors with switches are incorporated in the ILO to overcome PVT variations. By switching these capacitors in or out of the ILO structure, the ILO's output frequency is brought to its locking range. So, the ILO can lock to the injected input data.

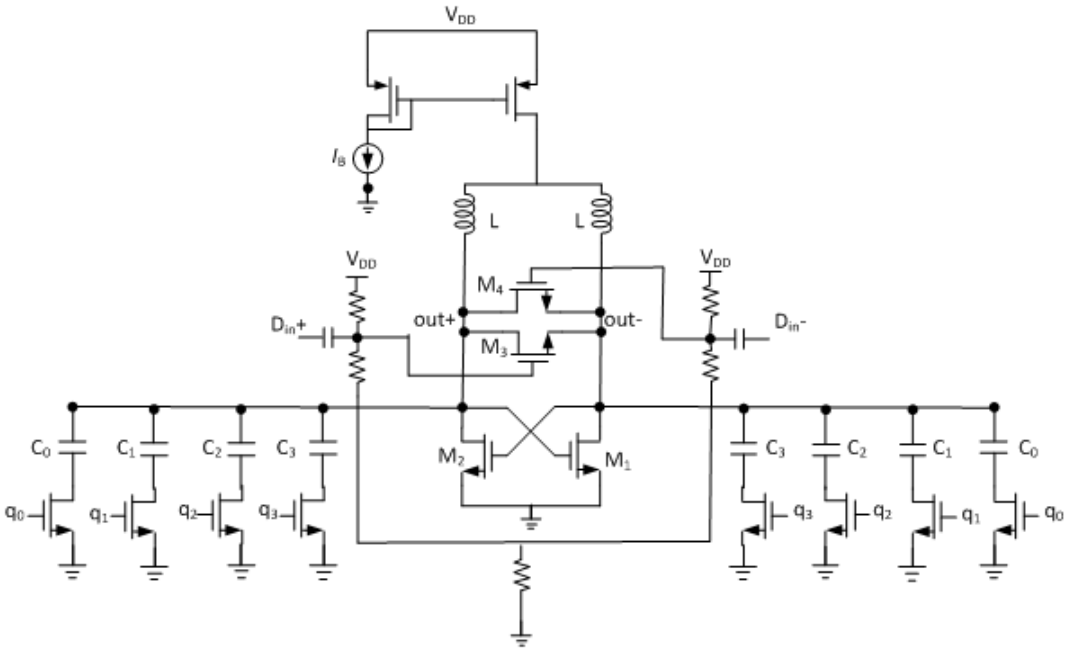


Figure. 3 Injection-locked LC oscillator with utilized capacitors

Since the lock range for this ILO is around 150MHz, the frequency shift in ILO's output frequency for each added or removed capacitor is designed to be 100 MHZ. The capacitor values can be calculated from the following equation.

$$f_{out} = \frac{1}{\sqrt{LC_{eq}}} = \frac{1}{\sqrt{L(C_0 + \Delta C)}} = \frac{1}{\sqrt{LC_0(1+\frac{\Delta C}{C_0})}} = f_0 \frac{1}{\sqrt{(1+\frac{\Delta C}{C_0})}} \quad (1)$$

Where f_{out} is the ILO output frequency, f_0 is the ILO free-running frequency, C_{eq} is the total capacitance, C_0 is parasitic capacitance of ILO, and ΔC is the capacitance value change for each step of counting. For example, when the counter has the value of three, the transistors q_0, q_1 are on and the capacitors C_1, C_2 are connected to the ILO. When the counter counts up and changes to four, the transistors q_0, and q_1 turn off and q_2 turns on hence, the capacitors C_3 are connected to the ILO. So, for this step of counting $\Delta C=C_3-(C_1+C_2)$. The values of C_1, C_2, C_3, C_4 are chosen such that the change in the value of capacitors connected to the ILO for each step of counting, ΔC, to be constant.

$$f_{out} \cong f_0 \frac{1}{\left(1+\frac{\Delta C}{2C_0}\right)} = f_0 - f_0 \frac{\Delta C}{2C_0} \quad (2)$$

$$\Rightarrow \frac{\Delta f}{f_0} = \frac{\Delta C}{2C_0} \quad (3)$$

It is clear that the capacitors values can be calculated easily for a certain frequency shift and a given free-running frequency of ILO.

3.2. Clock buffer

In order to isolate the capacitive loading of the next stage on the ILO, we use the clock buffer which is shown in Fig. 4. The bandwidth limitation in conventional CML buffers with resistive

loads leads to limited output voltage swings. In order to increase signal swing and to solve the bandwidth limitation problem, we can use the inductive peaking technique. We choose the inductor and resistor values to adjust the buffer delay such that the phase difference between the input data and the clock to be equal to 90˚and, as a result the clock edges align with the center of the input data eye.

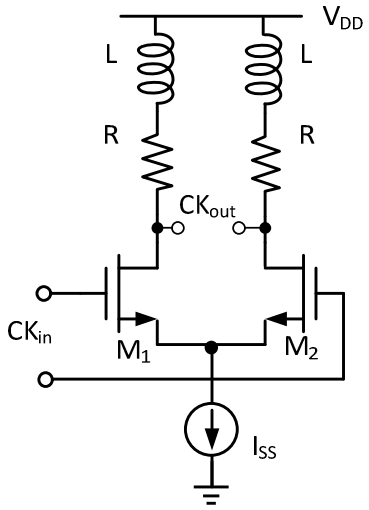


Figure. 4 Clock buffer

3.3. Flipflop

We can classify flipflops into two categories: static and dynamic. Although the static latches can operate in higher speeds, they consume more power in contrast to their dynamic counterparts. We use the static flipflops only in situations that we need the fast operation, such as decision circuits and first stages of divider. The dynamic flipflops are used in all other situations, such as next stages of the divider and frequency detector circuit, to reduce the power consumption. The details of these two types of flipflops are described as follows.

3.3.1. Static Flipflop

The CML topology is used in our design because it can speed up the operation to some extent. The CML circuit operation is fast, because they have lower output voltage swing compared to the static CMOS circuits. We also use inductive peaking technique similar to [11, 12] which improves the speed of CML circuits by extending the bandwidth.
Fig.5 shows the designed CML latch circuit.

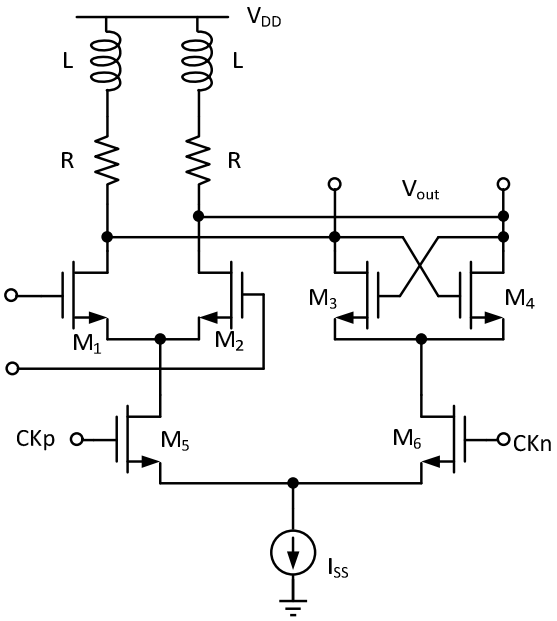


Figure. 5 The designed CML latch circuit

3.3.2. Dynamic Flipflop

As mentioned before, the dynamic flipflop shown in Fig. 6 is used to reduce the power consumption in situations where we do not need fast operation speed [13].

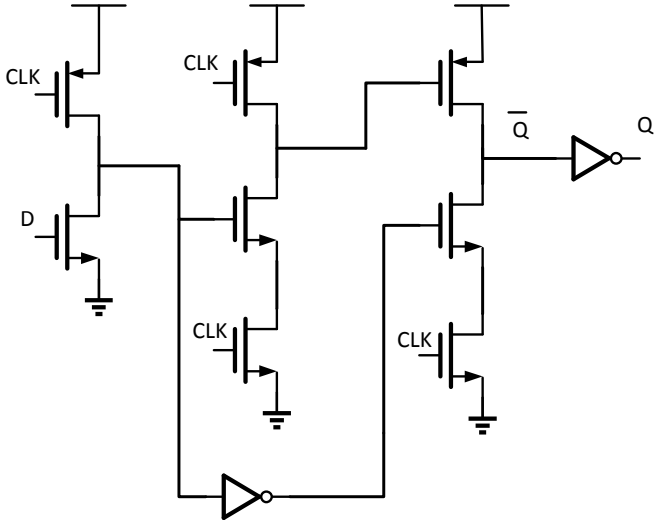


Figure. 6 Dynamic latch circuit

We have also depicted a dynamic divider in Fig. 7 which is used in the next stages of the divider chain. This dynamic divider consumes less power than CML ones. This structure is made of two consecutive D flipflops which are dynamic latches that sample the data in every rising edge of the clock.

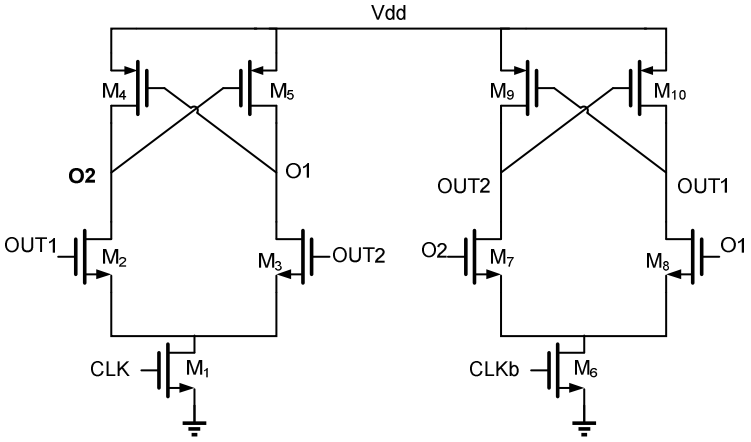


Figure. 7 Dynamic divider

3.4. Counter circuit

For turning the switches, used in the injection locked oscillator, on and off, a 4-bit up/down counter is utilized which is shown in Fig. 8 [14] This counter receives its clock and control inputs, which determines the up or down counting state, from the frequency detector circuit.

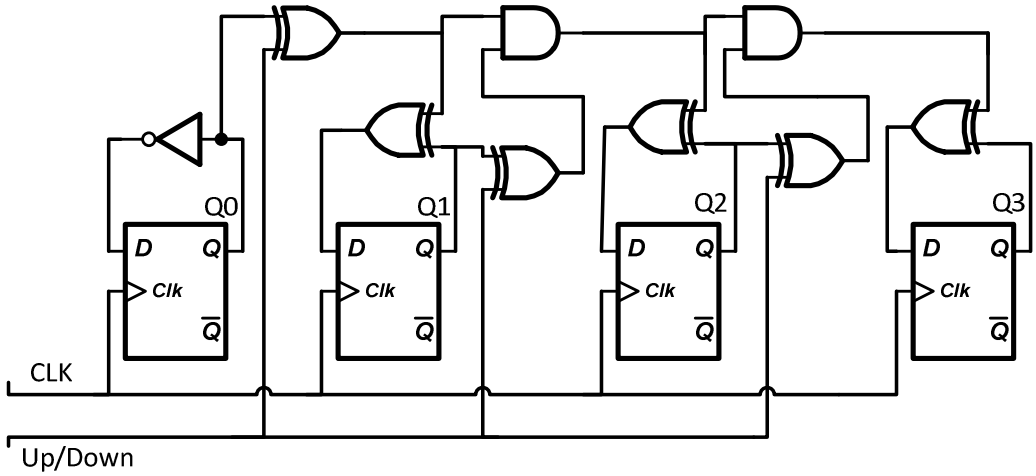


Figure. 8 Up/Down Counter circuit [14]

4. SIMULATION RESULTS

The proposed circuit has been designed and simulated in a 0.18 µm CMOS technology. This circuit consumes 55.3mW from a 1.8V supply voltage, where the most of it is consumed in the CML circuits. The input data is shown in Fig. 9 and the recovered data in response to a 2^7-1 continuous mode PRBS is shown in Fig. 10. The simulated jitter values for the recovered data are 6 ps, pp and 1.3 ps, rms. The recovered clock is shown in Fig. 11. The simulated peak-to-peak and rms jitters for the recovered clock are 4.8 ps and 1.1ps, respectively. The ILO locking range of 150MHz is achieved. By using the frequency locked loop, the locking range of the CDR circuit is extended to 1.5 GHz. The CDR circuit recovers the data in less than 50 ps which is equal to 1 bit. Fig. 12 shows this fast locking time.

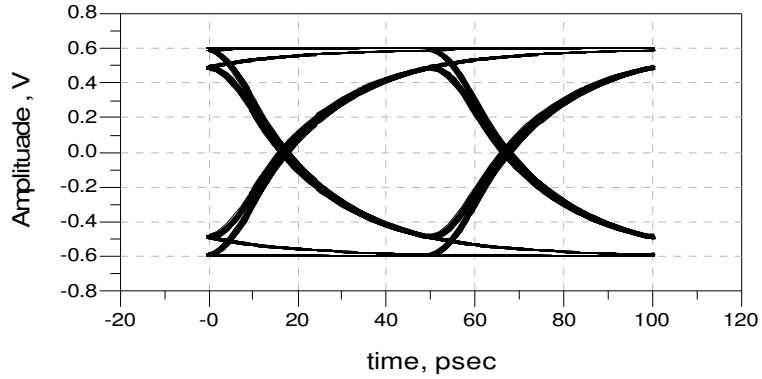


Figure. 9 Data eye diagram at the CDR input

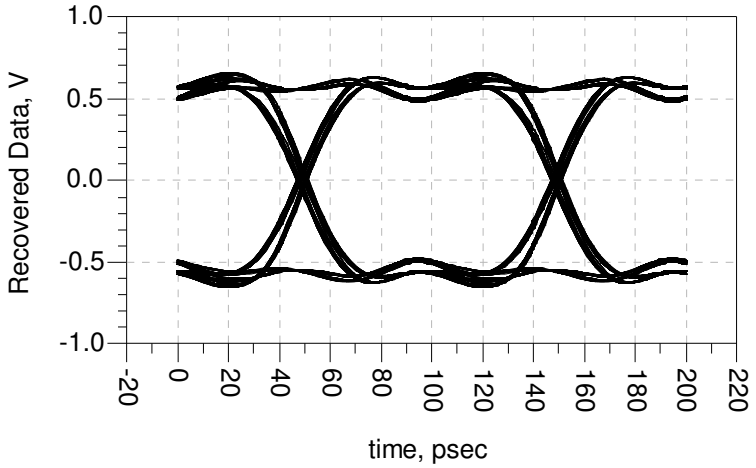


Figure. 10 Data eye diagram at the receiver output

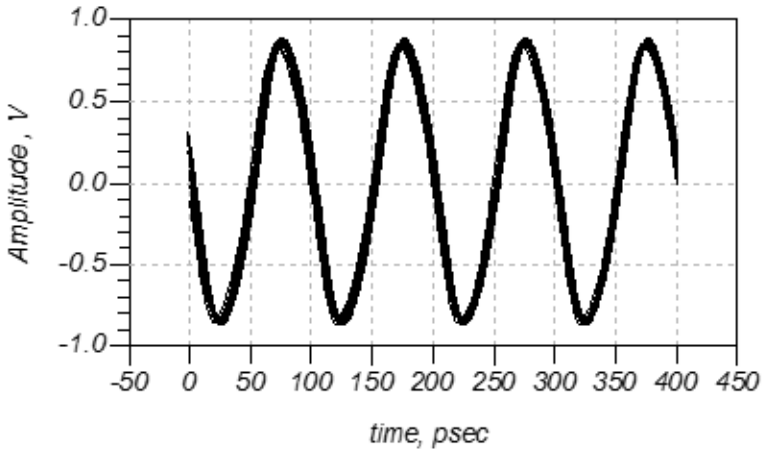


Figure. 11 Recovered clock with 2^7-1 PRBS input data

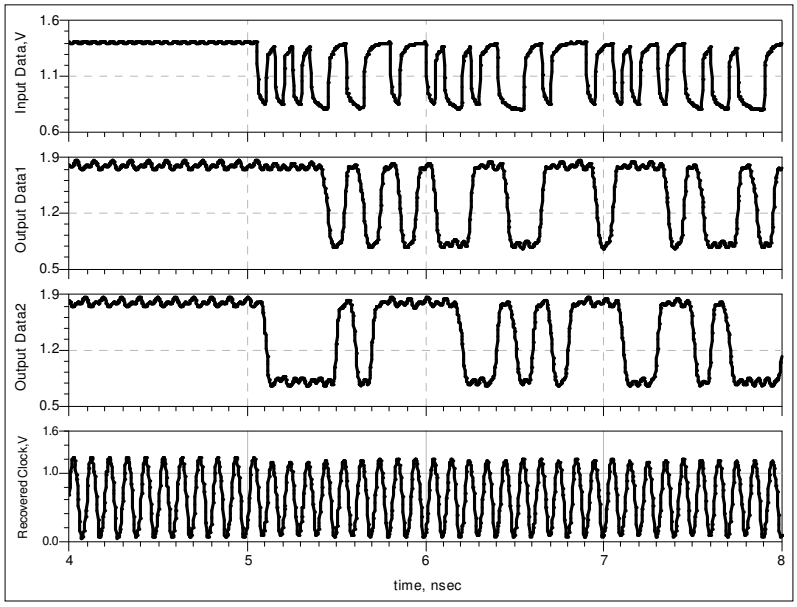


Figure. 12 Simulated input and output waveforms

Fig.13 depicts the FD outputs, and it shows that when the ILO locks to the input data the FD does not create any clock pulses for the counter. It means that after lock, the CLK becomes constant, hence the counter does not count anymore and it shows that the CDR circuit is locked to the input data.

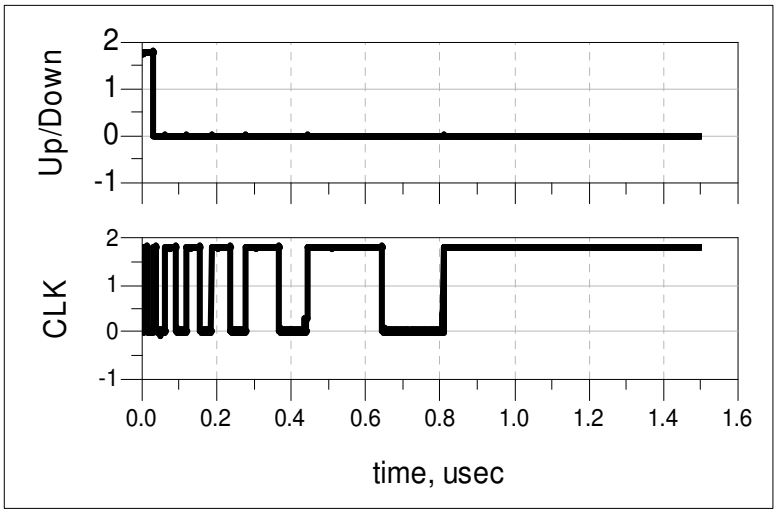


Figure. 13 FD output waveforms

The circuit is simulated in different process corners, temperatures and supply voltages. At the slow/slow process corner, 70◦ C and 1.65V, the rms jitter of the recovered clock is 1.33 ps. The consumed power in this situation is 47 mW and the circuit locks after 1 bit. At the fast/fast corner, −20◦ C and 1.95 V, the rms jitter of the recovered clock is 1.12 ps and the consumed power is 70.2mW and the circuit locks after 1 bit.

Table 1 summarizes and compares the performance of this work and some other burst mode CDRs recently published. The operation range and the speed of the proposed circuit, while it uses a technology of 0.18µm CMOS, have been improved over recently reported structures.

Table 1. The simulation result of the proposed CDR compared with similar work

	[6]	**[15]**	**[16]**	**[17]**	**[18]**	**This work**
Data rate	20 Gb/s	10 Gb/s	71 Gb/s	1.3-5.2 Gb/s	30 Gb/s	20 Gb/s
Recovered clock jitter	1.2 ps.rms (with 2^7-1 PRBS)	8.5 ps.rms (with 2^7-1 PRBS)	N/A	0.82 ps.rms (with 2^7-1 PRBS)	4 ps.rms	1.1 ps.rms (with 2^7-1 PRBS)
Operation range	800 MHz	600 MHz	N/A	N/A	N/A	1.5 GHz
Locking time	1 UI	< 5 UI	N/A	< 20 UI	N/A	1 UI
Supply voltage	1.5	1.8	3.3	1.1	N/A	1.8
Power Diss.	175 mW	36 mW	0.5 W	12.4 mW	210 mW	55.3 mW
Technology	90 nm CMOS	0.18 µm CMOS	0.18 µm SiGe	40 nm CMOS	65 nm CMOS	0.18 µm CMOS
Simulation/ Measurement	✓	✓	✓	✓	✓	✓

5. CONCLUSIONS

This work proposes a 20 Gb/s CDR circuit for burst mode applications which is designed and simulated in a 0.18µm CMOS process. The CDR employs a super harmonic injection-locked oscillator, hence frequency of the oscillator is reduced to the half of the bit rate and two flip flops are needed for sampling the data with the half rate clock. With the help of the proposed frequency tracking technique, the circuit accommodates frequency deviations caused by PVT variations. In fact, the simulation results demonstrate that the CDR circuit provides a truly wide operation range (1.5GHz) with reasonably low power consumption.

REFERENCES

[1] ''G.984.2 Gigabit-capable passive optical networks (GPON): Physical media dependent (PMD) layer specification'', ITU-T, 2003.

[2] C. Liang and S. Liu, "A 20/10/5/2.5Gb/s Power-scaling Burst-Mode CDR Circuit Using GVCO/Div2/DFF Tri-mode Cells," ISSCC Dig. Tech. Papers, pp. 224-608, Feb., 2008.

[3] P. Han and W. Y. Choi, "1.25/2.5-Gb/s dual bit-rate burst-mode clock recovery circuits in 0.18-□m CMOS technology," in IEEE Transactions on Circuits and Systems-II: Express Briefs, vol. 54, pp. 38-42, Jan. 2007.

[4] M. Nogawa et al., "A 10 Gb/s burst-mode CDR IC in 0.13 μm CMOS," in IEEE ISSCC Dig. Tech. Papers, Feb. 2005, pp. 228–229.

[5] Kaeriyama, S. and Mizuno, M., "A 10Gb/s/ch 50mW 120×130μm clock and data recovery circuit", in Proc. ISSCC, February 2003.

[6] J. Lee, M. Liu, "A 20Gb/s Burst-Mode CDR Circuit Using Injection-Locking Technique", ISSCC, pp 586, Feb 2007.

[7] M. Tiebout, "A CMOS direct injection-locked oscillator topology as high-frequency low-power frequency divider," IEEE J. Solid-State Circuits, vol. 39, no. 7, pp. 1170–1174, Jul. 2004.

[8] B. Razavi, "A study of injection locking and pulling in oscillators," IEEE J. Solid-State Circuits, vol. 39, no. 9, pp. 1415–1424, Sep. 2004.

[9] M. Hsieh and G. E. Sobelman, "Architectures for Multi-GigabitWire-Linked Clock and Data Recovery,"IEEE Circuits and Systems Magazine, vol. 8, no. 4, pp. 45-57, Fourth Quarter 2008.

[10] Jri Lee and Ke-Chung Wu " A 20-Gb/s Full-Rate Linear Clock and Data Recovery Circuit With Automatic Frequency Acquisition," IEEE Journal of Solid-State Circuits (December 2009), 44 (12), pg. 3590-3602

[11] Terada J, Ohtomo Y, Nishimura K, Katsurai H, Kimura S, Yoshimoto N. Jitter-reduction and pulse-width-distortion compensation circuits for a 10gb/s burst-mode cdr circuit. In: IEEE ISSCC Dig. Tech. Papers. San Francisco; 2009, p. 104 –105,105a.

[12] Y. T. Chen, M. W. Li, T. H. Huang, and H. R. Chuang, "A V-band CMOS direct injection-locked frequency divider using forward body bias technology," IEEE Microw. Wireless Compon. Lett., vol. 20, no. 7, pp. 396-398, Jul. 2010.

[13] B. Razavi, et al., "Design of high-speed, low-power frequency dividers and phase locked loops in deep submicron CMOS," IEEE J. Solid-State Circuits, vol. 30, pp. 101–109, Feb. 1995.

[14] Mircea R. Stan, Alexandre F. Tenca and Milos D. Ercegovac, "Long and Fast Up/Down Counters," IEEE Transactions on Computers, vol., 47, no. 7, July, 1998.

[15] Che-Fu Liang, Hong-Lin Chu, and Shen-Iuan Liu, "10Gbps inductorless CDRs with digital frequency calibration", IEEE Trans. Circuits and Systems-I: Regular Papers, vol. 55, pp. 2514-2524, Oct. 2008.

[16] T. S. Mukherjee, M. Omer, J. Kim, Design and Optimization of a 71 Gb/s Injection-locked CDR. ISCAS 2009: 177-180

[17] K. Maruko, T. Sugioka, H. Hayashi, Zhiwei Zhou, Y. Tsukuda, Y. Yagishita, H.Konishi, T. Ogata, H. Owa, T. Niki, K. Konda, M. Sato, H. Shiroshita, T. Ogura, T.Aoki, H. Kihara, and S. Tanaka, "A 1.296-to-5.184Gb/s Transceiver with 2.4mW/(Gb/s)Burst Mode CDR Using Dual-Edge Injection-Locked Oscillator," ISSCCDig. Tech. Papers, pp. 364-365, Feb. 2010.

[18] Y. Take, N. Miura, and T. Kuroda, "A 30 Gb/s/link 2.2 Tb/s/mm2 inductively-coupled injection-locking CDR for High-Speed DRAM Interface," IEEE Journal of Solid-State Circuits (JSSC), vol. 46, pp. 2552-2558, NOV. 2011.