AN OPERATIONAL AMPLIFIER WITH RECYCLING FOLDED CASCODE TOPOLOGY AND ADAPTIVE BIAISNG

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ABSTRACT

This paper presents a highly adaptive operational amplifier with high gain, high bandwidth, high speed and low power consumption. By adopting the recycling folded cascode topology along with an adaptive-biasing circuit, this design achieves high performance in terms of gain-bandwidth product (GBW) and slew rate (SR). This single stage op-amp has been designed in 0.18μm technology with a power supply of 1.8V and a 5pF load. The simulation results show that the amplifier achieved a GBW of 335.5MHz, Unity Gain Bandwidth of 247.1MHz and a slew rate of 92.8V/μs.

KEYWORDS

Recycling Folded Cascode, Operational Amplifier, slew rate, Adaptive biasing, Transconductance

1. INTRODUCTION

In high performance analog integrated circuits, such as switch-capacitor filters, delta-sigma modulators and pipeline A/D converters, op amps with very high dc gain and high unity-gain frequency are needed to meet both accuracy and fast settling requirements of the systems. However, as CMOS design scales into low-power, low-voltage and short-channel CMOS process regime, satisfying both of these aspects leads to contradictory demands, and becomes more and more difficult, since the intrinsic gain of the devices is limited. [1]

In order to achieve high-gain, the folded cascode amplifier is often adopted as the first-stage of two-stage amplifiers. Actually, in the deep-submicron CMOS technology, high-gain amplifiers are difficult to be implemented because of the inherent low intrinsic gain of the standard threshold voltage MOS transistors. At the same time, because of the reliability reasons in the deep-submicron processes, the output swing of amplifier is severally restricted with the lower power supply voltage. [2]

To efficiently increase operational amplifier's gain and output swing, multi-stage fully-differential operational amplifier topology is appreciated. The operational amplifier with three or even more stages equipped with the Nested-Miller compensation or the Reversed Nested-Miller compensation shows high efficiency in the gain enhancement, while they require additional large compensation capacitors compared to the traditional two-stage operational amplifier, which will lead to a larger die area and the limited slew rate. Besides, additional common mode feedback (CMFB) circuits would consume additional power. [3]

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This paper presents a novel idea of implementing recycling folded cascode [4] along with an adaptive-biasing circuit[5] to achieve high gain, high bandwidth and high slew rate specifications. Section 2 describes the proposed design. Section 3 analyzes the design and working of the circuit. Implementation is discussed in section 4, simulations in section 5, followed by conclusion in section 6.

2. PROPOSED STRUCTURE

The proposed design presented in this paper employees the recycling folded cascode along with an adaptive bias current circuit. This single stage operational amplifier is capable of providing high gain of around 70dB along with a high bandwidth of 250 MHz and a slew rate of around 100V/μs which is approximately twice as that of the recycling folded cascode without the additional adaptive-biasing circuit.

Recycling folded cascode is basically a modified folded cascode where the load transistor also acts as a driving transistor, hence, enhancing the current carrying capability of the circuit. Recycling folded cascode is obtained by splitting the input transistors and the load transistors as given in figure 1. The cross-over connections of these current mirrors ensure that the small signal currents are added at the sources of M1, M2, M3 and M4 and are in phase.

This is called as recycling folded cascode (RFC), as it reuses/recycles the existing devices and currents to perform an additional task of increasing the current driving capability of the circuit.
The proposed modification in the recycling folded cascode topology involves replacing the transistor M0 with an adaptive-biasing circuit (figure 1) [5] which further enhances the current driving capability of this circuit and hence the speed.

2.1 Adaptive Biasing Design

Adaptive biasing circuit consists of two level shifters and a current sources $I_{B.}$ They have a very low output resistance (typically in the range of 20 – 100 ohms). Quiescent current in M1 and M2 is the well-controlled bias current I_B of the level-shifter transistors assuming M1, M2, M1a and M1b are matched.

Since the ac input signal is applied to both the gate and the source terminals of M1 and M2, the transconductance of this input stage is twice as that of a conventional differential pair.

It is clear that for large $V_{in,d}$ the output current increases with it, enhancing quadratically the current boosting. The minimum supply voltage of this circuit is $|V_{TH}| + 3|V_{DS,sat}|$ where $|V_{DS,sat}|$ is the minimum $|V_{DS}|$ for operation in saturation region. For $|V_{TH}| = 0.7V$ and $|V_{DS,sat}| = 0.2$ V, it yields 1.3V. Hence, the circuit is suitable for low voltage operations.

3. ANALYSIS AND DESIGN OF THE PROPOSED STRUCTURE

3.1 Low Frequency Gain

The open loop gain of an operational amplifier determines the precision of the feedback systems employing it. A high open loop gain is a necessity to suppress linearity [6]. The low frequency gain of OTAs is frequently expressed as the product of the small signal transconductance, Gm and the low frequency output impedance, Ro. The low frequency gain of the adaptive recycling folded cascode is almost the same as that of the recycling folded cascode topology, i.e.

$Ro_{ARFC} \approx gm_{16}r0_{16}\ (ro_4 \| ro_{10}) \| gm_{14}ro_{14}ro_{12}$ (1)

$Gm_{ARFC} \approx Gm_{RFC}\ (=gm_1(1+K)\ )$ where K=3 (2)

Both the RFC and adaptive RFC (ARFC) have similar noise injection gains from either supply. Although there is no discernable change in low frequency gain but extended bandwidth of the adaptive RFC ensures high GBW. Moreover, the extended GBW of the adaptive RFC extends the improved PSRR performance to higher frequencies than the RFC.

3.2 Phase Margin

The phase margin is often viewed as a good indicator to the transient response of an amplifier, and is determined by the poles and zeros of the amplifier transfer function. The adaptive RFC shares a dominant pole ωp1, determined by the output impedance and capacitive load and a non-dominant pole ωp2, determined by the parasitic at the source of M15/M16. It has a pole-zero pair, ωp3 and ωpz (= (K+1) ωp3), associated with the current mirrors M7:M8 and M9:M10. However, this pole-zero pair is associated with NMOS devices, which puts it at a high frequency. In addition, adaptive RFC also have a pole due to adaptive current source, ωp4. Due to low Impedence at that node it is pushed to a high frequency.

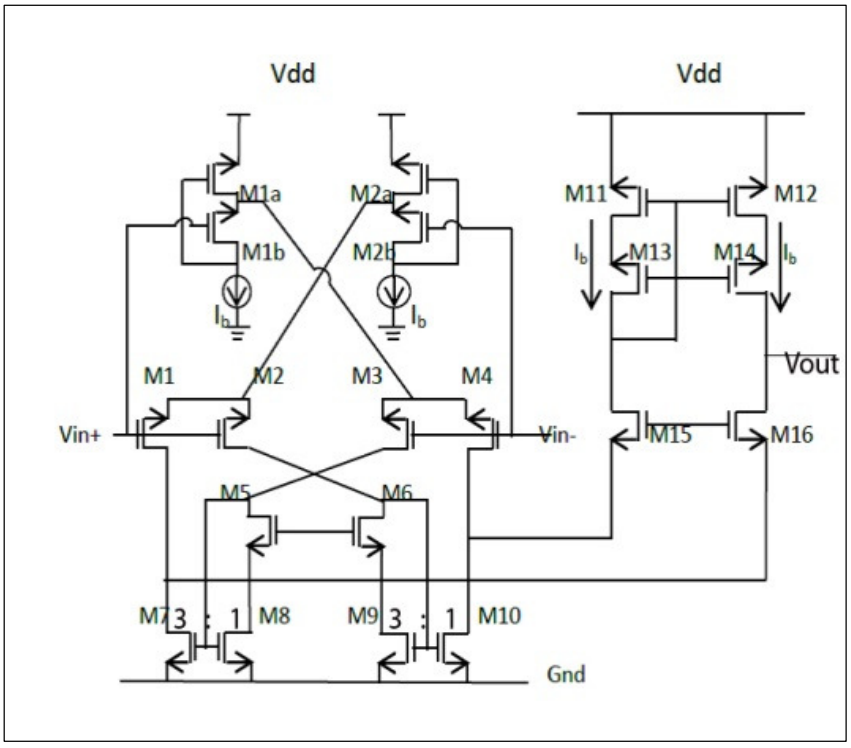

Figure1. Schematic of the proposed design

The pole-zero values from the PZ analysis in cadence virtuoso have been tabulated in Table 1 and Table 2. Also, their positioning with respect to each other is shown in figure 2.

Table1. Pole Analysis

Pole	Real Value
ω_{p1}	-1.267e+05
ω_{p2}	-3.551e+08
ω_{p3}	-5.324e+08
ω_{p4}	-9.908e+08
ω_{z}	-21.296e+08

Table 2. Zero Analysis

Pole	Real Value
ω_{z}	-21.296e+08

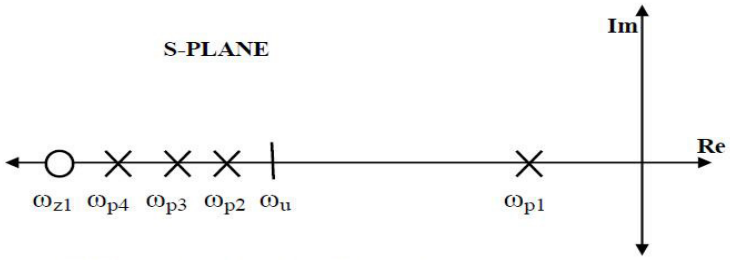

Figure 2. Pole-zero analysis of the proposed design

3.3 Slew Rate

Slew rate is one of the most critical design aspects especially for the kind of circuits where high speed is necessity. To achieve a high slew rate, adaptive biasing circuit plays a vital role. The upper part of the proposed design [5] that is the adaptive biasing circuit consists of four matched transistors M_1, M_2, M_3 and M_4 cross-coupled by two dc level shifters. Each level shifter is built using two transistors (M_{1a}, M_{2a} and M_{1b}, M_{2b}) and a current source. These level shifters are called Flipped Voltage Followers (FVFs). The dc level shifters must be able to source large currents when the circuit is charging or discharging a large load capacitance. Moreover, they should be simple due to noise, speed, and supply constraints.

Analysis of the proposed design shows that there is a significant improvement in its slew rate over the RFC topology. Suppose Vin+ goes high, it follows that M_1 and M_2 turn off, which forces M_9 and M_{10} to turn off. Consequently, the drain voltage of M_9 rises and M_{16} is turned off whereas M_3 is driven into deep triode. This directs current I_d into M_4 and in turn is mirrored by a factor of 3(K) (M_7, M_8) into M_{15}, and again by a factor of 1 into (M_{11}, M_{12}). For simplicity, if we ignore any parasitic capacitance at the sources of $M_{1,2,3,4}$ and follow the similar derivation steps but assuming Vin+ goes low, the result is symmetric slew rate expressed in (3)

$$SR\ (adaptive)_{RFC} = 6I_d/C_L\ [4] \qquad (3)$$

We know that, $I_d = I_D + i_d$ (4)

Due to presence of the adaptive biasing circuit, this circuit changes current according to the input voltage and hence remains self-biased. It also causes minimal increase in power dissipation as the current only increase proportional to the voltage in one branch and correspondingly decreases in the other one.

Since the ac input signal is applied to both the gate and the source terminals of $M_{1,2}$ and $M_{3,4}$, the transconductance of this input stage is twice as that of a conventional differential pair.

The ac small-signal differential current of the input stage is

$$I_d = i_1 - i_2 \approx (1 + (g_{m2A,B}\, r_{oA,B} - 1)/(g_{m2A,B}\, r_{oA,B} + 1)) \qquad (5)$$

Clearly ac small signal current is twice as that in the case of RFC without adaptive biasing circuit. Hence, Slew rate has improved in the proposed circuit.

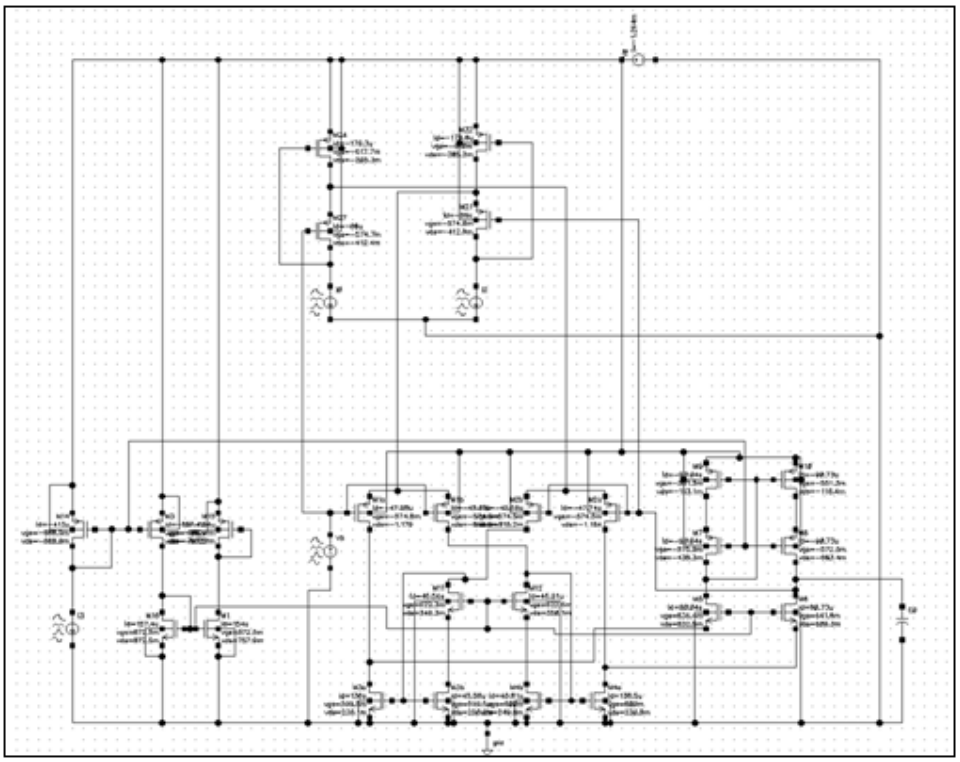

Figure 3. Snapshot from Virtuoso of Proposed Design Schematic

4. IMPLEMENTATION

To validate the theoretical results, we first implemented the recycling folded cascode topology as a benchmark for comparison with our proposed design. And then we simulated our own design and compared the results with our implementation of the RFC. Table 3 details the transistor sizes used in the implementation of the proposed structure as well as of our RFC implementation.

Table 3. Device sizes in implementation

Device	Proposed design	RFC
M_o[4]	-	60µm/500nm
M_{1a}, M_{1b}	100µm/500nm	-
M_{2a}, M_{2b}	128µm/360nm	-
M_1, M_2, M_3, M_4	64µm/360nm	64µm/360nm
M_{11}, M_{12}	64µm/360nm	70µm/500nm
M_{13}, M_{14}	64µm/360nm	84µm/500nm
M_5, M_6	8µm/180nm	8µm/180nm
M_{15}, M_{16}	10µm/180nm	10µm/180nm
M_7, M_{10}	24µm/500nm	24µm/500nm
M_8, M_9	8µm/500nm	8µm/500nm

5. SIMULATION RESULTS

All the simulations were done on cadence virtuoso with 0.18 µm technology using a VDD of 1.8V. The load capacitance was taken to be 5.6pF for all the simulations.

Here is the procedure for all the simulations. First of all DC analysis was done to ensure saturation for all transistors. After that, the AC analysis with differential input signal as 1VPP was done to measure the gain, GBW, UGB and Phase margin. After the AC analysis, a transient analysis was done to measure the slew rate and settling time (1%). For the transient analysis, the input signal was given as a square pulse (as shown in figure 12) of amplitude 1V at 5MHz. The results of the simulations are tabulated in Table 4 and Table 5. Table 6 details the bias currents in all the transistors of the proposed structure implementation.

Table 4. Results comparison with RFC Implementation

Parameters	**Proposed structure (tt)**	**RFC simulation**
DC Gain(dB)	68.48	71
UGB(MHz)	247.1	153
GBW(MHz)	335.5	172.26
Slew rate(V/µs)	92.8	67.4
Settling time (1%)(ns)	12.39	21.93
Phase Margin	26.3^o	58.1^o
Power Dissipation(mW)	2.493	2.18
I(total) (mA)	1.385	1.215
Capacitive load	5.6 pF	5.6 pF
Technology	0.18µm	0.18µm

Table 5. Result of proposed design at extreme corners

Parameters	tt	ff	ss
DC Gain(dB)	68.48	63.83	66.3
UGB(MHz)	247.1	267.6	203.9
GBW(MHz)	335.5	352	280.27
Slew rate(V/µs)	92.8	134.4	71.4
Settling time (1%)(ns)	12.39	8.9	17.25
Phase Margin	26.3^o	34.9^o	25.2^o
Power Dissipation(mW)	2.493	3.334	2.049
I(total) (mA)	1.385	1.684	1.265
Capacitive load	5.6 pF	5.6 pF	5.6pF
Technology	0.18µm	0.18µm	0.18µm

Table 6. Bias Current in Proposed Structure

Device	I_{bias}(µA) (tt)
M_{1a}, M_{2a}	181.1
M_{1b}, M_{2b}	86
M_1, M_4	48.79
M_2, M_3	46.29
M_{11}, $M_{12,}$ M_{13}, $M_{14,}$ M_{15}, M_{16}	90.63
M_5, M_6	46.29
M_7, M_{10}	139.4
M_8, M_9	46.29

The UGB of the proposed design is 247.1MHz while for RFC it is 153MHz showing a significant increase in bandwidth as expected. The GBW has also increased from 172.26 MHz for RFC to 335.5 MHz for the proposed design. As proved theoretically, the slew rate has improved from 67.4V/µs to 92.8V/µs. Also, correspondingly, the settling time (1%) has decreased from 21.93 ns to 12.39 ns showing an increase in the speed of the circuit significantly. Although the phase margin has reduced but it can be dealt with by using a compensation capacitance when a second stage is added to this design. Compensation capacitor will introduce a RHP zero in two stage op Amp, which will cause serious issue. Hence RC compensation is a better choice, as it will allow moving the zero away or forcing it in LHP. The most impressive aspect of this design is the fact the increased speed and bandwidth is achieved with nearly the same power dissipation as the RFC. The circuit has been implemented on all corners with all transistors in the saturation state. Table III demonstrates the simulation results of the circuit in all corners i.e. tt, ss and ff.

Figure 4 shows the linear settling time response plotted during the transient analysis which was used for the slew rate and settling time calculations. The open loop AC response of the amplifier

in tt, ff and ss corners is shown in figures 5, 6 and 7 respectively. Simulation graphs of settling time calculation are shown in figure 8, 9 and 10.

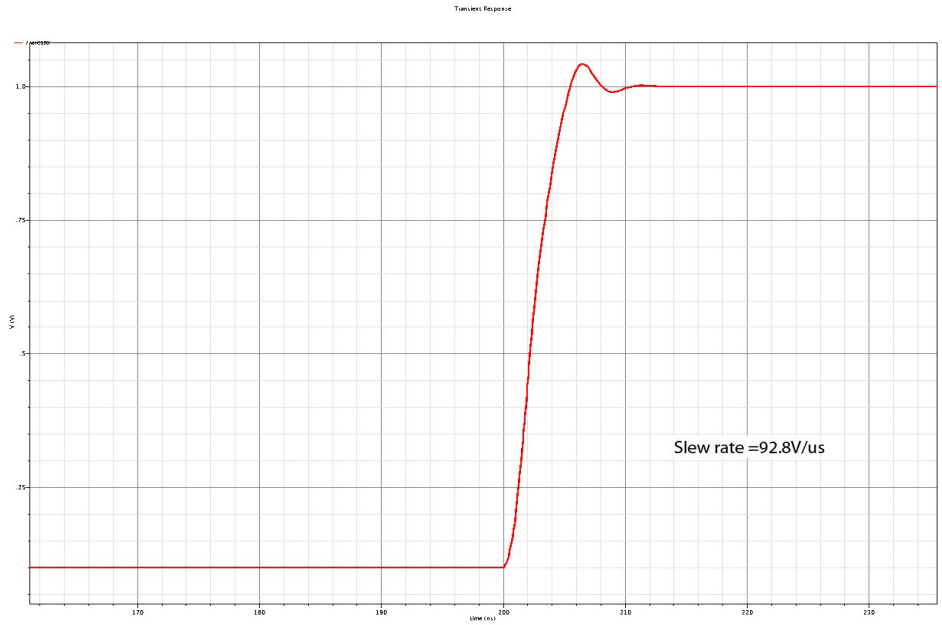

Figure 4. Graph for calculating rate slew

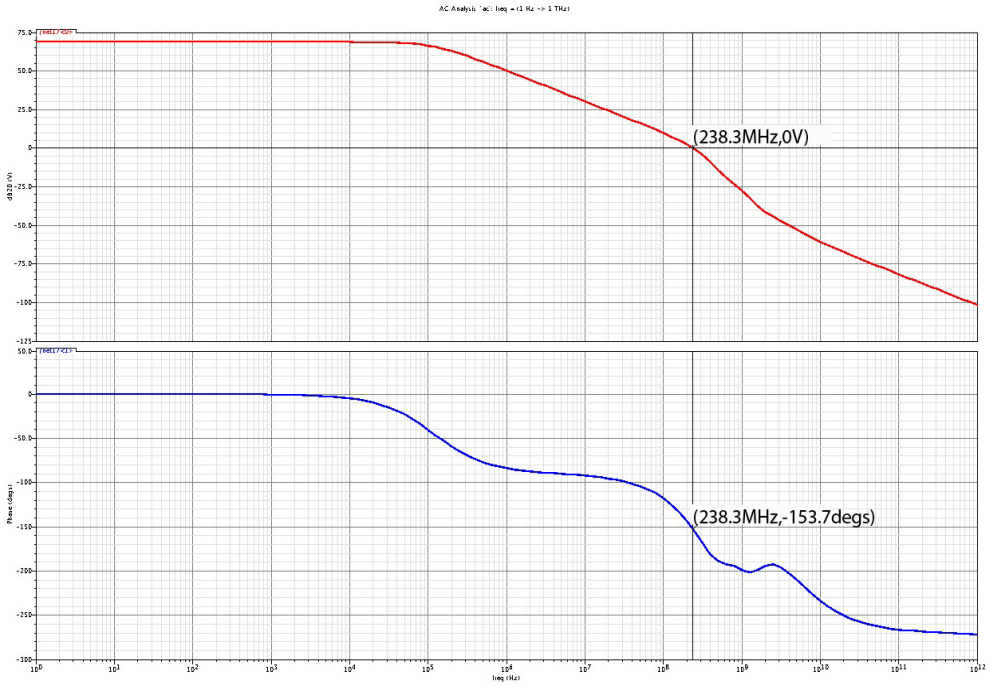

Figure 5. Gain & Phase plot for tt case

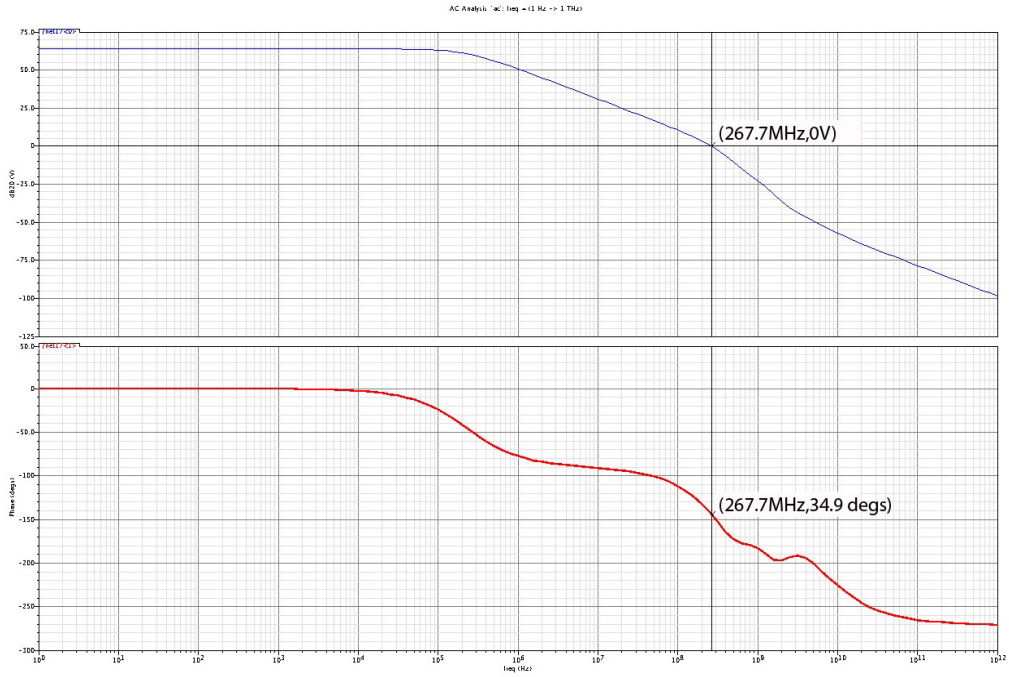

Figure 6. Gain & Phase plot for ff corner

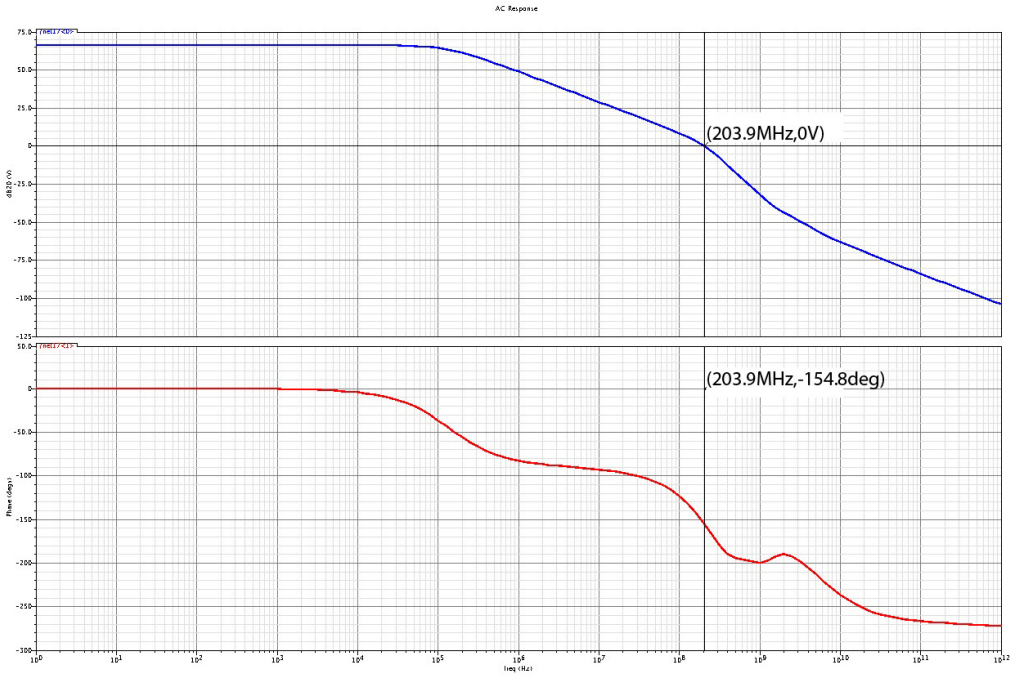

Figure 7. Gain & Phase plot for ss corner

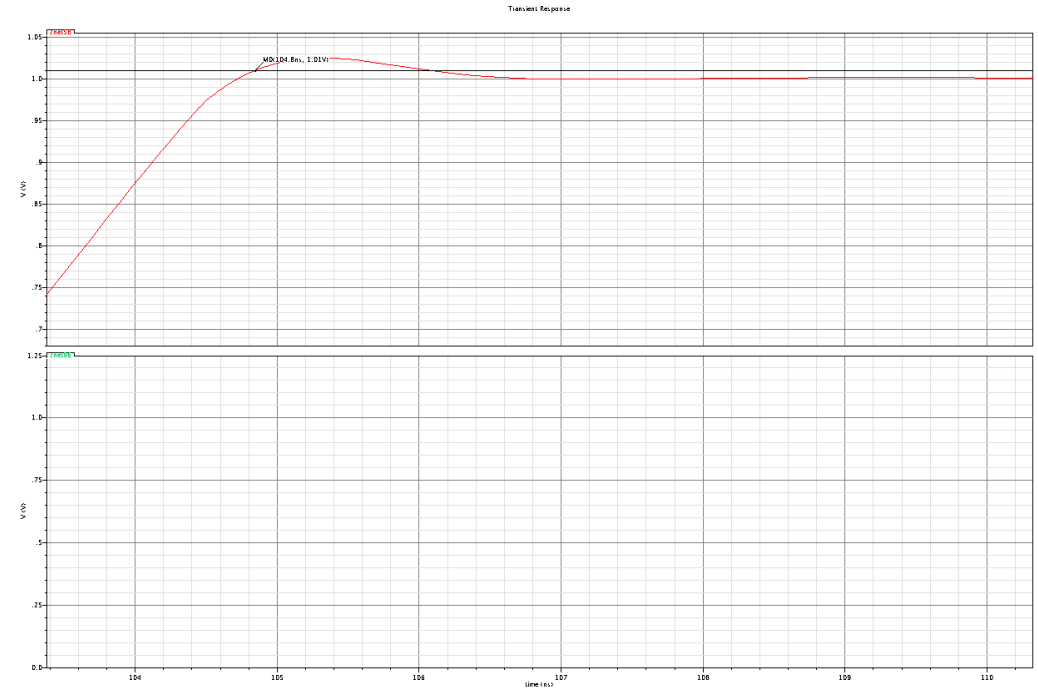

Figure 8. Settling time calculation at ff corner

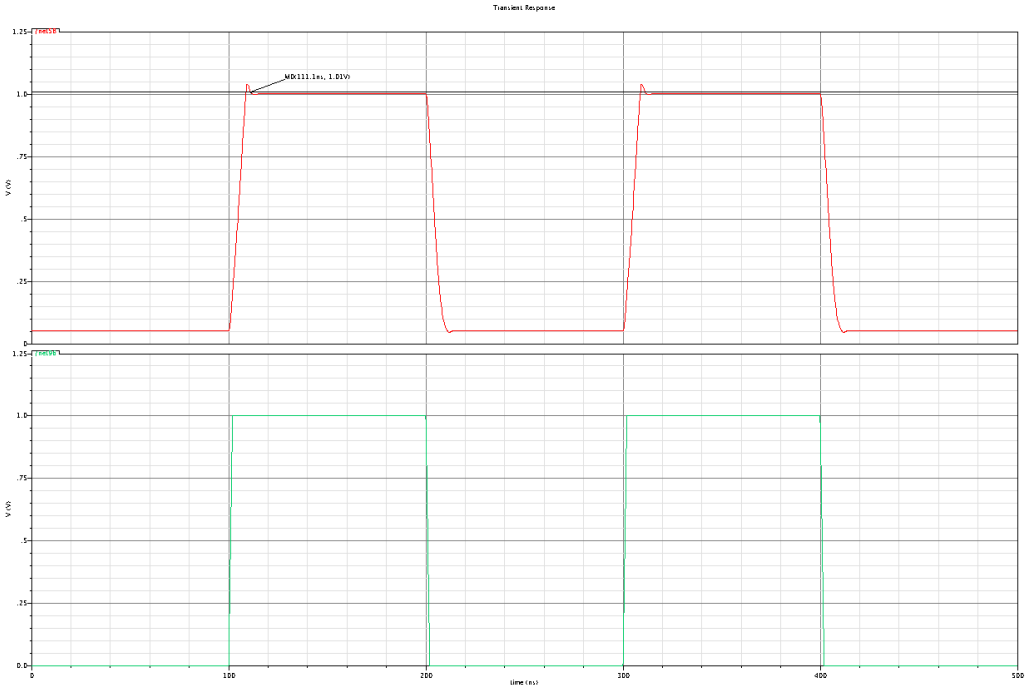

Figure 9. Settling time calculation at tt

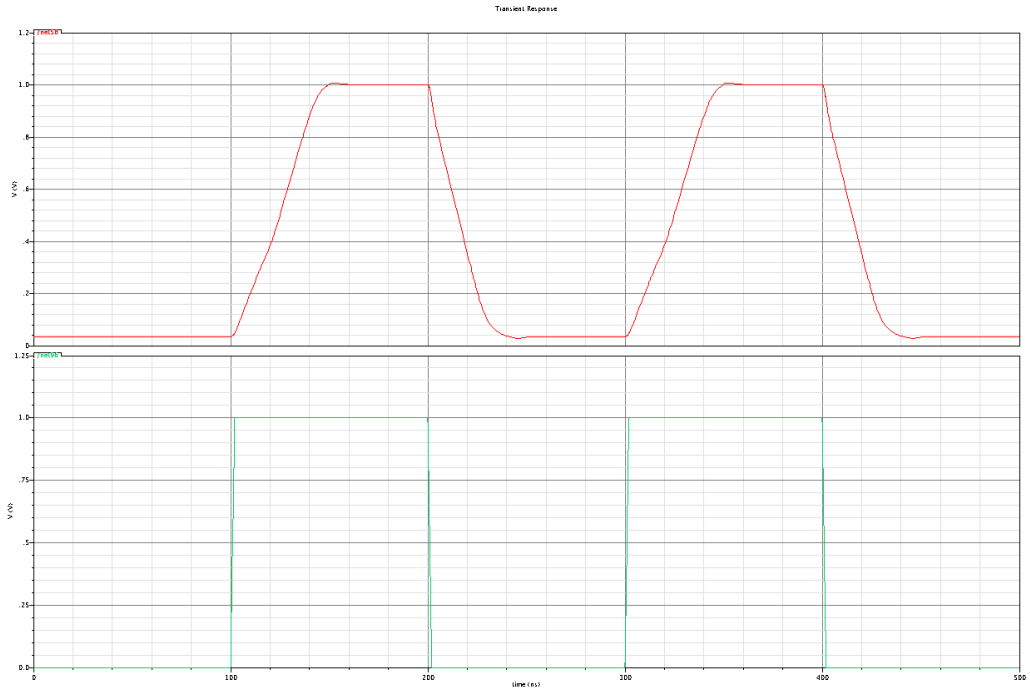

Figure 10. Settling time calculation at ss corner

5.1 Operational Amplifier as a Voltage Follower

The proposed design was implemented with a negative feedback in a voltage follower configuration (shown in figure 11) to test the stability of the design. An input pulse of 1V was given at 5MHz to check its response and functioning. Figure 9 below shows the input and output pulses in a voltage follower configuration. It is evident from the output graph that the delay introduced by the voltage follower is very small. Also, a distortion less and non-sluggish output is achieved as a result of high slew rate and bandwidth provided by the ARFC.

Due to high slew rate and bandwidth characteristics, ARFC finds application in various other speed critical circuits such as switched capacitor circuits, comparators etc.

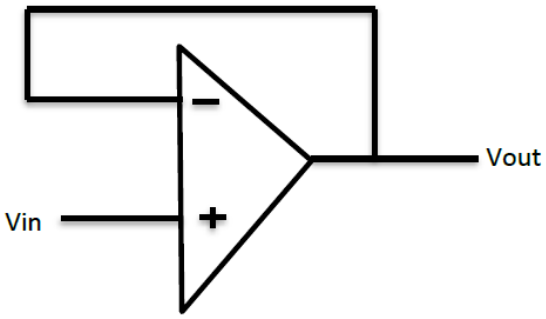

Figure 11. Voltage follower

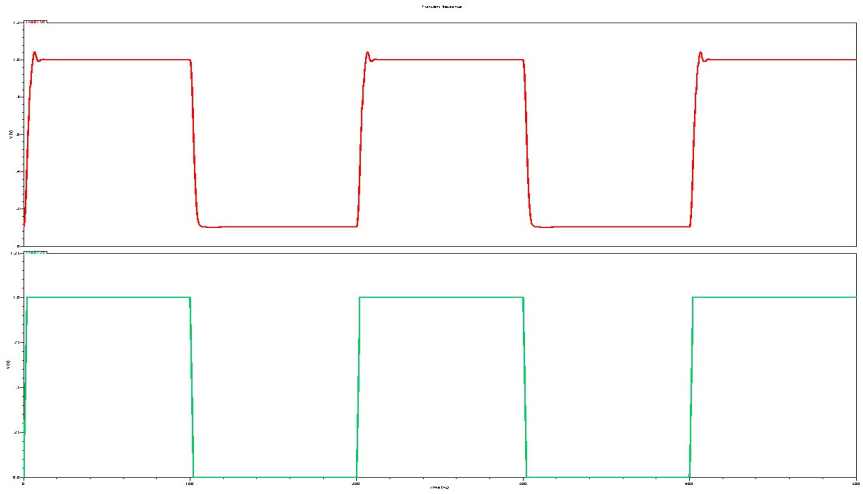

Figure 12. Transient Response in a voltage follower

7. FUTURE WORK

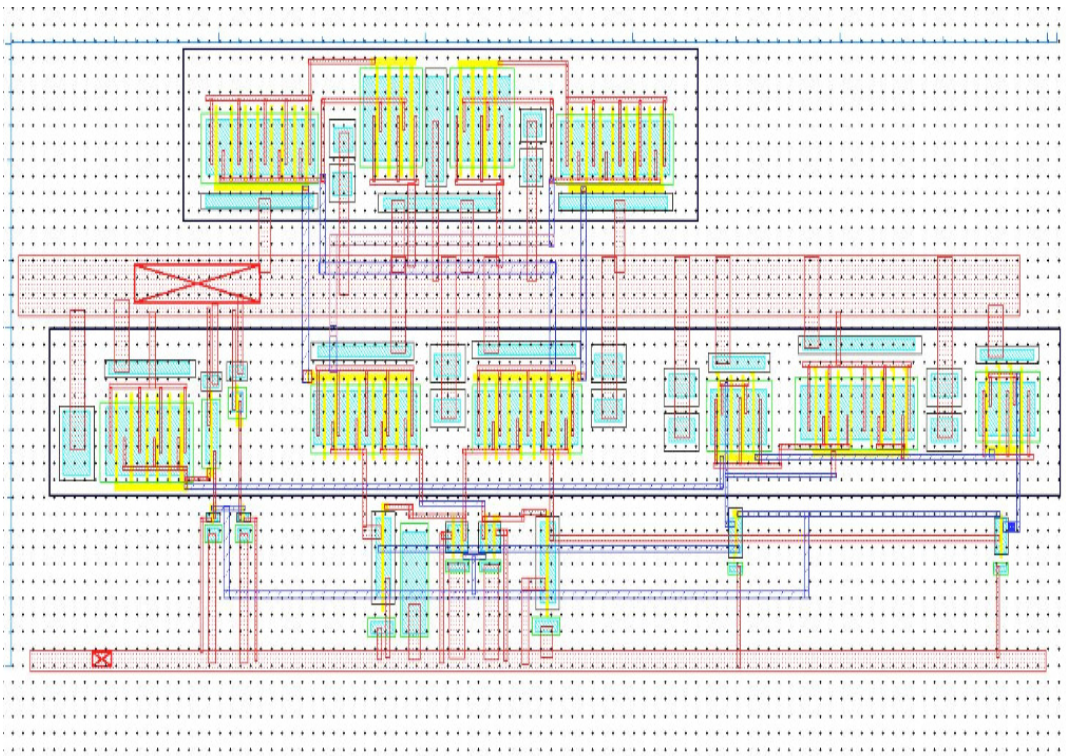

Figure 13. Preliminary layout of the proposed design

Figure 13 shows the preliminary layout that has been implemented for the proposed design. The future work for this research includes the optimization of the layout. Once an efficient layout is achieved with better routing and placement, the target will be to achieve a robust design. In the final stage, the design will be implemented on silicon.

From the design perspective, this design can be improved in terms of GBW by introducing a second stage. We can also implement compensation technique (in this case RC compensation) to improve the phase margin.

Other than focusing on solving the previous challenges, we aim to implement and test this topology for other technology such as 40nm etc. as this design is scaling independent (up to some extent).

8. CONCLUSION

It has been demonstrated that the proposed design shows a significant improvement over the conventional RFC in terms of UGB, GBW and slew rate with nearly the same power consumption. The additional adaptive biasing circuit added to the RFC, not only improves its speed and frequency response but also makes the circuit very adaptive to the changes in input voltage and noise fluctuations. With the RFC itself having an adaptive load, this addition of a self-adjusting current source makes it a very flexible, adaptive and self-biased circuit. This feature of the circuit also helps reducing the power consumption by changing currents corresponding to the changes in the input voltage. The theoretical results were confirmed with good agreement with the simulation data.

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