OPTIMIZATION OF CMOS 0.18 μM LOW NOISE AMPLIFIER USING NSGA-II FOR UWB APPLICATIONS

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ABSTRACT

A design and optimization of 3-5 GHz single ended Radio Frequency (RF) Low Noise Amplifier (LNA) for ultra-wide-band (UWB) applications using standard UMC 0.18 μm CMOS technology is reported. Designing of RF circuit components is a challenging job, since even after performing lengthy calculations and finding parameter values it is less guarantee that the design performs as expected. In view of this the optimization tool; Elitist Non-Dominated Sorting Genetic Algorithm (NSGA-II); has been employed to get the optimized starting values of components in the proposed LNA design. The obtained NSGA-II parameters were simulated using Cadence Spectre- RF simulator. The designed Low Noise Amplifier achieves a power gain of 22 dB and a minimum Noise Figure of 3 dB is achieved. It dissipates 12.5 mW of power out of 1.8 V supply.

KEYWORDS

LNA, NSGA-II Algorithm, Noise Figure, Power Gain, return losses

1. INTRODUCTION

Recent years have experienced explosive growth in the Radio Frequency /microwave semiconductor industry owing to the proliferation of a host of applications. Single-chip Bluetooth devices are already available and similar integration is likely to be achieved in cellular telephones and wireless networking in near future. Radio Frequency components are the basic building blocks of transceivers operating in GHz frequency range. Designing of RF circuit component needs lot of effort. After performing lengthy calculations and finding the parameter values it is not guaranteed that the circuit performs as expected. In Radio Frequency Integrated Circuits (RFIC), Low Noise Amplifiers are considered as black magic box because of their uncertain response with higher frequencies. Due to mismatch of input impedance and output impedance maximum power transformation is not possible. For Designing of the tank circuit, input and output impedance circuit, we need to design a passive filter with optimized component values. Optimization of the component value is a time consuming job. In view of this a CAD tool using Non-Dominated Sorting Genetic Algorithm (NSGA-II) has been employed. The design goal is formulated as an objective function. Some approximations and estimations on the design parameters are made in order to satisfy the requirement of the genetic algorithm. Many applications of genetic algorithm and optimization of LNA parameter by binary coded genetic algorithm is reported in [2, 3]. In this paper the design and optimization of single ended LNA using real coded genetic algorithm is presented. The rest of the paper is organized as: section-II gives brief introduction of Non-Dominated Sorting Genetic Algorithm. In section-III analysis and

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design problem of low noise amplifier is presented, in section-IV design objective and constrains optimization of LNA is mentioned. In section-V simulation result and discussion is presented. Scope and limitation of the NSGA-II has been discussed in section-VI and finally section-VII concludes the paper.

2. ELISTIST NON-DOMINATED SORTING GENETIC ALGORITHM (NSGA-II)

Genetic algorithms [3, 4] are search techniques used in computing to find true or approximate solutions to search or optimization problems. It is based on the concepts of natural selection, reproduction and mutation and has been used extensively in optimization problems. It can be classified in two sets depending on type of coding of the members; one is binary coded and the second is real coded [3]. In the past few years GA has undergone lots of developments developing its features, processing time, etc., some such developments are Multi Objective Genetic Algorithm (MOGA) [5,6], Elitist Non Dominated Sorting Genetic Algorithm [3].

3. ANALYSIS AND DESIGN OF LOW NOISE AMPLIFIER

The early part of this section is based on the literature survey and concludes with own design. As one of the essential components, Low Noise Amplifiers (LNAs) for wireless applications have attracted significant research interest and various approaches to the design of narrow band LNAs (operating below 3 GHz) and wideband LNAs (operating above 3 GHz) have been proposed previously [7-15] and as shown in Fig. 1(a-d). Distributed amplifiers [7] can provide very large bandwidth because of their unique gain-bandwidth tradeoff. However, large power consumption and chip area make them unsuitable for typical low –power, low cost wireless applications.

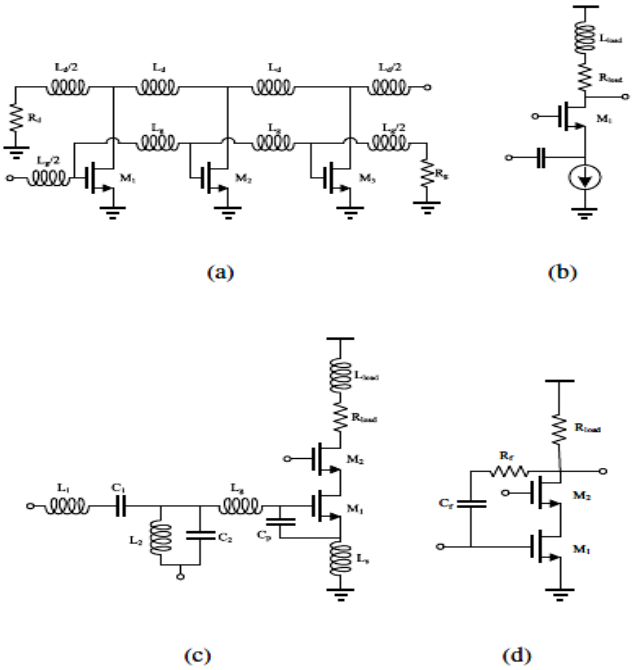


Figure 1. Various LNA Topologies (a) Distribute amplifier, (b) common gate, (c) inductive degeneration, (d) resistive feedback

Common-gate amplifiers [8, 9] exhibit excellent wide band input matching, but suffer from a relatively large noise figure (NF). Narrow-band LNAs like an inductively degenerated common-source amplifier can also be converted into a wideband one by adding a wideband input matching network [10]. However, the insertion loss of the passive input matching degrades the NF rapidly with frequency. Resistive-feedback amplifiers [11, 12-14] have very good wideband input matching characteristics. However, low NF and low power consumption can be hardly achieved simultaneously across a large frequency range. In [15], the noise cancellation technique is used to relax this trade-off in resistive feedback amplifiers.

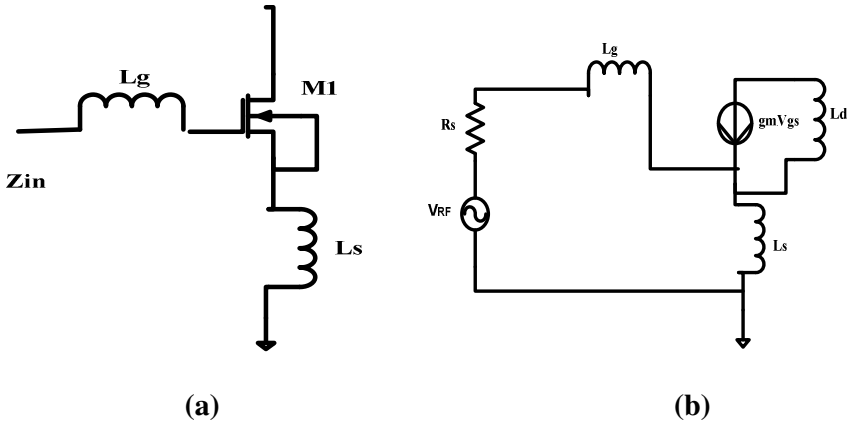


Figure 2. (a) Inductive source degeneration, (b) Small signal equivalent of 2(a)

A typical LNA must fulfill several challenging requirements. The LNA must provide a good input matching over a band more than 500 MHz. A high gain is also preferred to amplify the weak signals at the receiver and to overcome the noise effects from the subsequent stages. In addition, the noise figure of the LNA must be low (typically < 3 dB) since it plays a major role in defining the receiver's sensitivity. Moreover, the LNA also has to be power efficient and physically small to save power and reduce the cost, respectively. An inductively degenerated LNA configuration is proposed, as shown in Figure 2 (a). Inductive degeneration improves the linearity of the amplifier. The input impedance can be derived from the small signal analysis [16] of Figure 2 (b). By looking into the input side of Figure 2 (b), input impedance Z_{in} can be:

$$Z_{in} = s(L_s + L_g) + R_g + \frac{1}{sC_{gs}} + (\frac{g_m}{C_{gs}})L_s \tag{1}$$

Where L_s, L_g are the source and gate inductances, respectively; R_g is the transistor gate resistance, C_{gs} is the transistor gate-to-source capacitance; g_m is the transistor trans-conductance. The inductor parasitic resistance is ignored here. Input match requires that at the resonance frequency of the circuit, the impedance of the input stage is purely real and should be equal to 50 Ω. It follows that:

$$R_g + (\frac{g_m}{C_{gs}})L_s = 50 \tag{2}$$

Where ω_0 is the resonance frequency (rad/s), and

$$j\omega_0 (L_s + L_g) + \frac{1}{j\omega_0 C_{gs}} = 0 \tag{3}$$

The noise factor (F) is defined as [7, 8]:

$$F = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \frac{\gamma}{\alpha} g_m R_s (\frac{\omega_0}{\omega_T})^2 \tag{4}$$

$NF = 10 \cdot \log_{10}(F)$ Where unity frequency: $\omega_T = \frac{g_m}{C_{gs}}$, $\alpha \equiv \frac{g_m}{g_{d0}}$, R_s : source resistance, R_l : series resistance of inductors, R_g : gate resistance, γ: the thermal noise coefficient, ω_0 : the resonance frequency, g_m: transistor trans-conductance. For a source inductively degenerated LNA in Fig.2, we could put a lower bound on the trans-conductance of the input transistor to ensure that the final designed LNA can provide a reasonable gain [9]

$$A_V = G_m Z_{eq} = \left(\frac{1}{jw_0 L_s}\right)\left(\frac{jw_0 L_1}{1 - w_0^2 L_1 C_0}\right) \tag{5}$$

In order to formulate a geometric programming problem, we have to do some transformation and introduce a new variable to satisfy the requirement of geometric programming on the objective and constraints. Inequality constraints, and the objective function must be in the form of polynomial, equality constrains must be in the form of monomial. Here noise figure and gain are formulated for low noise amplifier. For low noise amplifiers, Objective function of Noise Figure can be formulated as:

$$F = F_{\min} + 50 \times R_n \times (0.02 - G_{opt})^2 \tag{6}$$

Where, $F_{\min} = \frac{1 + 2 \times W_0 \times \sqrt{\delta \times \gamma \times (1 - C^2)}}{Wt \times \sqrt{5}}$ $Rn = \frac{\gamma}{\alpha \times G_m}$

$Gopt = \alpha \times W_0 \times Cgs \sqrt{\frac{\delta \times (1 - C^2)}{5 \times \gamma}}$

The objective function of the Gain of LNA can be formulated as:

$$Gain = \frac{W_t \times R_{load}}{W_0 \times 2 \times R_{load}} \tag{7}$$

And the objective function of power consumption has been formulated as:

$$P_{DC} = I_D \times V_{DC} \tag{8}$$

Where, $I_D = \frac{\mu_n \times C_{ox} \times Width \times V_{od}^2}{2 \times ChannelLen gth}$

In above equation, second order effects on drain current have been neglected to reduce the complexity of the program. As the schematic diagram of the LNA is depicted in Figure 3, an

input impedance matching circuit is needed to match the source impedance to transistor input impedance. Objective function for Input impedance can be formulated from following equation.

$$Z_{in} = s(L_s + L_g) + R_g + \frac{1}{sC_{gs}} + (\frac{g_m}{C_{gs}})L_s \quad (9)$$

L_s and L_g is used to tune the input impedance (Z_{in}) to 50Ω at 3 GHz frequencies. C_{gs} *and* R_g Model the impedance looking into the gate of MOSFET. Here we can include pad capacitance and bond wire inductance also [10].

4. DESIGN OBJECTIVES AND CONSTRAINT OPTIMIZATION FOR NSGA-II

The simulations have been done for LNA with following constraints. Based on the technology parameters following have been defined as constant:

$$Cox\ (fF/\mu m2) = 8.632\ , Rs\ (\Omega) = 50\ , RL\ (\Omega) = 50\ ,$$
$$\beta\ (\Omega/nH\ ) = 1, \gamma = 2.5, L(\mu m) = 0.18\ , \lambda = 0.5,$$
$$Vth = 0.47V\ , Vdd = 1.8V$$

Design constraints for the component of circuit were taken as follows:

$$(1)\ 5 \le W1 \le 105\,\mu m\ \ (2)\ 0.1 \le Ls \le 50\,nH$$
$$(3)\ 0.1 \le Lg \le 50nH\ \ (4)\ 0.1 \le C \le 0.5\,pF$$

Simulations have been done with these parameters using NSGA-II. The NSGA parameters that were given are as follows: Mutation probability= 0.23671, Population size=100, Crossover Probability=0.99431, Number of generations=50.

5. SIMULATION RESULTS AND DISCUSSIONS

5.1. Simulation results using NSGA-II

The above mentioned optimization technique is implemented for Low Noise Amplifier design to optimize gain and noise figure. Direct equations have been used for gain and noise figure which were calculated for cascode LNA with inductive source degeneration. Program structure for LNA optimization using NSGA-II is shown in Figure 3 below. The "func-con. h" header file has been modified and the fitness functions and constraint functions have been replaced with the equations as discussed in section 3. Also, "LNA_equations.h" file has been added, which actually evaluates all these equations.

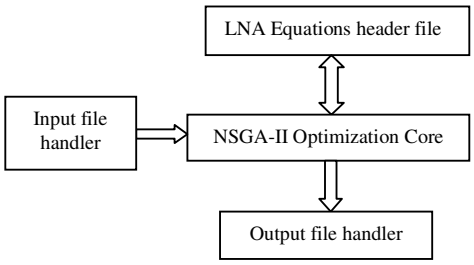
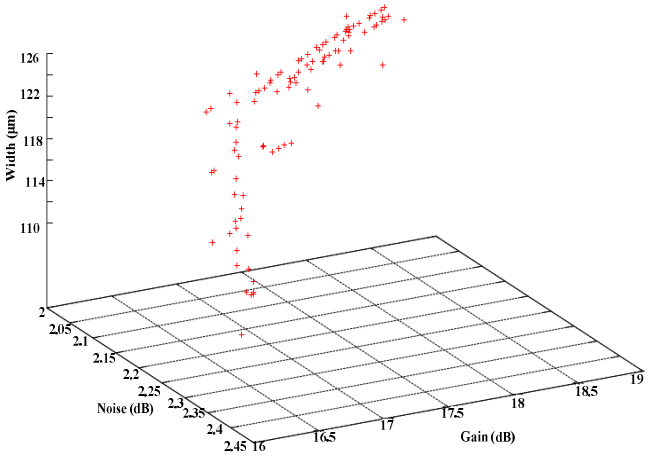


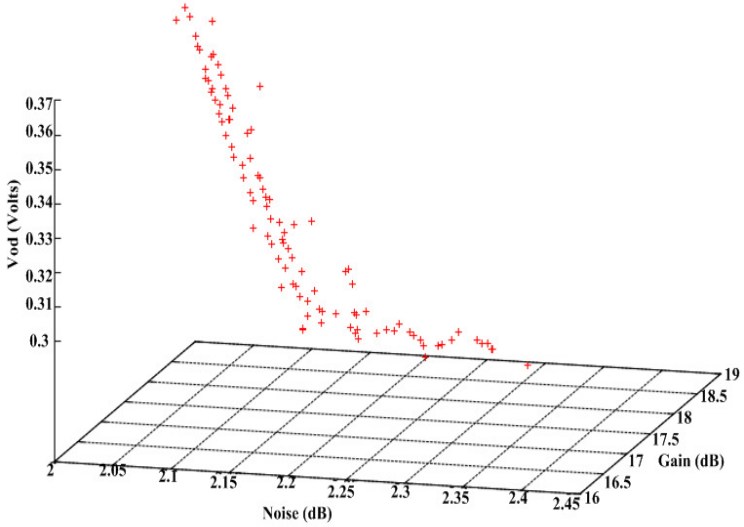
Figure 3. LNA Optimization Program Structure

After NSGA-II optimizer generates output files, another program convert those into design parameters and we can plot those values using GNUPLOT software as plotted in Figure 4(a-f). The trans-conductance, g_m, of the device is very much important to achieve good gain for LNA. However, this g_m depends on the transistor width. Also, g_m/I_D ratio needs to be maintained to achieve a required LNA gain. Thus, the width of the transistor needs to be chosen to give enough gain and minimum noise figure. From Figure 4 (a), thus, 'W' is chosen to be 105 µm. The overdrive voltage is one of the important parameters for transistor operating point analysis. The transistor should operate in the desired operating region for maximum gain. Thus, plots in Figure 4 (b) are plotted using NSGA-II to guess the initial overdrive voltage required for the transistor to be in the desired operating region.

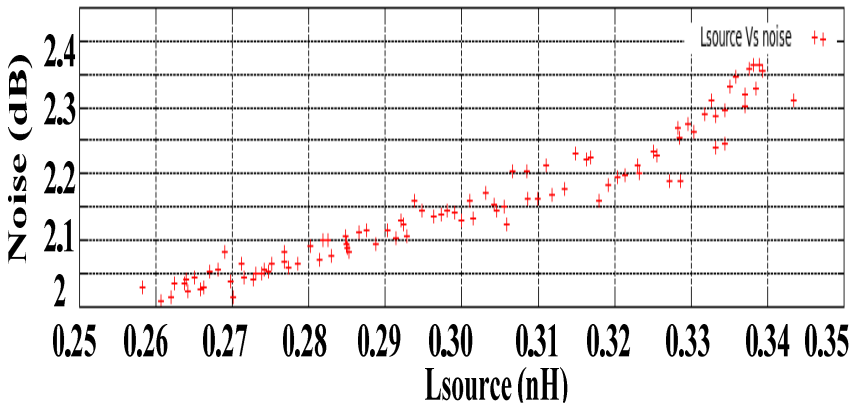
The optimized value of food is chosen to be 0.35 V from Figure 4 (b) since at this overdrive voltage maximum gain with low noise figure can be achieved simultaneously. The role of a source degenerated inductor (L_s) here is to match the input impedance to 50 Ω with low noise. From Figure 4 (c), it can be seen that the noise is increasing with L_{source} .Thus the optimum value of source at a minimum noise figure is chosen to be 0.27 NH.



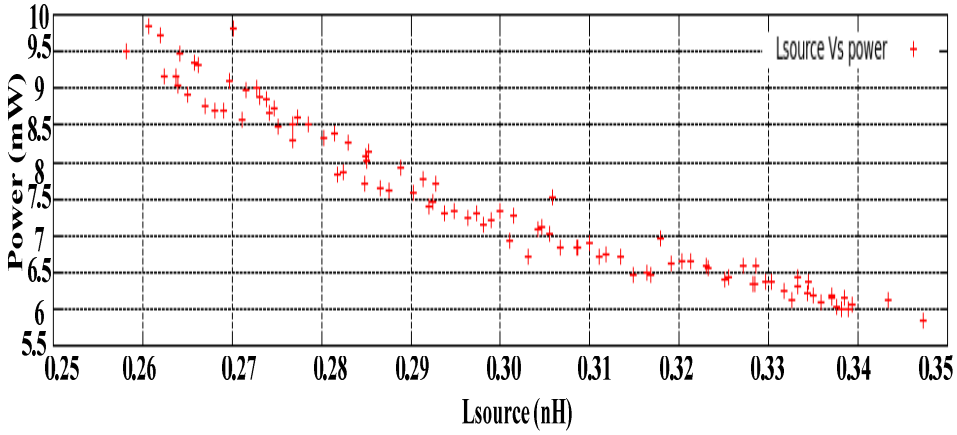
(a)



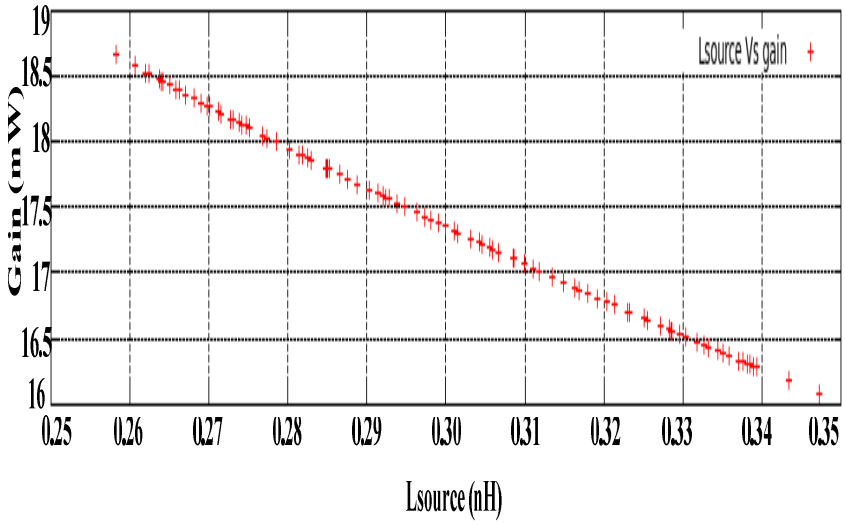
(b)


Lsource Vs noise
Noise (dB)
2.4
2.3
2.2
2.1
2
0.25 0.26 0.27 0.28 0.29 0.30 0.31 0.32 0.33 0.34 0.35
Lsource (nH)

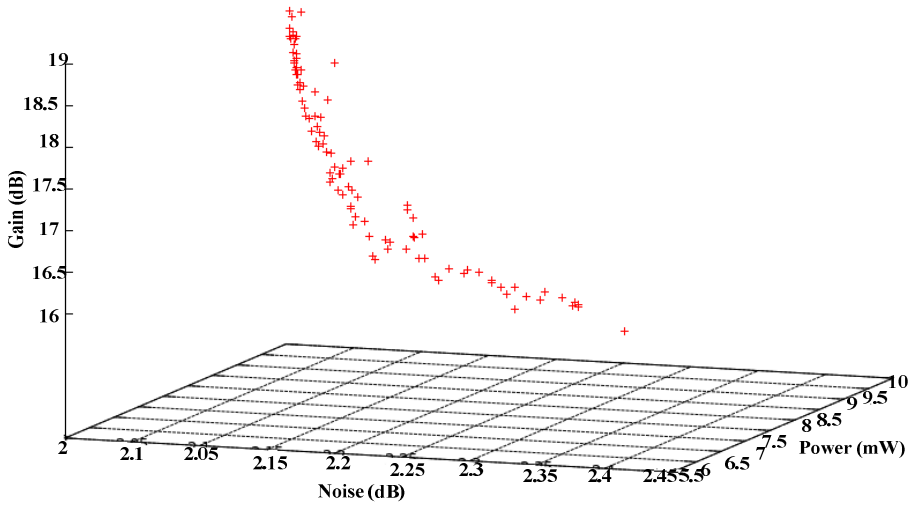
(c)


Lsource Vs power
Power (mW)
10
9.5
9
8.5
8
7.5
7
6.5
6
5.5
0.25 0.26 0.27 0.28 0.29 0.30 0.31 0.32 0.33 0.34 0.35
Lsource (nH)

(d)


Lsource Vs gain
Gain (mW)
19
18.5
18
17.5
17
16.5
16
0.25 0.26 0.27 0.28 0.29 0.30 0.31 0.32 0.33 0.34 0.35
Lsource (nH)

(e)



(f)

Figure 4. Simulation results using NSGA-II (a) Noise vs. Gain vs. Width of the transistor, (b) Noise vs. Gain vs. Overdrive voltage, (c) Noise vs. L_{source} (d) Power dissipation vs. L_{source} , (e) Gain vs. L_{source} & (f) Power vs. Noise vs. Gain

The effect of variation of a source inductor in power consumption can be seen from Figure 4 (d), where it can be seen that with the increase in value of source degeneration inductor; power dissipation reduces. But, for RF design the inductor should not be bulky. There always exists a trade-off among power dissipation, gain and noise figure for a Low Noise Amplifier design. The same can be seen in Figure 4 (e). While, from Figure 4 (f), it can be seen that the gain reduces with the increase in value of the source degenerated inductance. Thus, L_{source} = 0.2 nH has been chosen as further optimized value which gives the best compromise between gain and noise figure trade-off.

5.2. Simulation of LNA using Specter RF

The initial start up values given after running NSGA-II algorithm has been used for the designing of CMOS Low Noise Amplifier for 0.18 µm technology. The design is finally simulated using the Cadence Specter design tool. Figure 5 shows the proposed current reused LNA design. The S-parameter analysis is performed to obtain the gain and noise figure parameters. Also parallel LC tank circuit at the output tunes to the resonating frequency of 4 GHz. Capacitors at the input and output are dc blocking capacitor. The source terminal inductor (L_s) needs to be properly design to have a 50 Ω input matching. The dc blocking capacitors has been chosen to be of 103 fF each. While L_g is calculated from Eq. (13), once the optimum value of L_s is chosen to be 0.2 nH.

Usually the value of a lead is picked up from the available literature as references and accordingly the parallel tuning capacitor needs to be tuned to operate at 4 GHz frequency. The value of bias resistor, R_{bias}, is chosen to be large to minimize the noise entering into the design.

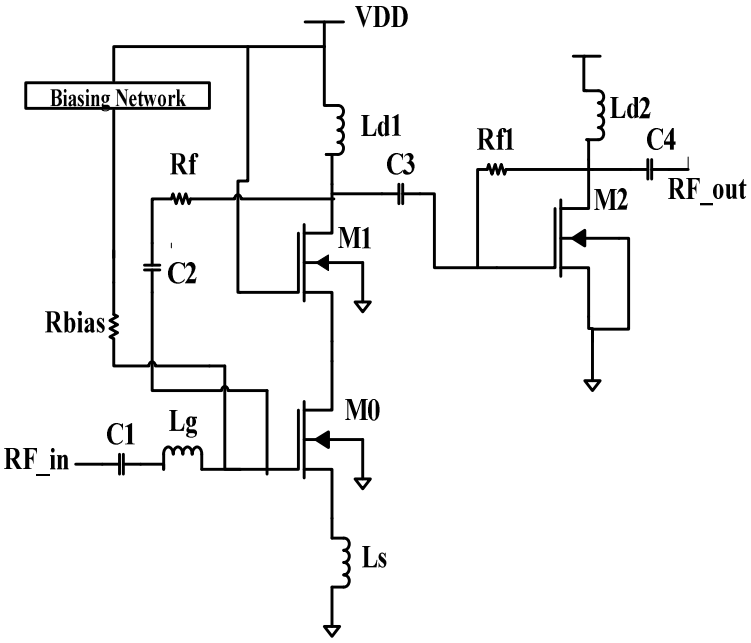


Figure 5. Proposed current reused two stage LNA

5.2.1. Parametric analysis

The parametric analysis is used for automating the generation of multiple simulations to test the effect of a source degeneration inductor (Ls) variation on the small signal gain (S_{21}). L_s is sweep from 50 pH to 200 pH as shown in Figure 6. It is observed that for 3-5 GHz band gain flatness is good for L_s as 200 pH, so, L_s is chosen to be 200 pH.

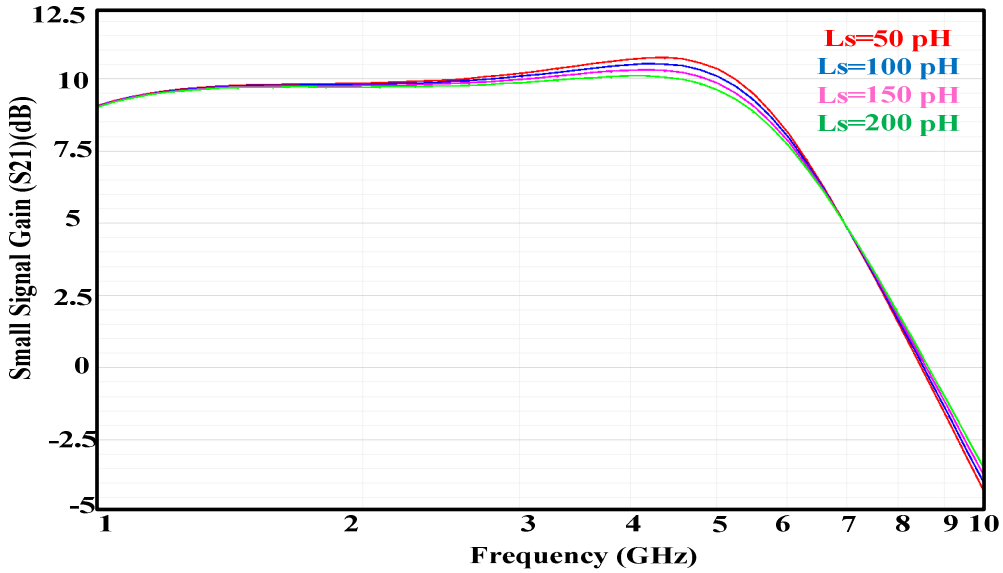


Figure 6. Parametric Analysis for Small Signal Gain

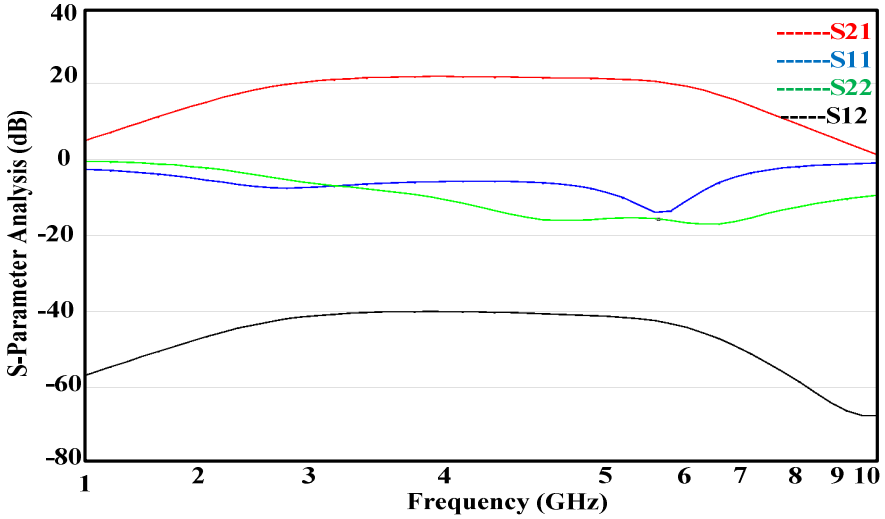


Figure 7. Overall S-parameter response of Single stage LNA

5.2.2. S-Parameter analysis

The simulated S-parameter results are as shown in Figure 7. The simulated results show that the LNA has a maximum flat gain of + 22 dB from 3 to 5 GHz band. Also, Figure 8 shows a smith chart analysis plots for input impedance matching. From smith chart it can be seen that the real part of the impedance is matched to 47 Ω. Thus minimum input and output return loss of < -10 dB each can be observed for 3 to 5 GHz. The input and output return losses have to be further improved by proper matching. The LNA also attends a high reverse isolation (S_{12}) of < - 40 dB for 3 to 5 GHz.

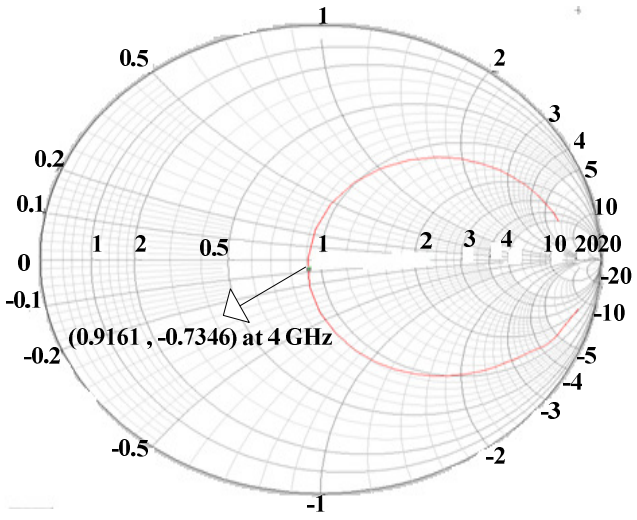


Figure 8. Input Impedance Matching using smith chart

5.2.3. Stability analysis

In the presence of feedback paths from the output to the input, the circuit might become unstable for certain combinations of source and load impedances. An LNA design that is normally stable might oscillate at the extremes of the manufacturing or voltage variations, and perhaps at unexpectedly high or low frequencies. The Stern stability factor characterizes circuit stability as in equation below:

$$K_f = 1+|\beta_f|^2 - |S_{11}|^2 - |S_{22}|^2 / 2|S_{21}||S_{12}| \quad (10)$$

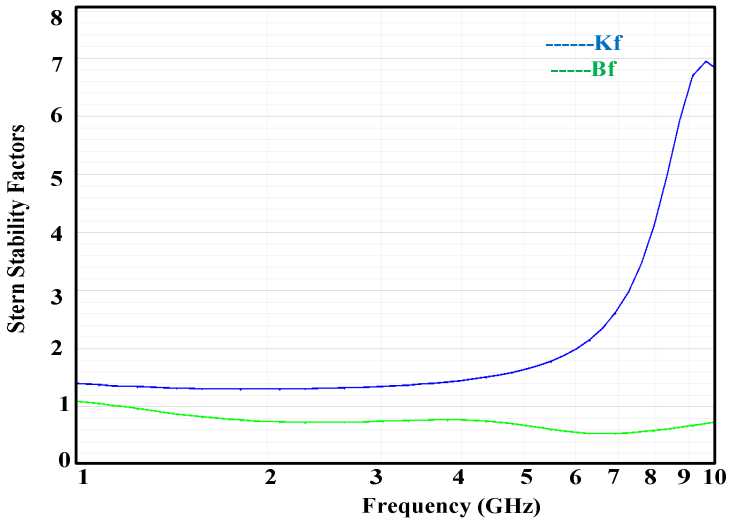


Figure 9. Stability Analysis

Where, $\beta_f = S_{11}S_{22}-S_{21}S_{12}$, If $K_f > 1$ and $\beta_f < 1$, then the circuit is unconditionally stable. The stability evaluation for the S parameters over a wide frequency range has been done to ensure that the K_f remains greater than one for all frequencies. As the coupling (S_{12}) decreases, that is as the reverse isolation increases, stability improves. One can use the techniques such as resistive loading and neutralization to improve stability for an LNA [11]. Stability analysis shows that $K_f > 1$ and $\beta_f < 1$ across the frequency band of interest, stating that designed LNA is un-conditionally stable as shown in Figure 9.

5.2.4 Linearity analysis

Linearity is also important parameter for LNA design along with gain. The linearity limits the actual power that can be drawn to the load by the LNA. The linearity is simulated using periodic steady-state (PSS) analysis. Figure 7 shows the linearity analysis with P_1dB compression point of -6.46719 dBm at 4 GHz.

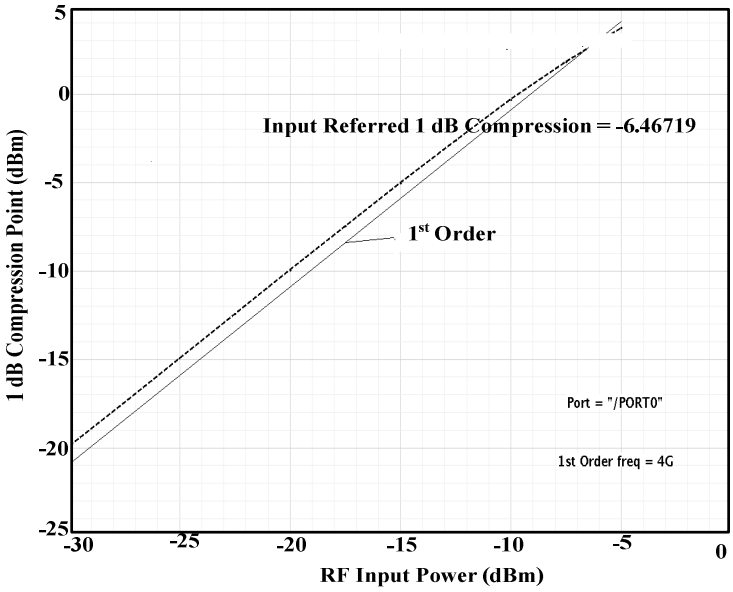


Figure 10. P_1dB compression point

5.2.5. Noise analysis

The overall noise figure (NF) and minimum noise figure (NF_{min}) of 2.31 dB and 2.1 dB respectively can be seen from Figure 11 for cascade common source with current re-use feedback.

Table-1 shows the performance summary of the proposed low noise amplifier and its comparison with the previously reported LNA designs. At the time of designing parasitic play important role in obtained results but here we are not considering them because our first motivation is to take initial guess of the values. The design parameters obtained from multi objective genetic algorithm is comparable with the result obtained in Cadence Spectre tool.

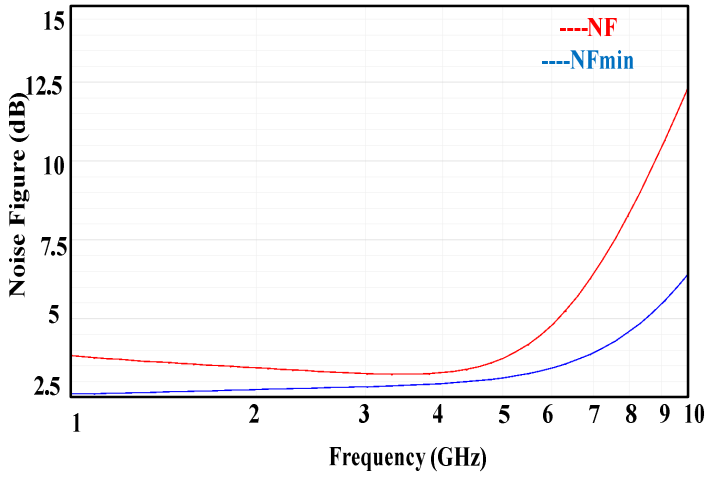


Figure 11. Noise Figure plots for two stage LNA

Table 1 Comparison of Wideband LNAs: Published and the optimized LNA design parameters

Proposed LNA designs			Previously Reported LNA Designs		
Targeted parameters		Optimized two stage LNA design with current re-used using NSGA-II	[15][16]	[17]	[18]
Technology	0.18µm CMOS	0.18µm CMOS	0.65 µm CMOS	0.18 µm CMOS	0.18 µm CMOS
Frequency of Operation	3-5 GHz	3-5 GHz	0.2-5.2 GHz	1-5 GHz	3-5 GHz
Supply Voltage	1.8 V	1.8 V	1.2 V	1.8 V	1.8 V
Gain	20 dB	22 dB	13-15.6 dB	11-13.7 dB	8.6-9.5 dB
S11	< -10 dB	< -10 dB	***	<-10 dB	<-10.3 dB
S22	< -10 dB	< -10 dB	***	***	-11.8 dB
S12	< -10 dB	-40 dB	***	***	***
NF	< 4 dB	3.5 dB	< 3.5	5-6.5 dB	2.7 dB
NF_{min}	< 3 dB	3 dB	***	***	***
P1dB	< -10 dBm	-6.46719	***	***	***
Power	< 15 mW	12.5 mW	***	9 mW	15 mW

Note: *** Not mentioned

6. SCOPE AND LIMITATION OF DESIGNED TOOL

Designed optimization tool gives only approximate values of the design parameters. This tool is designed only for final stages of RFIC design process. Parasitic effects associated with passive on-chip components like capacitors, inductors and resistors have not been taken into account for shorter simulation time of the circuit.

7. CONCLUSION

This paper shows that the optimization of RF Circuits is possible with real coded genetic algorithm. It is found that real coded Multi-Objective Genetic Algorithm has many advantages over binary coded genetic algorithm. Non-Dominated Sorting Genetic Algorithm is used for optimization tool, which is giving comparative results with design software simulation like Cadence Spectre tool. In this paper it is shown that the Low Noise Amplifier can be designed for the noise figure of 3.5 dB and power gain of 22 dB. The two stage LNA topology with current reused technique is designed and optimized for 3-5 GHz UWB applications. The simulated S_{11} and S_{22} parameters are well below – 10 dB is obtained with the simple matching network for the desired band of 3-5 GHz. The designed LNA dissipates 22 mW of power out of 1.8 V supply. Also the proposed LNA design is found to be unconditionally stable and operates linearly throughout the desired band. A comparison between the present results and the results of previously reported LNA shows that the reported LNA design reaches the state-of-the-art LNA designs for UWB application. In future; the NSGA-II optimization tool can be used to extend for 3.1-10.6 GHz LNA design for ultra-wide-band wireless RF system. Thus the design tool is useful in finding circuit element values quickly reducing the RF circuit designer time.

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