DESIGN AND IMPLEMENTATION OF 10 BIT, 2MS/s SPLIT SAR ADC USING 0.18um CMOS TECHNOLOGY

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ABSTRACT

This paper focuses on Design and Implementation of 10 Bit, 2MS/s successive approximation Register (SAR) Analog to digital converter (ADC) using Split DAC architecture. This SAR ADC architecture is designed and simulated using GPDK 0.18um CMOS technology. It consists of different blocks like sample and hold, comparator, Successive Approximation Register (SAR) and Split Digital to analog converter (DAC). For each block of SAR ADC power is calculated. DAC is an important component within the SAR ADC. The charge redistribution DAC in a Split capacitor configuration has a total capacitance which is 96.87% smaller compared to a conventional binary weighted design. Hence Split DAC gives an optimized architecture and it consumes less power. Optimized design of DAC architecture ensures the accuracy of the components, which improves the performance of SAR ADC. Comparator constructed from resistances, capacitance and dependent voltage sources instead of MOS transistors. Dynamic range for SAR ADC using split DAC is 60.19dB. The supply voltage is 1.2V. The total Power consumed by SAR ADC using Split array DAC is 95.65114uW and SAR ADC using binary weighted capacitor DAC is 211.19084uW.

KEYWORDS

Successive Approximation , Analog- to- Digital converter, Digital- to- Analog converter, Split array, Charge redistribution

1. INTRODUCTION

Successive approximation register (SAR) analog to digital converters (ADCs) have attracted more attention because of low power, excellent power efficiency, scalability and characteristics of digital nature. In the literature survey there are various kinds SAR topologies such as binary-weighted SAR, C-2C SAR, split SAR, etc. In general, their principle of working is based on the use of a binary search algorithm to estimate the digital equivalent of an input analog signal. SAR ADCs using binary weighted DAC present a good linearity performance but suffer from exponential reliance of the total capacitance on resolution which results in low sampling speed, and large area occupation. On the converse, much higher speed is provided by C-2C SAR ADCs

but introduce non-linearity issue because of the parasitic capacitances at the intermediate nodes which limit their resolution below 8 bits. The resolution drawback of C-2C SAR ADCs is eliminated by split SAR ADCs while maintaining their speed advantage by reducing the number of intermediate nodes. Fundamentally, the split SAR ADC consists of two capacitor arrays most significant bit (MSB) array and least significant bit (LSB) array connected by a bridge capacitor. The total weight of the LSB array must be equal to the weight of the lowest-bit capacitor of the MSB array in order for the two capacitor arrays have the same scaling. This requires the attenuation capacitor to have a fractional value, which can be difficult to match when the design is implemented. Therefore, the linearity of the ADC is considerable reduced. In [1], to increase the linearity, an attenuation capacitor with integer capacitance value is used. An attenuation capacitor is added to the LSB array to keep the correct scaling. In addition, in order to reduce the input loading capacitance, one unit capacitor is added to the MSB array and the input is only sampled onto the bottom plates of the MSB array. To calibrate the weight mismatch between the lowest-bit capacitor of the MSB array and the capacitors of the LSB array a Capacitor DAC mismatch calibrator is designed [1] [6].

One serious issue for SAR ADCs is the capacitor mismatches that result from process variations and device parasitic. It normally limits the ADC linearity to less than 10-bit. The capacitor mismatch is minimized by increasing the size of the capacitor; however, this slows down the conversion speed and unfortunately increases the chip area and power. A much better way to alleviate the capacitor mismatch issue is to perform capacitor mismatch calibration [2] [3]. On one hand, in very high sampling rate (200–500 MS/s) applications, medium-resolution SAR ADCs are increasingly used. On the other hand, in low energy radios and biomedical applications, ultra low power and low-frequency SAR ADCs are being used. In several cases, a significant part toward the total power consumption of the SAR ADC is due to the capacitive digital-to-analog converter. This has brought to force the challenge of further reducing the power consumption of the DAC. Many studies have been performed on reducing the switching power of the DAC [4]. In SAR ADCs the binary-weighted capacitive DAC is more widely used. But, the exponential increase in the capacitance of the DAC array with the resolution, which imposes larger consumption of switching energy, area and settling time. The split capacitive DAC is a valuable alternatives, which has been recently reconsidered for medium resolution. Its key drawback lies in the parasitic capacitors that destroy the desired binary ratio of the capacitive DAC array, thus degrading the conversion linearity. However, the split structure can become suitable for a medium-resolution applications by using the metal-insulator-metal capacitor or/and DAC mismatch calibrations. On the other hand, the switching sequences of the DAC array are directly correlated with the conversion linearity, where the conventional charge-redistribution switching results in worse conversion linearity and extra energy losses [5].

In a SAR ADC, the capacitive DAC, comparator and SAR logic are the main sources of energy consumption. The digital energy consumption reduced by the technology innovation while the power consumption of comparator and capacitive DAC is restricted by the noise and matching requirements. The switching energy is significantly determined by the capacitor switching scheme mainly in the capacitive DAC [7]. The split SAR ADC offers the excellent trade-off in terms of area, speed, and power consumption [8]. The capacitive digital-to-analog converter dominates the overall power consumption compared with a digital control circuit and comparator in SAR analog-to-digital converter [9].

This paper describes design and implementation of 10-bit, 2MS/s split SAR ADC using 0.18um CMOS technology. Section 2 discusses the SAR ADC review. Section 3 discusses the basics of SAR ADCs and Modifications. Section 4 explains the implementation of split DAC and split SAR ADC using Cadence. Section 5 contains experimental results and Section 6 contains conclusions.

2. SAR ADC REVIEW

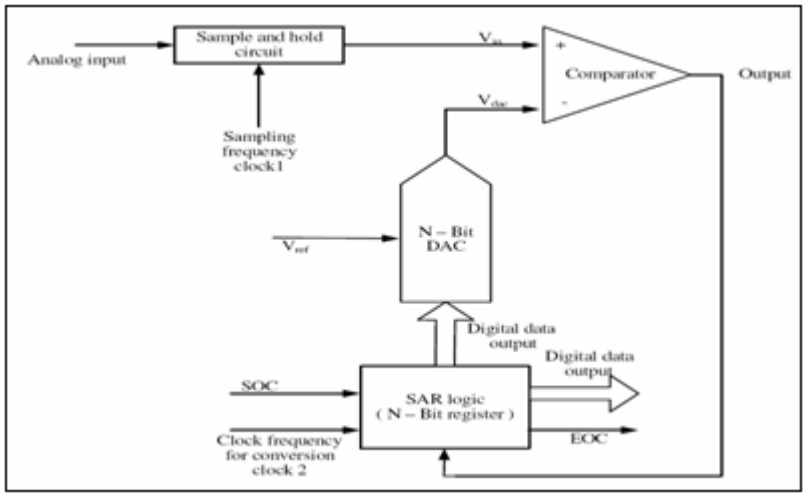


Figure 1. N-Bits SAR ADC Architecture

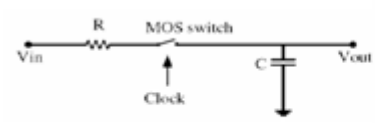
The block diagram of SAR-ADC is as shown in Fig. 1. It consists of sample and hold circuit, successive approximation register, N-bit capacitive DAC and high speed comparator. The fundamental principle of data conversion is based on successive approximation algorithm and is as given in (1) [10], the MSB bit sets V_{ref} to 0.5. The next bit attenuates V_{ref} to 0.25 and so on, finally giving zero, once the analog signal value becomes equal to the sum of the attenuated V_{ref} values. This approximation is the heart of any given SAR converter.

$$V_{analog} - \{V_{ref}[b_0\, 2^{-1} + b_1\, 2^{-2} + \text{---} b_{N-1}\, 2^{-N}]\} = 0. \quad (1)$$

3. BASICS OF SAR ADC AND MODIFICATIONS

3.1. Sample and Hold circuit

The sample and hold circuit design is a key aspect in any high resolution, high speed ADC process, as the conversion process depends only on the instantaneous voltage developed across the hold capacitor. The simplest form of a sample and hold circuit design for a sinusoidal input, and the circuit behaviour can be graphically shown in Fig. 2 and Fig. 3 respectively. It consists of a MOSFET switch with a finite ON resistance R, a hold capacitor of value C and a clock signal controlling the ON/OFF time of MOS switch.



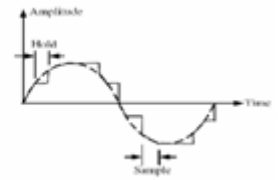


Figure 2. Sample and Hold Circuit Figure 3. Response to sinusoidal I/P

3.2. Charge Redistribution DAC

Fig. 4 shows a charge redistribution DAC is a parallel array of binary-weighted capacitors, and $2^N C$ is the total capacitance. All capacitors are discharged firstly. The digital signal switches each capacitor to either ground or V_{ref}, causing the output voltage, V_{out}, to be a function of the voltage division between the capacitors [11].

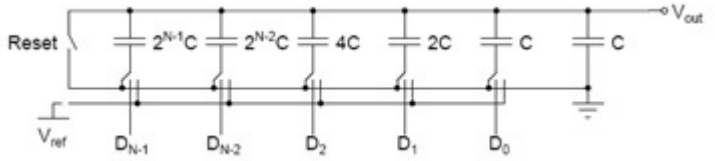


Figure 4. A Charge-redistribution DAC

The capacitor array totals $2^N C$. Thus, if the MSB is high and the remaining bits are low, then a voltage divider occurs between the MSB capacitor and the rest of the array. The analog output voltage, V_{out}, becomes:

$$V_{out} = V_{ref} \cdot \frac{2^{N-1} C}{\left(2^{N-1} + 2^{N-2} + 2^{N-3} + \ldots + 4 + 2 + 1 + 1\right) C}$$

$$= V_{ref} \cdot \frac{2^{N-1} C}{2^N C} = \frac{V_{ref}}{2} \qquad (2)$$

Which confirms the fact that the MSB changes the output of a DAC by ½ V_{ref}. Fig. 5 shows the equivalent circuit under this condition.

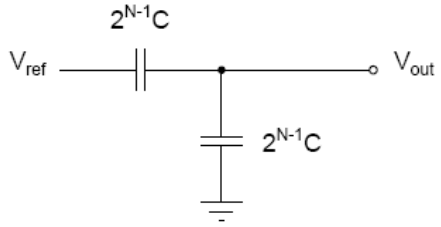


Figure 5. Equivalent circuit with the MSB = 1, and all other bits set to zero

The ratio between V_{out} and V_{ref} *due* to each capacitor can be generalized to:

$$V_{out} = \frac{2^k C}{2^N C} . V_{ref} = 2^{k-N} . V_{ref} \qquad (3)$$

Where it is assumed that the *k*-th bit, D_k, is one and all other bits are zero. Superposition can then be used to find the value of V_{out} for any input word by:

$$V_{out} = \sum_{k=0}^{N-1} D^k \, 2^{k-N} . V_{ref} \tag{4}$$

3.3. Split array DAC

The charge-redistribution architecture is very much accepted because of its simplicity and relative good accuracy. While a linear capacitor is required, high resolution in the 10- to 12-bit range can be achieved. However, as the resolution increases, the size of the MSB capacitor becomes a main concern. For example if the unit capacitor, *C*, were 0.5pF, and a 12-bit DAC were to be designed, the MSB capacitor would need to be:

$$C_{MSB} = 2^{N-1}.0.5pF = 1024 \text{ pF} \tag{5}$$

A split array technique used to reduce the size of capacitors. A 6-bit example of the array is shown in Fig. 6. This architecture is slightly different from the charge-redistribution DAC shown in Fig. 4 in that the output is taken off a different node and an additional attenuation capacitor is used to separate the array into a LSB array and a MSB array. Note that the MSB (D_5) corresponds to the rightmost switch and the LSB (D_0) now corresponds to the leftmost switch [11].

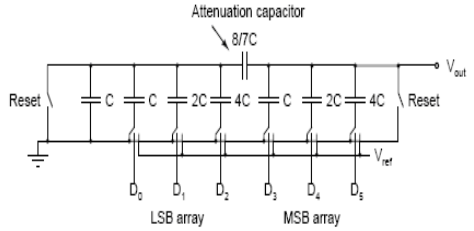


Figure 6. A Charge-redistribution DAC using a split array

The value of the attenuation capacitor can be found by:

$$C_{att} = (\text{Sum of the LSB array capacitors / sum of the MSB array capacitors}) * C \tag{6}$$

Where the sum of the MSB array equals the sum of LSB capacitor array minus *C*. The value of the attenuation capacitor should be such that the series combination of the attenuation capacitor and the LSB array, assuming all bits are zero, equals *C*. To prove this a derivation is made; refer to formula (7) [12]. The output voltage is defined as the attenuation factor times the LSB bits plus the MSB bits times the reference voltage. The attenuation factor is a capacitive divider between the attenuation capacitor and the sum of the LSB capacitors. One can see that with some manipulation this is equal to formula (4).

$$V_{out} = \left(\frac{\frac{2^{N/2}}{2^{N/2}-1}}{\frac{2^{N/2}}{2^{N/2}-1} + 2^{N/2}} \sum_{k=0}^{N/2-1} D_k \, 2^{k-N/2} + \sum_{k=N/2}^{N-1} D_k \, 2^{k-N} \right) . V_{ref}$$

$$= \left(\frac{1}{2^{N/2}} \sum_{k=0}^{N/2-1} D_k \, 2^{k-N/2} + \sum_{k=N/2}^{N-1} D_k \, 2^{k-1} \right) . V_{ref} \tag{7}$$

$$= \left(\frac{2^{N/2}}{2^{N/2}} \cdot \sum_{k=0}^{N/2-1} D_k 2^{k-N} + \sum_{k=N/2}^{N-1} D_k 2^{k-N} \right) . V_{ref}$$

$$= \left(\sum_{k=0}^{N/2-1} D_k 2^{k-N} + \sum_{k=N/2}^{N-1} D_k 2^{k-N} \right) . V_{ref}$$

$$= \sum_{k=0}^{N-1} D_k 2^{k-N} . V_{ref}$$

3.4. Comparator

The introduction of the Application Specific Integrated Circuits has created the need to simulate complex circuits which include both analog and digital functions on the same chip. The circuit simulation becomes quite difficult because of couple of problems. Firstly, mixed mode simulators are required for the combined analog and digital functions on the same chip. Secondly, the large number of active devices per chip, significantly increases the required simulation time and increases the problem of convergence. Hence, macro-modeling addresses the second concern by reducing the complexity of the circuit. Macro-models use simplified simulation elements mathematical functions to define the behavior of a simulation model. Macro-modeling techniques are the only practical method of modeling some complex circuitry. Macro-functions are used in practice to reduce modeling-time and make simulations run faster and converge better [13]. The macro model of comparator constructed from resistances, capacitance and dependent voltage source is shown in Fig. 7 instead of transistors. It reduces the simulation time and power consumption.

Figure 7. Comparator.

3.5 SAR LOGIC DESIGN

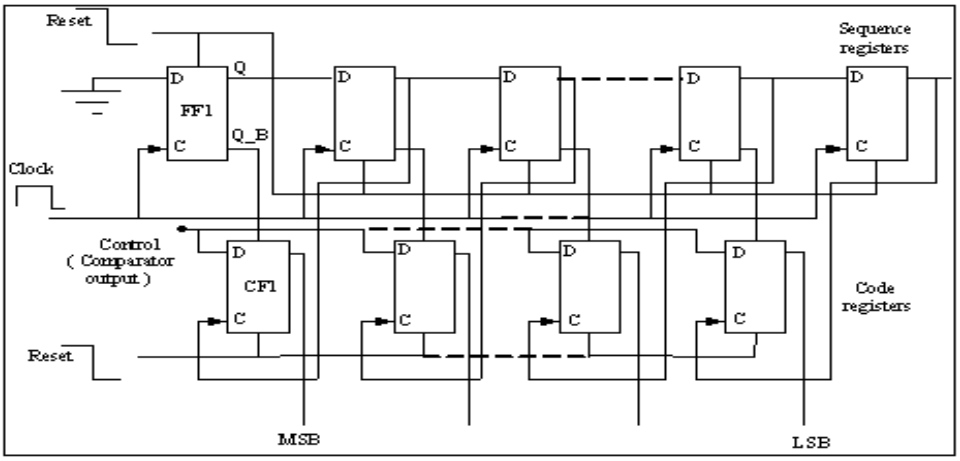


Figure 8. SAR Logic [14]

The schematic of the SAR logic is as shown in Fig. 8. Firstly the reset line goes low, and controls set line of flip-flop1 [FF1] and reset lines of all other sequencer flip-flops. The same reset signal also controls the reset line of code register flip-flops. Output Q and output Q_B of FF1 are set to 1 and 0 respectively. Q_B also controls set line of code register flip-flop1 [CF1]. Hence the CF1 output is forced to 1. This is the MSB bit and the weight for voltage full scale range VFSR/2. It should be noted that, since sequence register is reset initially, the set input of all the code registers flip- flops except CF1 is at logic 1. Hence all the other code register output states are logic 0. We get a sequence MSB=1 and all others set to 0. The analog equivalent of this weight will be generated by the DAC. When reset goes high and clock is triggered, (notice that D input of FF1 sequencer array is grounded-logic 0) Q becomes 0 and FF2 outs logic High. This low to high transition of FF2 triggers or clocks the code register flip- flop CF1 to store control bus value (comparator output) to its output. When clock runs further, the code register flip-flop retains the set value as FF2 output goes to zero (D-flip flop positive edge triggered). This process is repeated for each of the flip-flops until after N-clock cycles a high state comes out of sequencer flip-flop controlling the code register least significant bit [LSB] flip-flop.

4. SYSTEM IMPLEMENTATION

4.1 Implementation of Split DAC

The schematic of 10 bit split DAC architecture is shown in Fig.9. In this a unit capacitance of 2.5fF is used. Attenuation capacitor of 2.5806fF is used to separate LSB capacitor array and MSB capacitor array. On MSB side input bits are D_9, D_8, D_7, D_6, D_5 and LSB side input bits are D_4, D_3, D_2, D_1, and D0. On MSB side each capacitor value is divided into two half capacitors connected in parallel and one half of the capacitance is connected to ground potential and other half capacitance is connected to corresponding input bit as shown in Fig. 10. This is done in order to reduce the voltage on the top node of the LSB side of the SPLIT DAC. This increasing of node voltage happens when DAC is connected in integrated SAR ADC. The symbol view of split DAC is shown in Fig. 11.

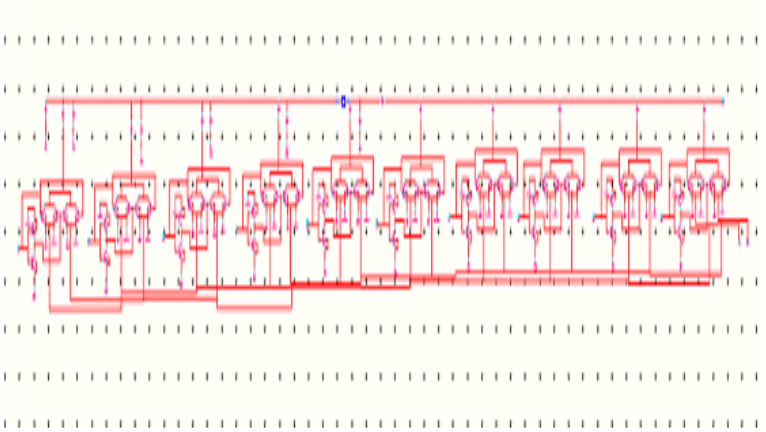


Figure 9. Schematic of 10 Bit Split DAC

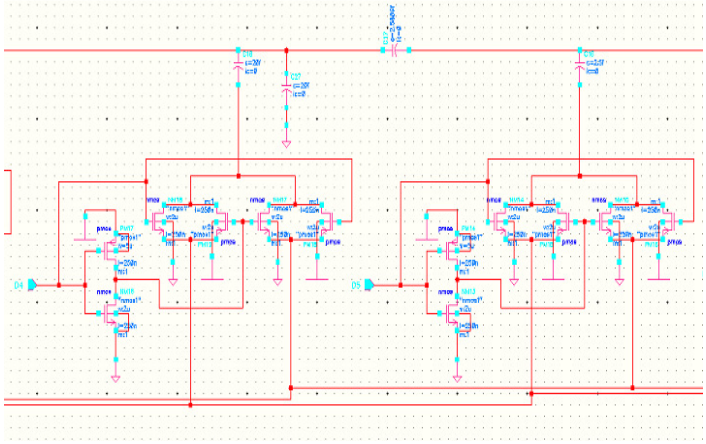


Figure 10. Circuit of Split DAC for 1Bit on LSB and 1 Bit on MSB side.

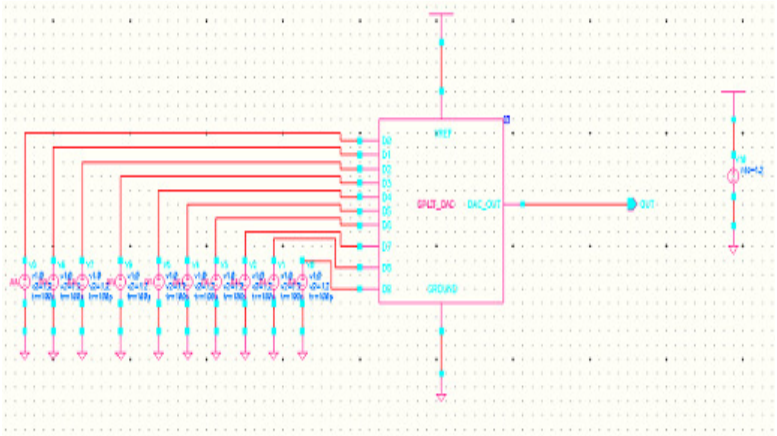


Figure 11. Symbol of Split DAC

4.2 Implementation of SAR ADC

The 10-bit SAR ADC using split DAC architecture is as shown in Fig. 12. The Fig. 12 consists of sample and hold circuit, comparator, SAR block and split DAC array. For this circuit analog signal of peak to peak amplitude of 1.2V with an offset of 600mV and frequency of 100 KHz is applied. The sampling signal of clock period is 1us and high voltage of 1.2V and low voltage of 0V is given. The clock signal of SAR block is 50ns, high voltage level of 1.2V and low voltage level of 0V.

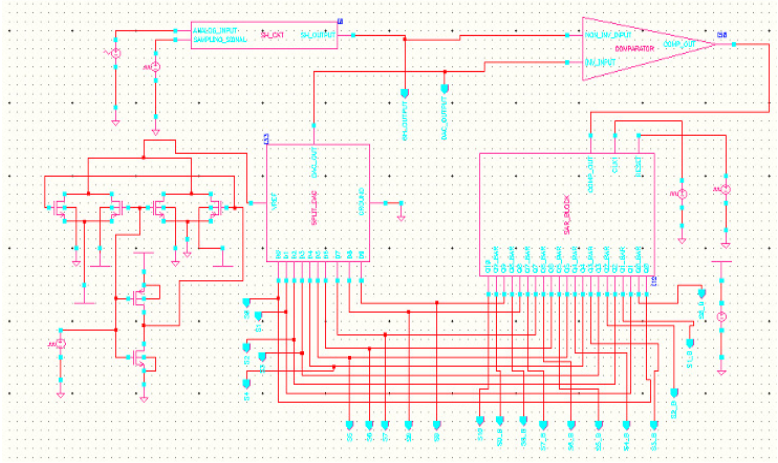


Figure 12. SAR ADC schematic using Split DAC

5. EXPERIMENTAL RESULTS

The simulation results of 10 bit split DAC architecture is shown in Fig. 13. Table I mentions 10 input samples and corresponding outputs in hex form of SAR ADC using split DAC. The simulation results of 10-Bit SAR ADC using split DAC are shown in Fig. 14. Table II & Table III mention power consumed in watts and in % by each block of SAR ADC using split array DAC and binary weighted DAC respectively. Total power consumed by SAR ADC using split DAC is 95.65114uW and SAR ADC using binary weighted DAC is 211.1908uW.

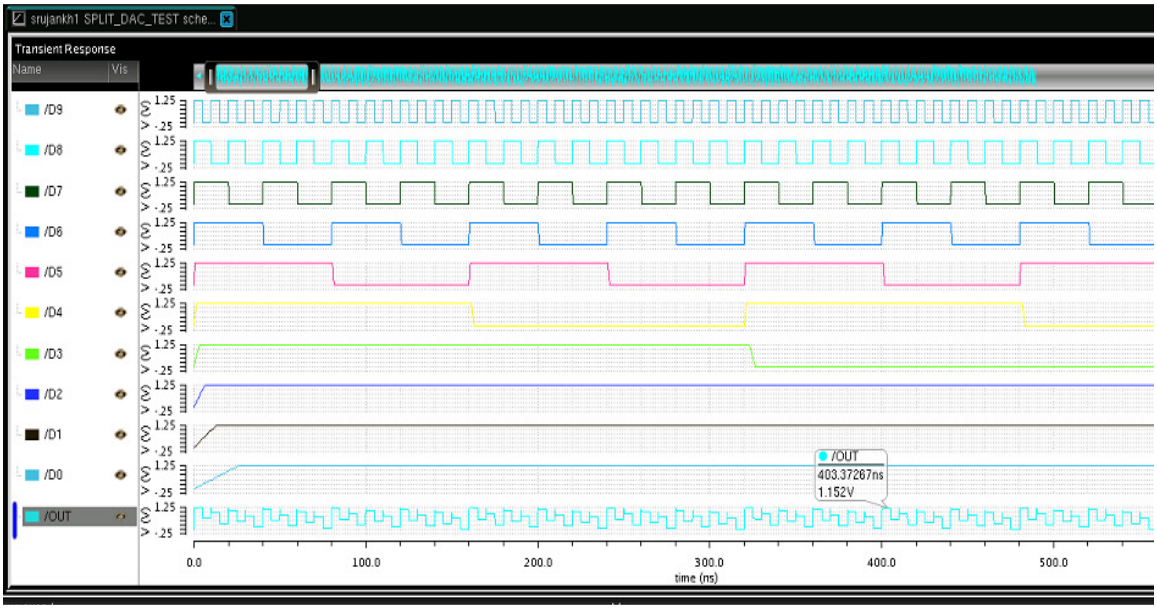


Figure 13. output waveforms of Split DAC

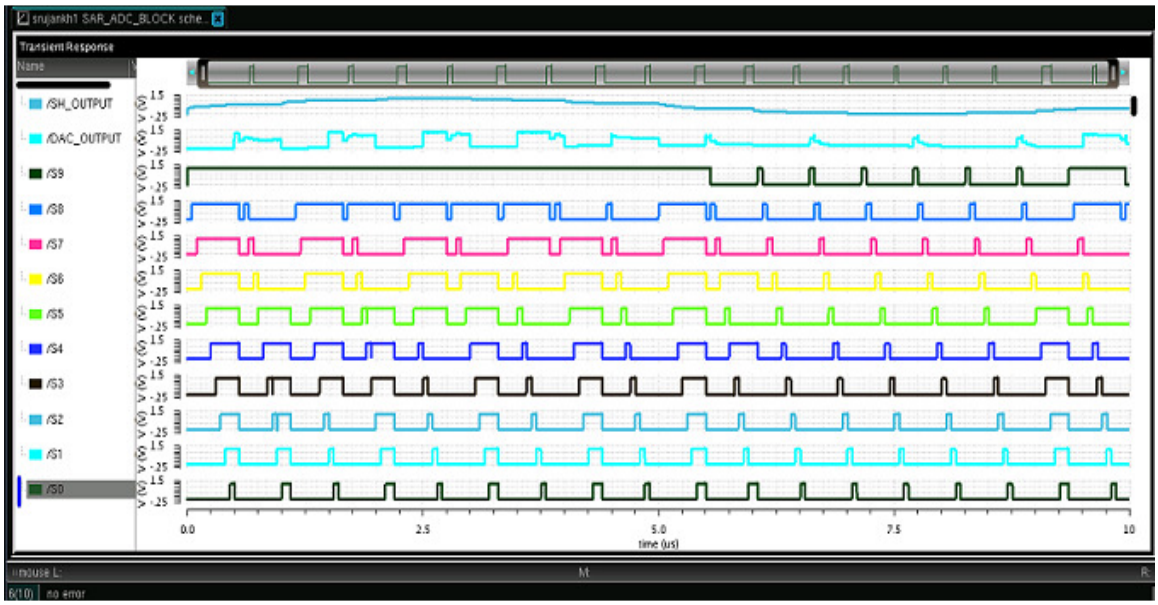


Figure 14 Output waveforms of Split DAC ADC

TABLE I: Input sine wave Samples and corresponding output of SAR ADC using split DAC.

Time	Sample and Hold circuit output	Split DAC output	SAR ADC OUTPUT in HEX
1us	754.4mV	706.1mV	23E
2us	1.095V	1.06V	338
3us	1.19V	1.174V	370
4us	1.089V	920.1mV	2C0
5us	802.1mV	801.4mV	200
6us	418.4mV	362.0mV	051
7us	115.3mV	245.7mV	004
8us	18.9mV	210.1mV	018
9us	113.9mV	188.9mV	040
10us	411.6mV	460.03mV	100

TABLE II: Power consumption of each block of SAR ADC using Split DAC.

Different blocks of SAR ADC	**Power consumed**	**% of Power consumped**
Sample and Hold Circuit	21.4487nW	0.0224
Comparator	10.4799uW	10.9563
Successive Approximation Logic	63.4359uW	66.3200
Split Digital to Analog Converter	17.4600uW	18.2538
Power Saving Circuit	4.2539uW	4.4473
Complete SAR ADC	95.65114uW	100

TABLE III: Power consumption of each block of SAR ADC using binary weighted DAC.

Different blocks of SAR ADC	**Power consumed**	**% of Power consumped**
Sample and Hold Circuit	21.4487nW	0.0101
Comparator	10.4799uW	4.9622
Successive Approximation Logic	63.4359uW	30.0372
Binary Weighted capacitor Digital to Analog Converter	132.9997uW	62.9760
Power Saving Circuit	4.2539uW	2.0142
Complete SAR ADC	211.1908uW	100

6. CONCLUSION

The designed 10 Bit, 2MS/s Successive Approximation ADC using Split DAC architecture is simulated using GPDK 0.18um CMOS technology and compared power consumption of this architecture with SAR ADC using binary weighted DAC architecture. Dynamic range for this architecture is 60.19dB. The charge redistribution DAC in a Split capacitor configuration has a total capacitance which is 96.87% smaller compared to a conventional design. Hence split array DAC occupies smaller area. The power consumed by SAR ADC using binary weighted DAC is 211.1908uW and Split DAC is 95.65114uW. Hence power consumed by SAR ADC using split capacitor configuration is less. Power consumed by each block of SAR ADC using split DAC and SAR ADC using binary weighted DAC are mentioned in Table II and Table III. Power consumption of binary weighted DAC is 132.9997uW and split DAC is 17.46uW.

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