SAF ANALYSES OF ANALOG AND MIXED SIGNAL VLSI CIRCUIT: DIGITAL TO ANALOG CONVERTER

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ABSTRACT

Digital to analog converter is widely used mixed-signal circuit. Testing of analog and mixed signals faces lots of challenges due to the wide range of circuits and unavailability of one appropriate fault model. SAF (stuck_at_Fault), Stuck_open and stuck_short fault model at transistor level is used in this paper. Further these fault models are used to analyze the effects on the characteristics parameter of 3-bit R-2R DAC.

KEYWORDS

Stuck_open, Stuck_short, testing, DAC, fault.

1. INTRODUCTION

Nowadays System on Chip (SoC) contains analog and mixed-signal (AMS) circuits. Wide range of AMS circuits are available. In last few decades the testing of digital ICs are fully explored. SoC consisting analog and mixed signals brings lots of challenges in testing [1]. AMS testing strongly depends on circuits. Limited controllability and observability increases the testing efforts of these AMS circuits. Testing of these AMS circuits can become limiting factor in contributing to manufacturing cost [2]. Also the reliability and performance of AMS circuits can be degraded due to sensitivity to small imperfections during the steps of the fabrication process and high integration density.

Analog to Digital Converter (ADC), Digital to Analog Converter (DAC) and Phase Locked Loop (PLL) are the examples of AMS circuits. The DAC is one of the most widely used mixed-signal integrated circuits as an interface between digital processing systems. Test of data converters like ADC and DAC is most challenging problems in testing of AMS circuit test.

Measurement equipment with high precision than the Device under Test (DUT) is required in conventional DAC test to characterize the performance of the DUT. This makes the design and manufacturing of the tester really a challenge and introduces high test costs [3].

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Analog and AMS circuit testing can be perform in two ways Simulation before test and simulation after test [4]. Simulation-before-test and simulation-after test, these two strategies were proposed in [5]. Simulation-before-test approaches begin with a fault list. The faults are then simulated to determine the corresponding responses to predetermined stimuli. Faults are consequently diagnosed by comparing simulated and observed responses. Simulation-after-test approaches begin with the failed responses, which are then used to estimate faulty parameter or component values.

In this paper, the fault models for AMS circuit is discussed. This paper also discusses the performance parameter of R-2R DAC and its CMOS implementation using 350nm technology. The simulation of 3-bit R-2R DAC for various transistor stuck_open and stuck _short are carried out. The paper is arranged as follows, section 2 describes the fault models for analog circuits. Basics of DAC and the simulation carried out for DAC are described in section 3. Section 4 covers all simulation results. Paper is concluded in section 5.

2. FAULT MODELS

Continuance and discreteness fundamentally distinguish analog from digital signals. Both in time and amplitude domains, the analog signals are continuous. Digital signals are discrete in both domains. Also digital signals are mostly binary, with VDD for logical high and GND for logical low. Mixed signals are quantization of analog signals [6]. Single Stuck_at Faults (SSF) are simple and effective. In industry SSF model is widely used fault model for digital ICs. Because of the wide range of analog and AMS circuits, no as such simple and effective fault model is available for them. Also no as such acceptable fault model is available.

Two categories of fault models are considered hard fault and soft fault [7]. They are defined according to the degree of faulty effects, to simplify fault modeling and fault simulation efforts.

Defects can occurs during the manufacturing process. If defects alter the circuit schematics then they are categories as hard faults. Dust particles during the metallization process can cause an opening or a short of metal wires. Fig. 1 shows the hard faults like open, short, extra device, and missing device.

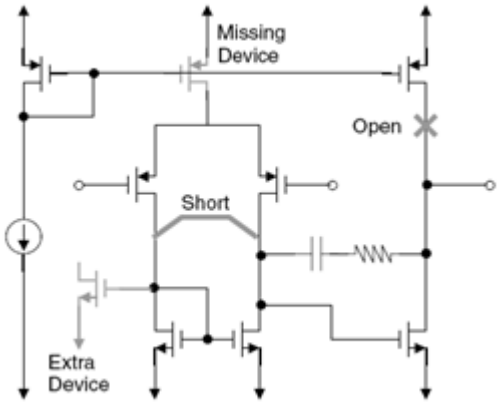


Figure 1. Hard Faults

Soft faults are those faults in which defect are too minor to cause hard faults. Device parameters may get change in soft faults. For example dust can block the poly silicon gate hence shorten the channel length of transistor. Soft faults are also classified into parametric faults and deviation faults. Parametric faults are used to model the variation in the parameter and Deviation faults refer to changes in the overall performance of the entire circuit.

3. DIGITAL TO ANALOG CONVERTER

Digital-to-analog converter is a device for converting a digital signal to an analog signal like binary code into current or voltage. The R-2R Ladder DAC is a binary weighted DAC that creates each value with a repeating structure of 2 resistor values namely R and 2R. CMOS implementation of R-2R DAC using 350nm technology is implemented to observe the fault free characteristics parameters DNL, INL, offset error and gain error. CMOS implementation of 3-bit R-2R DAC is shown in Fig.2.

This DAC converter converts all combinations of 3 bits from digital form into correspondent "staircase" voltage levels. The response of DAC is shown in Fig.3. All the simulation have been done using Mentor Graphics tools using CMOS 350nm technology [8].

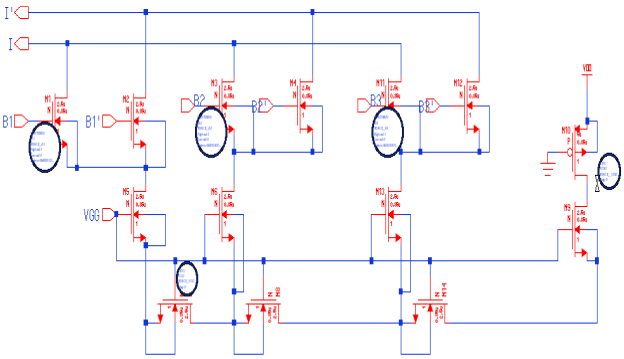


Figure 2. 3-bit R-2R DAC

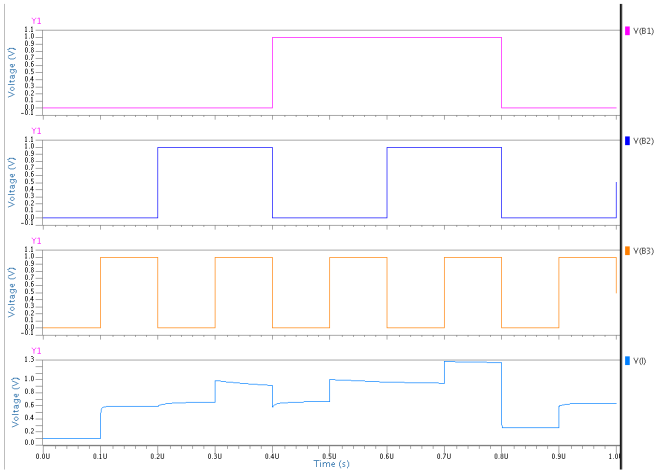


Figure 3. Response of 3-bit R-2R DAC

Differential nonlinearity (DNL) and integral nonlinearity (INL) are two characteristics parameter shows the nonlinearity errors in a DAC. DNL is the maximum deviation in the output steps from the ideal value of one least significant bit (LSB). INL is the maximum deviation of the output transfer curve from a linear transfer curve which is defined as a fit line passing through the end points.

For an n-bit DAC, each analog output V_k corresponds to a digital input k, where k is from 0 to $2^n - 1$. Linear transfer curve and the value of one LSB is defined by fit line through the two end points namely V_0 and V_{2^n-1}. LSB, DNL and INL are defined by the equation 1, 2 and 3 respectively.

$$LSB = \frac{V_{2^{n-1}} - V_0}{2^n - 1} \tag{1}$$

$$DNL(k) = \frac{V_{k+1} - V_k}{LSB} - 1 \tag{2}$$

$$INL(k) = \frac{V_k - V_0}{LSB} - k \tag{3}$$

A gain error exists if the slope of the best line through the transfer curve is different from the slope of the best line for the ideal case. For the DAC the gain error becomes,

Gain error =Ideal slope - Actual slope

The analog output should be 0V when all the digital input bits are 0. However, an offset exists if the analog output voltage is not equal to zero. This error called as offset error which is similar to offset of operational amplifier.

Ideal 1 LSB step width=$V_{ref}/2^N$ =0.158, where V_{ref} =1.27, N=3. Table 1 shows DNL values calculated from actual input and output. Fig. 4 shows the DNL for 3-bit R-2R DAC without any stuck_open and stuck_short fault.

Table 1. DNL values

Input	Actual Output	DNL
000	0.10	0
001	0.27	0.162
010	0.59	-0.028
011	0.72	-0.128
100	0.75	-0.078
101	0.83	-0.018
110	0.97	0.142
111	1.27	0

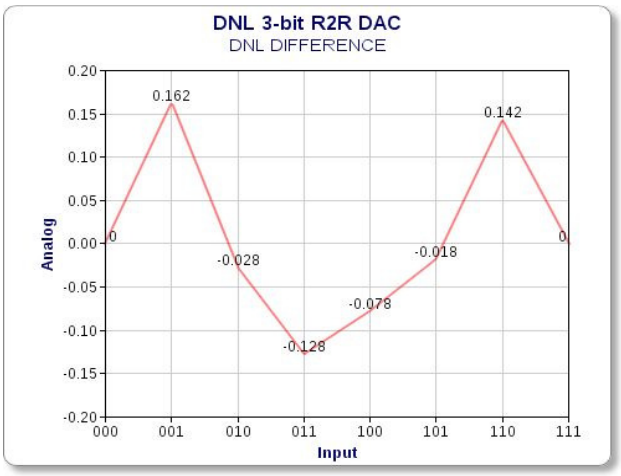


Figure 4. DNL for 3-bit R-2R DAC

MAX DNL=0.162

GAIN ERROR= $[(V_{111}-V_{os})/(V_{ref}-1LSB) -1]*100$
$= [(1.27-0.1)/(1.27-0.158) -1]*100$
$= +5.20\%$

OFFSET ERROR=0.1V

Table 2 shows INL values calculated from actual and ideal output. Fig. 5 and Fig. 6 shows the INL and INL differences for 3-bit R-2R DAC respectively without any stuck_open and stuck_short fault. MAX INL=0.227

Table 2. INL values

INPUT	ACTUAL OUTPUT (V)	IDEAL OUTPUT (V)	INL
000	0	0	0
001	0.27	0.181	0.089
010	0.59	0.363	0.227
011	0.72	0.544	0.176
100	0.75	0.725	0.025
101	0.83	0.906	-0.076
110	0.97	1.087	-0.117
111	1.27	1.27	0

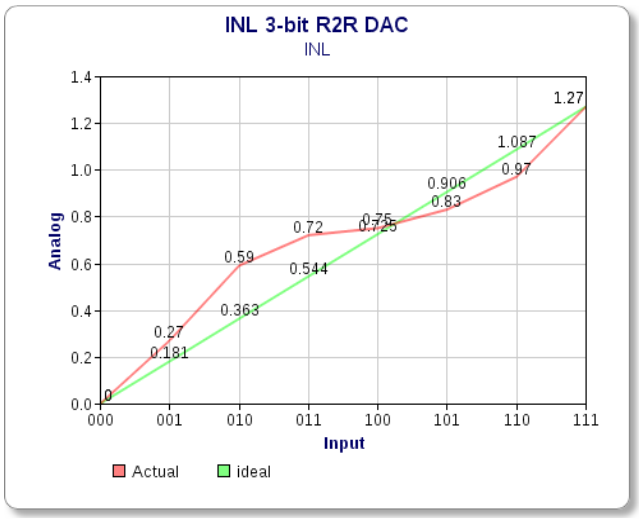


Figure 5. INL for 3-bit R-2R DAC

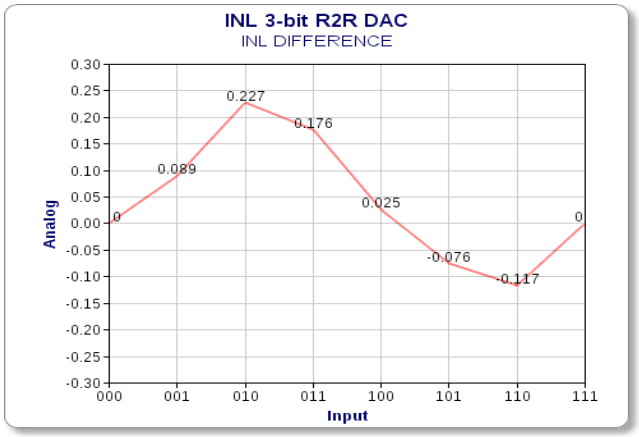


Figure 6. INL difference for 3-bit R-2R DAC

4. FAULT SIMULATION

The defect for ideal MOS as switch is modeled as a switch being permanently in the either open or the shorted state [9].

Stuck_open and stuck_short fault models assumes just one transistor to be open or short. In this paper fault simulations are perform for 3-bit R-2R DAC considering stuck_open and stuck_ short. The effects of these faults are observed for various characteristics parameters of DAC like DNL, INL, gain error and offset error. Fig. 7 and Fig. 8 shows the response in case of M1 as open and M1 as short respectively for the DAC shown in Fig. 2.

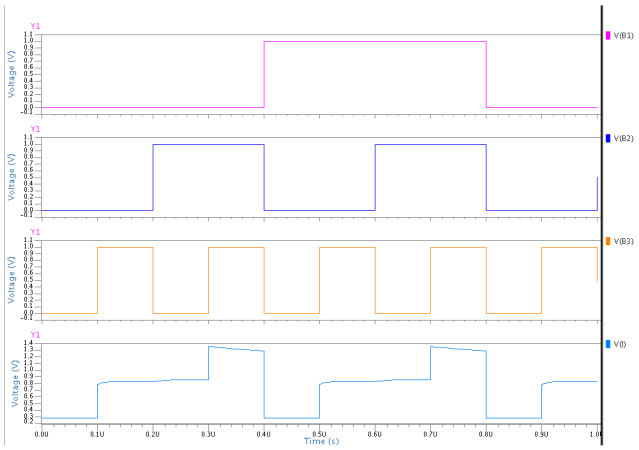


Figure 7. Simulation result of R-2R 3-bit DAC (M1 open)

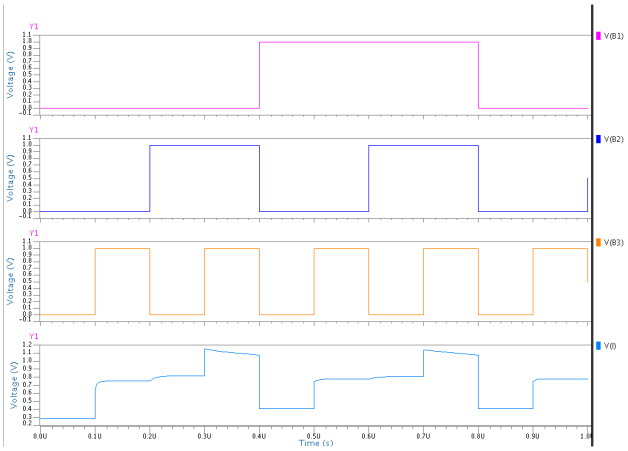
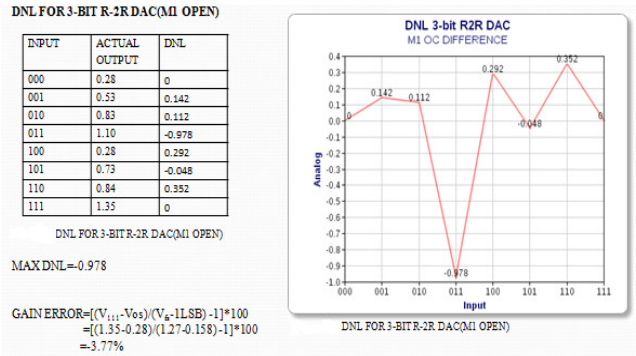


Figure 8. Simulation result of R-2R 3-bit DAC (M1 short)

The effects of M1 as stuck_open is observed and characteristics parameter are calculated. This is summarized in Fig.9 and Fig.10. Also Fig. 11 and Fig. 12 shows changes in parameter when M1 is stuck_short.



DNL FOR 3-BIT R-2R DAC(M1 OPEN)

INPUT	ACTUAL OUTPUT	DNL
000	0.28	0
001	0.53	0.142
010	0.83	0.112
011	1.10	-0.978
100	0.28	0.292
101	0.73	-0.048
110	0.84	0.352
111	1.35	0

DNL FOR 3-BIT R-2R DAC(M1 OPEN)

MAX DNL=-0.978

GAIN ERROR=[(V_{111}-Vos)/(V_8-1LSB) -1]*100
=[(1.35-0.28)/(1.27-0.158)-1]*100
=-3.77%

Figure 9. Effect on DNL for 3-bit R-2R DAC (M1 open)

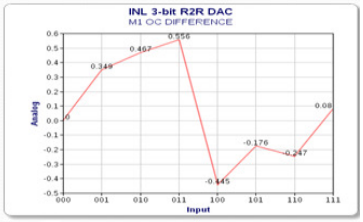
INL FOR 3-BIT R-2R DAC(M1 OPEN)
OFFSET ERROR=0.28

INPUT	ACTUAL OUTPUT	IDEAL OUTPUT	INL
000	0	0	0
001	0.53	0.181	0.349
010	0.83	0.363	0.467
011	1.10	0.544	0.556
100	0.28	0.725	-0.445
101	0.73	0.906	-0.176
110	0.84	1.087	-0.247
111	1.35	1.27	0.08

INL FOR 3-BIT R-2R DAC(M1 OPEN)

MAX INL=0.556

INL FOR 3-BIT R-2R DAC(M1 OPEN)



INL DIFFERENCE FOR 3-BIT R-2R DAC(M1 OPEN)

Figure 10. Effect on INL for 3-bit R-2R DAC (M1 open)

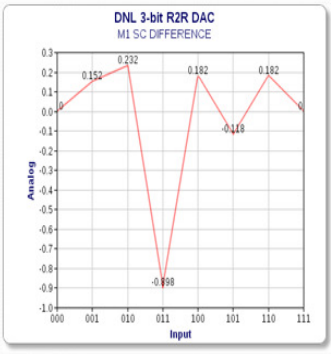
DNL FOR 3-BIT R-2R DAC(M1 SHORT)

INPUT	ACTUAL OUTPUT	DNL
000	0.28	0
001	0.45	0.152
010	0.76	0.232
011	1.15	-0.898
100	0.41	0.182
101	0.75	-0.118
110	0.79	0.182
111	1.13	0

DNL FOR 3-BIT R-2R DAC(M1 SHORT)

MAX DNL=-0.898

GAIN ERROR=[(V_{111}-Vos)/(V_R-1LSB) -1]*100
=[(1.13-0.28)/(1.27-0.158)-1]*100
=-23.56%



DNL FOR 3-BIT R-2R DAC(M1 SHORT)

Figure 11. Effect on DNL for 3-bit R-2R DAC (M1 short)

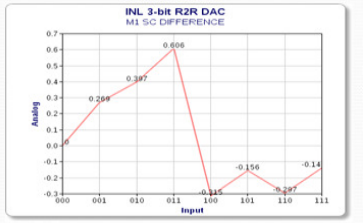
INL FOR 3-BIT R-2R DAC(M1 SHORT)
OFFSET ERROR=0.28

INPUT	ACTUAL OUTPUT(v)	IDEAL OUTPUT(v)	INL
000	0	0	0
001	0.45	0.181	0.269
010	0.76	0.363	0.397
011	1.15	0.544	0.606
100	0.41	0.725	-0.315
101	0.75	0.906	-0.156
110	0.79	1.087	-0.297
111	1.13	1.27	-0.14

INL FOR 3-BIT R-2R DAC(M1 SHORT)

MAX INL=0.606

INL FOR 3-BIT R-2R DAC(M1 SHORT)



INL DIFFERENCE FOR 3-BIT R-2R DAC(M1 SHORT

Figure 12. Effect on INL for 3-bit R-2R DAC (M1 short)

The faults are manually created for various MOS for the DAC shown in Fig.2. The effects of these stuck_open and stuck_short faults are observed for various characteristics parameters of DAC like DNL, INL, gain error and offset error. These are summarized in table 3.

Table 3. Stuck_open and stuck_short fault analyses for 3-bit R-2R DAC

STUCK AT FAULT	DNL (MAX) (V)	INL (MAX) (V)	OFFSET ERROR	GAIN ERROR (%)
Non Faulty	0.162	0.227	0.10	+5.20
M1 Stuck_at_open	-0.978	0.556	0.28	-3.77
M1 Stuck_at_short	-0.898	0.606	0.28	-23.56
M3 Stuck_at_open	-0.708	0.609	0.28	-5.57
M3 Stuck_at_short	-0.618	0.689	0.28	-24.46
M11 Stuck_at_open	0.312	0.387	0.28	-29.85
M11 Stuck_at_short	0.342	0.417	0.28	-10.97

5. CONCLUSION

We have carried out the fault analyses on CMOS 350nm 3-bit R-2R Digital to Analog Converter. The stuck_open and stuck_short transistor fault model is used for the fault analyses. Characteristics parameter of DAC has been observed for the stuck_open and stuck_short transistor faults. By observing the variations in the characteristics parameters we can claim the existence of respective faults. This analyses will helpful for the testing of DAC.

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