LOW POWER, LOW NOISE AMPLIFIERS DESIGN AND ANALYSIS FOR RF RECEIVER FRONT END USING 90NM CMOS TECHNOLOGY USED FOR WIMAX APPLICATIONS

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ABSTRACT

This work is mainly to ensure the reliability of low power low noise amplifier design and analysis which is useful for 4G receiver front ends in particularly WIMAX applications. The low noise amplifiers implemented by using different topologies namely (a) Cascoded Common source amplifier technique(b) Folded Cascode amplifier technique (c) Shunt feedback amplifier technique (d) Current reuse Common gate amplifier with gm boosted technique with 90 nm TSMC CMOS technology, which is used for WIMAX applications with 1V supply. In order to simulate and measurement the parameters such as Scattering parameters(S21, S12 S11. S22),noise-figure, input matching, output matching ,stability, linearity the Cadence ,Agilent technologies ADS and lab view graphical software have been used and Compare the performance of the various parameters .

KEYWORDS

RF CMOSLNA, WIMAX, soc , noise figure

1. INTRODUCTION

The communication system that comprises of transmitter and receiver will experience not only attenuation but also the interference at the receiver end. The signal strength will be normally in milli-volt range hence unable to drive the demodulator circuitry; therefore it is mandatory to amplify the signal before giving it to the demodulator circuit. But the amplifier will not only amplify the signal but also amplify the noise as well. Hence amplifier with minimum noise addition is required. So LNA is essential and first active block in receiver front end[1]

The emerging wireless consumer market has experienced a remarkable improvement since the introduction of the first modern mobile phone systems, new application areas, high data rates and increase in the number of subscribers, a prime goal of the IC manufactures is to provide low cost solutions. The wireless communication area network standards, such as WIMAX, Bluetooth, Wi-Fi technologies of all the components make it possible to integrate on a single silicon chip

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including transceiver sections .So the SOC (system on chip)solution to enable with CMOS technology [2].

WIMAX is a trade mark for a family of wireless communication protocols that provide fixed and mobile internet access .This is a wireless communication system also known as IEEE 802.16 family standard .WIMAX is a internet protocol based similar to 802.11/Wi-Fi networks with the coverage and quality service of cellular networks WIMAX can provide broad band wireless access up to 30 miles for fixed stations and 3-10 miles for mobile stations .Data rates up to 40MB/s for mobile stations and,1gb/s for fixed stations.[3].

This paper summarises as follows ,Section 2 describes the topologies of the implemented low power low noise amplifier .Section 3 represents the proposed circuit design. The analysis of simulation measured results presented in section 4 the conclusions in section 5 followed references in Section 6.

2. LOW NOISE AMPLIFIERS

LNA (low noise amplifier) is a crucial element which is used in front end circuit of receiver because of its gain and noise characteristics are closely related to the system sensitivity and dynamic range. Receiving multiple signals at different power levels over different frequency ranges .It gives low noise and high linearity .The maximum power gain 50 ohm termination for proper operation and can route the LNA to the antenna which is located an unknown distance away without worrying about the length of the transmission line.

2.1. Cascoded CS (common source) amplifier topology

This is widely used architecture as shown in fig .1 cacode technique with inductive degenerated topology was improved the isolation between input and output matching along with enhancement of gain of the amplifier as shown in fig ,the cascade transistor Q_2 reduces the voltage gain of Q_1.So that it improves the reverse isolation [6] and also Q_2 transfers the current I_d ,to R_L by providing the gain equal to the basic common source, by reducing the parasitic capacitances ,it improves the performance of the amplifier at higher frequencies with reducing Miller effect.

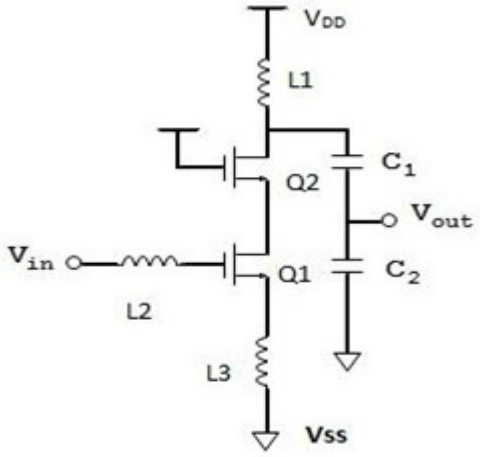

Figure 1 : Cascoded CS (common source)amplifier topology

2.2. Folded cascode amplifier topology

Folded cascode topology is used for very low voltage application as shown in fig 2. It has low operated supply voltages as the PMOS and NMOS transistors are placed in parallel between the ground rail and supply .The PMOS cascode transistorQ_2 reduces the input capacitance and offers good reverse isolation with better stability [7]. Improved trans-conductance, gain and slew rate by reducing the bias current of ideal deice.

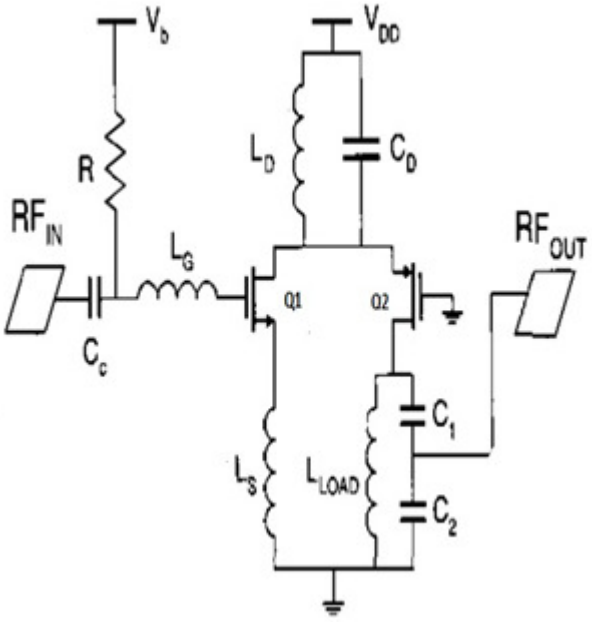

Figure2: Folded cascode amplifier topology

2.3 Shunt feedback low noise amplifier topology

The resistive shunt feedback provides wideband input and output matching with low noise figure(NF) degradation by reducing the Q factor of the narrow band LNA input and flatters the pass band gain as shown in fig(3),it is able to attain a very high linearity [8] improves the gain, which is set by feedback .The feedback components are combination of a resistor in series with a capacitor which increases the bandwidth and gain with linearization. The high input impedance and high frequency performance improved to MOSFETS by providing an additional inductor can be placed in series with the capacitor and resistor [8].The band pass filter connected at input includes the input impedance of a cascode amplifier improves the better performance with low power dissipation but due to this band pass filter the chip area is high and noise figure degradation.

2.4. Current reuse Common gate amplifier topology

As shown in fig (4) ,the current reuse common gate LNA has better reverse isolation compare with common source LNA .The purpose of a CG input stage improves stability over the design of common source LNA. It attains noise and gain performance comparably low power and less chip area by the current reverse technique with boosting gm. The dual inductive degeneration and resistive current reuse techniques are superimposed in the first stage for broad band, noise and

input impedance matching[6].To improve bandwidth the inductive degenerated technique is implemented in the second stage .By combining a NMOS and PMOS transistor between the supply rails as shown in fig 4.

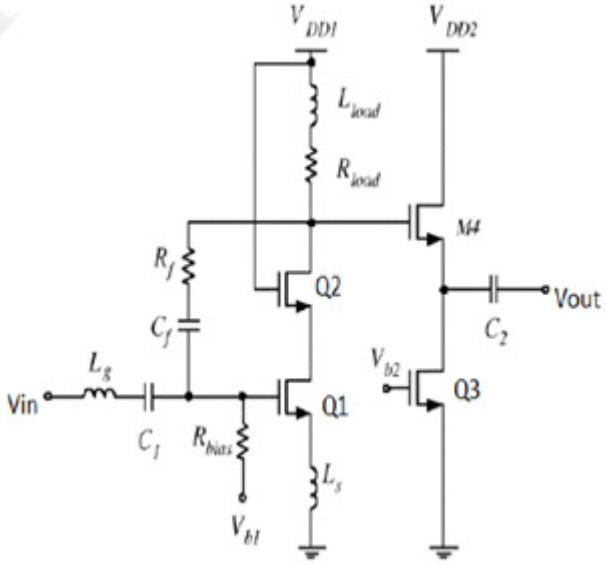

Figure 3 : Shunt feedback low noise amplifier topology

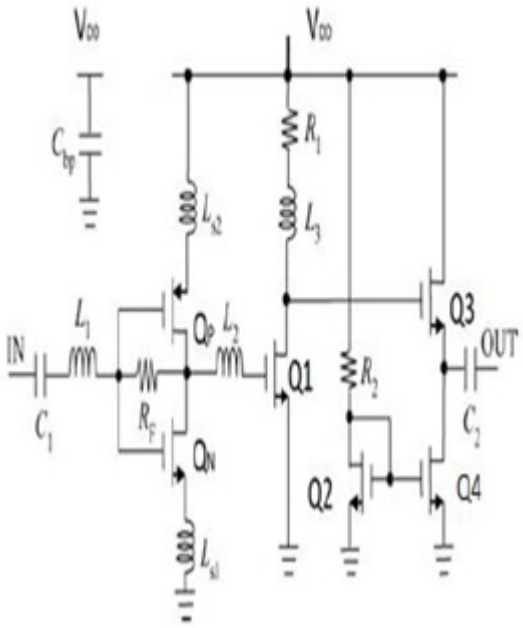

Figure :4 Current reuse Common gate amplifier topology

3. PROPOSED CIRCUIT DESIGNS

The WIMAX receiver performance specifications requirements are shown in table 1.According to IEEE 802.16 family standard the specifications of various parameters.

TABLE I: WIMAX RECEIVER REQUIREMENTS

S.No	PARAMETER	SPECIFICATIONS OF WIMAX
1	Radio technology	MIMO-SOFDMA
2	Range	30 miles
3	Speed	70 Mbps
4	Frequency range	2-10Ghz
5	Receiver maximum input level on channel rejection tolerance	≥30dBm
6	Channel bandwidth	2-20Mhz
7	Noise figure	≤7dB
8	First adjacent channel rejection	≥4dB
9	Second adjacent channel rejection	≥23dBm

The receiver front end specifications requirements are shown in table 2

S.No	Parameter	Low noise amplifier
1	Gain	20dB
2	Noise figure	3dB
3	Linearity	-10dB
4	Input and Output matching	≤-10dB

3.1. Cascoded common source Low noise amplifier:

The input impedance z_{in} equal to

$$Zin = (gm/Cgs).\ L3 + 1/(s.Cgs) + s.(\ L2 + L3) \quad (1)$$

$$\omega 0 = 1/\sqrt{(L2+L3\ .Cgs\ )} \quad (2)$$

$$Zin = (gm/\ Cgs).\ L3 \text{ (At Resonance)} \quad (3)$$

Where g_m is trans conductance, C_{gs} gate to source capacitance, Ls source inductance, L_G gate inductance respectively.

The input impedance reduces as shown in equation computed with the value of L_3 at a resonant frequency shown in fig 5.The degenerating inductor L_3 gives the real input impedance of LNA is computed with the value of L_3 determine the value of gate inductance L_2,that will set the resonant frequency is calculated .In order to reduce the junction capacitance in the layout, the width of the cascode transistor Q_2 set equal to the width of the input transistor. The output matching network was composed of the drain inductor L1 and the output capacitors C1 and C2 will designed.

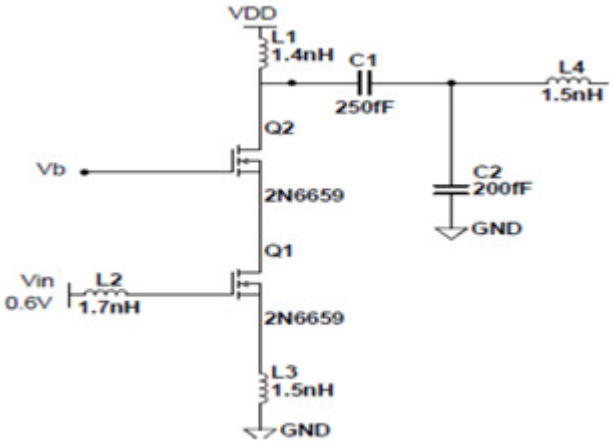

Figure 5 : Cascoded CS (common source) amplifier topology

3.2. Folded cascode amplifier

The input impedance of the folded amplifier is described by the source inductance Ls while gate inductance LG is computed based on the resonant frequency. The inductor LD resonates with drain junction capacitance of Q_1 and the source capacitance of Q_2.The output matching network made by the inductor Lload and capacitor C_1 and C_2 .The schematic shown in fig 6. below.

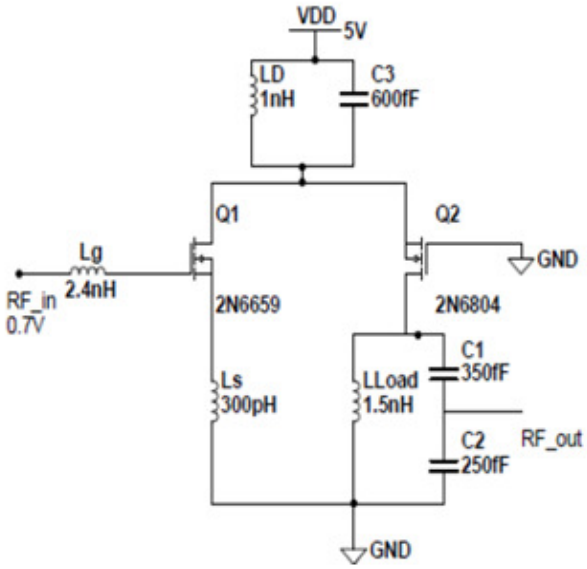

Figure 6 : Folded cascode amplifier topology

3.3.Shunt feedback amplifier topology

The schematic of shunt feedback amplifier shown in fig 6. Power gain can be adjusted by the value of feedback resistor as shown in below equation. Where R_F is feedback resistor ,Z_O output impedance and the transducer gain . Inductor Ls is added for simultaneously noise and input ,output matching and L_G is placed at the gate of the transistor Q_4 to aid in matching .The capacitances CF.C1 and C2 is used for ac coupling purpose .The feedback capacitor for biasing purpose.

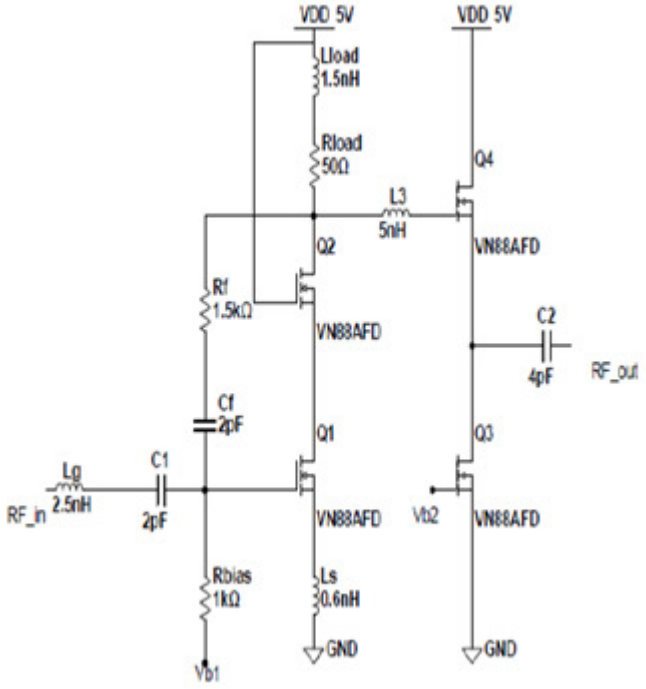

Figure 7 : Shunt feedback low noise amplifier topology

3.4. Current reuse common gate low noise amplifier

The schematic for current reuse common gate LNA shown in fig below 8.The resistive current reuse amplifier utilizes dc current reuse to save the power consumption and to improve trans-conductance g_m to the amplifier .This composed two stages, the first stage of amplifier increases the voltage gain with low power dc supply voltage ,it adopts a current reuse topology with self biasing by a feedback resistor Rf as shown in fig.

The disadvantage of this topology is parasitic capacitances due to this degradation of input impedance and the -3dB bandwidth at high frequency ,to overcome this dual source degenerated inductors (L_{S1} and L_{s2})and inter stage inductor L_2 are proposed for the tuning of the parasitic capacitances .LC network (L1 and C1) combined with dual degenerated inductors (L_{S1} and L_{S2}) for input matching and intrinsic capacitances of current reuse topology to form a multi section LC ladder network to achieve a wideband matching with 50 ohm characteristic impedance.

The total trans-conductance in this stage is g_{mt} is

$$gmT = gmn/(1+j\omega Ls\ 1.gmn)+gmp/(1+j\omega Ls2.gmp) \quad (4)$$

The voltage gainAV1 of the first stage LNA

$$AV1 = gmT.\ [(1+j\omega Ls1.gmn).Ron//\ (1+j\omega Ls2.gmp).Rop//Zin] \quad (5)$$

The input impedance Zin of LNA

$$Zin = j\omega L1 + Zsd//\ Zfb \quad (6)$$

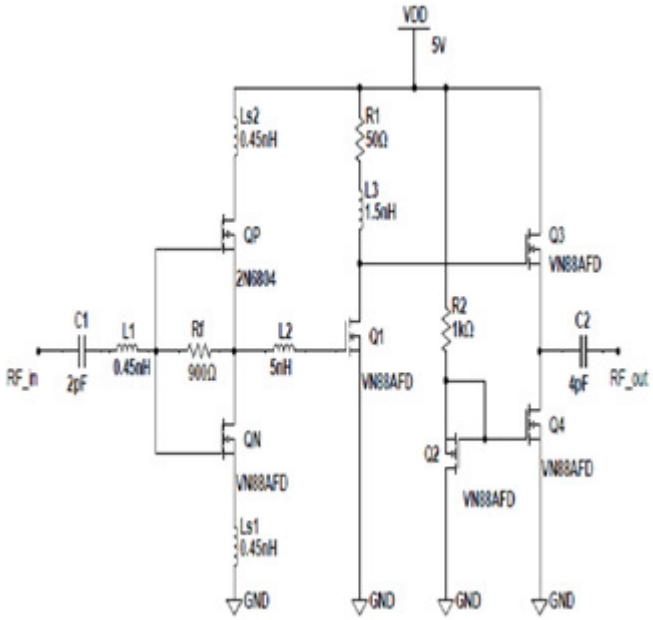

Figure 8 : Current reuse Common gate amplifier topology

4. RESULTS

The LNA topologies designed by using the 90nm CMOS process .The LNAS were designed to operate at the unlicensed national information infrastructure (U-NII) band of 5.75GHz to 5.85 GHz .The measurement taken at 5.8 GHz. The shunt feedback amplifier achieved the highest gain with 20dB followed by the cascaded common source amplifier with 14dB and the folded cascode achieved the lowest gain with a gain of 13dB

The linear zing effect of feedback gives the shunt feedback amplifier its wideband characteristics to the narrow band characteristic of these cascode amplifier. The total double side band noise figure as shown in fig 9.The noise figure of the LNA topologies are 1.7 db for cascoded common source 1.7 dB for the folded cascode and 2.63 dB for the shunt feedback amplifier .The stability factor plot shown in fig 10 . All topologies are un conditionally stable with stability factor larger than 1 at the required frequency.

The simulation S Parameter results for all topologies ,table 3:

S.No	Topology	Frequency (GHz)	Pdc (mw)	Gain (dB)	IIP3 (dB)	Noise figure (dB)
1	Cascaded CS	5.8	20	14	-7.42	1.7
2	Folded cascode	5.8	47.5	13	-6.2	1.8
3	Shunt feedback	5.8	55.5	20	-5.15	2.7
4	Current reuse CG	5.8	16.1	18	-7.35	1.8

S.No	Topology	S_{21} 20	S_{12} -10	S_{11} -10	S_{22} -20
1	Cascaded CS	14	-9.55	-14.5	-23.8
2	Folded cascode	13	-12.4	-9	-26.03
3	Shunt feedback	20	-11.4	-24	-31.24
4	Current reuse CG	18	-9.7	-10.3	-46

According to above table reuse isolation better than -20 dB. The current reuse common gate LNA can achieved -46dB .The third order interception point represents the linearity of the low noise amplifier.

- ---------- Shunt feedback LNA
- ---------- Current reuse Common gate LNA
- ---------- Folded Cascode LNA
- ---------- Cascoded Common source LNA

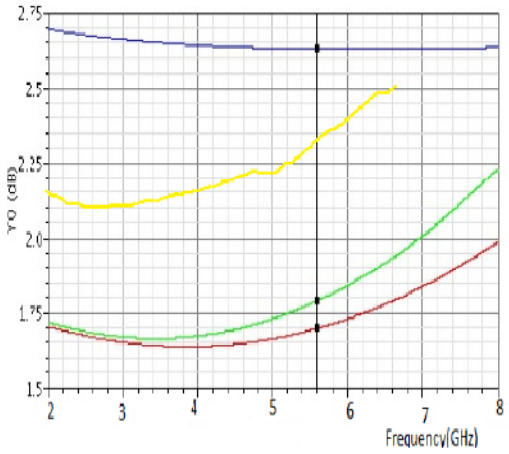

Figure: 9 frequency versus gain

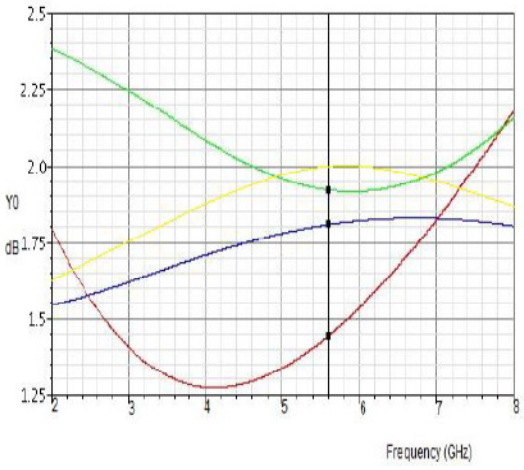

Figure: 10 Frequency versus gain

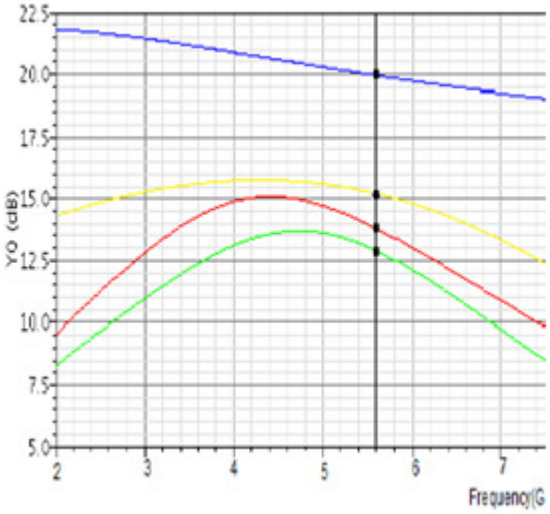

Figure: 11 Frequency versus admittance

4.1.Comparison of various parameters :

From the above comparison table cascoded common source low noise amplifier achieved the best figure of merit .Due to high gain of the shunt feedback amplifier .So the best to use in the front end of receivers is shunt feedback amplifiers.

5. CONCLUSION

A standard CMOS 90nm technology with 1V supply was used for all the topologies of cascoded common source amplifier ,the folded cascoded amplifier, shunt feedback amplifier and current reuse common gate low noise amplifier according to requirements of receiver front end .So that choose the best low noise amplifier depends upon performance of parameters particular low noise amplifier. From this presented work the cascoded common source topology attains lowest noise figure due to better input matching using inductive degeneration .The folded cascode technology is also attained low noise figure .The cascoded common source topology is also attains the lowest power dissipation because of it contains only one current branch. The shunt feedback amplifier attained the highest gain by changing the value of the feedback resistor. The current reuse CG LNA topology is proposed in narrow band LNA designs can successfully extended to UWB purpose because of good linear performance accept the high noise figure comparatively other LNAs.

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