# DESIGN OF QUATERNARY LOGICAL CIRCUIT USING VOLTAGE AND CURRENT MODE LOGIC

Shweta Hajare and Pravin Dakhole

Research scholar Department of Electronics Engineering,
Yeshwantrao Chavan college of Engg, Nagpur, India

***ABSTRACT***

*In VLSI technology, designers main concentration were on area required and on performance of the device. In VLSI design power consumption is one of the major concerns due to continuous increase in chip density and decline in size of CMOS circuits and frequency at which circuits are operating. By considering these parameter logical circuits are designed using quaternary voltage mode logic and quaternary current mode logic. Power consumption required for quaternary voltage mode logic is 51.78 % less as compared to binary . Area in terms of number of transistor required for quaternary voltage mode logic is 3 times more as compared to binary. As quaternary voltage mode circuit required large area as compared to quaternary current mode circuit but power consumption required in quaternary voltage mode circuit is less than that required in quaternary current mode circuit .*

***KEYWORDS***

*Multiple-Valued Logic (MVL), Quaternary voltage mode, Quaternary current mode, MIN, MAX*

## 1. INTRODUCTION

The growth in the IC industry showed an exponential trend over the last decades. As the number of transistors per unit area increases, the industry has faced some new problems. The major problem that the industry must solve to maintain this growth is the interconnections (both on chip and between chips) and the routing of these interconnections. The silicon area that used for these interconnections may be greater than that used for the active logic elements.

The use of circuits with more than two logic levels has been offered as a solution to these interconnection problems. The Multiple-Valued Logic (MVL) circuits, have a potential for reducing chip area consumed by interconnection wiring and functional units in Very-Large Scale Integration (VLSI) . Applying signals having more than two levels to a single wire reduces the number of wires for the same range of data, and this reduction results in a decrease in number of required IC pins. As the interconnection length and number of wires used are reduced, the space between any two wires increases without increasing the tot al silicon area, leading to a decrease in resistance and capacitance of contacts and interconnections, and the interconnection delay can be greatly decreased. According to aspect MVL logic has two basic scheme First scheme accepts MV inputs and produces MV output [1,2]. The internal processing is binary. This scheme is useful when MVL is to be used for reduction of interconnecting complexity. The other scheme accepts binary input and produces binary output. Internal processing is using MV circuits as shown in figure 1 and figure 2.

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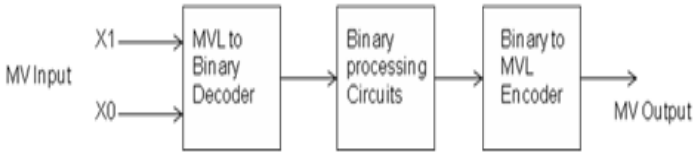


Figure 1. MVL circuit with binary processing

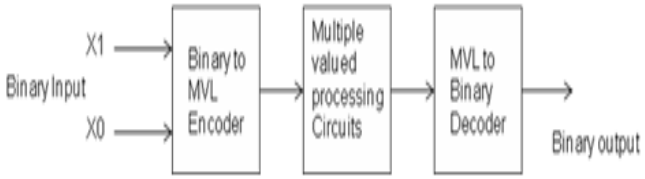


Figure 2. MVL circuit with multi valued processing

In any numerical system, the smaller the radix the larger the number of digits necessary to express a given quantity.

The number necessary to express a range of N is given by

$$N = R^d \quad (1)$$

where R is the radix and d is the necessary number of digits, rounded up to the next highest integer value where necessary.

If it is now assumed that the cost or complexity C of system hardware is proportional to the digit capacity R x d, then

$$C = k (R \times d) \quad (2)$$

$$= k [R \log N / \log R]$$

where k is some constant. Differentiating with respect to R will show that for minimum cost C, R should be equal to e = 2.718. Since in practice R must be an integer, by comparing R = 3 (ternary) would be more economical than R = 2.(binary).

Alternatively, if it is assumed that circuit cost and complexity C for processing one signal line remains constant irrespective of radix, then total system cost C is merely proportional to d. In this case

$$C = k \times d$$
$$= k [\log N / \log R] \quad (3)$$

which is a gradually decreasing cost with increasing radix R[1] Among radix value that are power of 2 ,system based on 4 shows considerable promise .Logic levels for binary ternary and quaternary logic is shown in figure 3.

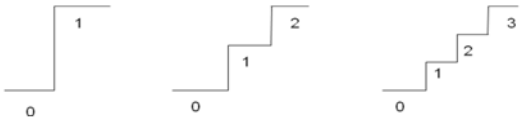


Figure 3 .Logic levels for binary ternary and quateranary logic

Multiple valued logic , Quaternary circuit can be realized as voltage and current mode depending on complexity and operation of the circuit.

Voltage Mode: - In Voltage Mode signal is transmitted by voltage level. Voltage-mode circuits, the information are transferred by voltage levels. Maximum allowable radix of the voltage-mode designs are determine by the supply voltage.

Current Mode: Introduced in 1983, current-mode CMOS MVL circuits were demonstrated that are compatible with the requirements for the very-large-scale-integration (VLSI) of circuits. Certain reference current unit are considered depending on its different logic level values are decided [3].

In this paper first part describe about quaternary logic. Second part describe about design of logical circuit in quaternary voltage and current mode and last part describe about result and conclusion.

## 2. QUATERNARY LOGIC

Quaternary is radix 4 numeral system. It uses the digits 0, 1, 2 and 3 to represent logic levels. It has the ability to represent any real number with a canonical representation [4].

In current mode, levels are decided according to reference current. The proposed design has reference current 5uA and quaternary levels depend on it is as given in Table1.

Table 1. Quaternary current logic levels

| Logic level | Current (uA) |
|---|---|
| 0 | 0 uA |
| 1 | 5uA |
| 2 | 10 uA |
| 3 | 15 uA |

In voltage mode ,levels are decided according to voltage and quaternary levels depend on it is as given in Table 2.

Table 2. Quaternary voltage logic levels

| Logic level | Voltage |
|---|---|
| 0 | 0 V |
| 1 | 1V |
| 2 | 2V |
| 3 | 3V |

# 3. DESIGN OF QUATERNARY LOGICAL OPERATOR

## 3.1 DESIGN OF LOGICAL CIRCUIT USING VOLTAGE MODE

### 3.1.1 QUATERNARY INVERTER

Quaternary inverter consist of 6 transistors three NMOS and three PMOS as shown in figure 4. These NMOS and PMOS are operated at different threshold voltages. If the input value is 0 V, PMOS1 is turned on, which sets the output to 3 V, whereas NMOS1 , NMOS2, and NMOS3 are turned off, cutting the remain paths. When the input value is set to 1 V, PMOS1 is turned off, whereas NMOS2 is turned on, which sets the output to 2 V. When the input value is set to be 2 V, PMOS2 is turned off, whereas NMOS3 is turned on, hence driving the output to 1 V.
PMOS3 turns off and NMOS1 sinks the output to zero only when the input value is set to 3 V [5].

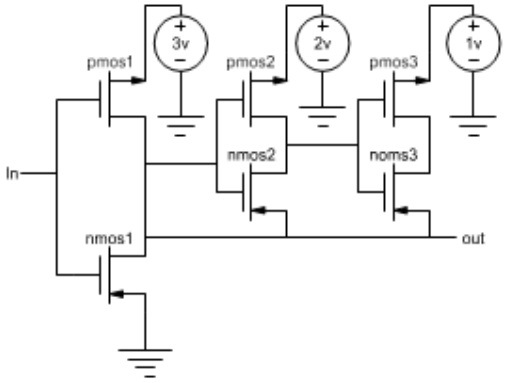


Figure 4 . Design of quaternary inverter [5]

### 3.1.2 DESIGN OF QUATERNARY MIN GATE

In Quaternary logic NMIN gate is nothing but NAND gate in binary logic, MIN gate is the AND gate in binary. In binary AND when the two values are high then only output is high for all other cases it is low. But in case of MIN gate the output sets to the lowest of the input value. Opposite is the function of NMIN gate i.e. NMIN is the not of MIN gate. So the combination of inverter with MIN gate forms NMIN gate , or the MIN gate is form by applying inverter at the output of NMIN gate .The circuit diagram for NMIN gate [5] for is shown in figure 5.

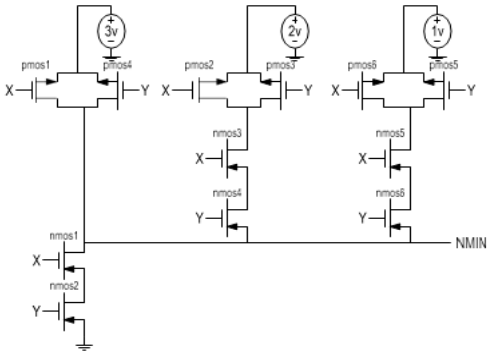


Figure 5. Schematic of Quaternary NMIN gate [5]

### 3.1.3 DESIGN OF QUATERNARY MAX GATE

In Quaternary logic NMAX gate is nothing but NOR gate in binary logic, MAX gate is the OR gate in binary. In binary OR gate when any one value is high then output is high for all other cases it is low. But in case of MAX gate the output sets to the highest of the input value.

Opposite is the function of NMAX gate i.e. NMAX is the not of MAX gate. So the combination of inverter with MAX gate forms NMAX gate , or the MAX gate is form by applying inverter at the output of NMAX gate [5] The schematic diagram for NMAX gate is shown in figure 6.

## 3.2 DESIGN OF LOGICAL CIRCUIT USING CURRENT MODE

### 3.2.1 COMPLEMENTARY OPERATOR

Complementary Operator Act as a basic inverter circuit. Whatever the input is given the inverted result obtained at the output of circuit. It basically defined as

$$\bar{x} = r - 1 - x \tag{4}$$

Where $x$ in input and $x$ is output. Schematic of complementary operator is shown in figure 7.

Table 3. Truth Table of Inverter

| In | 0 | 1 | 2 | 3 |
|---|---|---|---|---|
| Out | 3 | 2 | 1 | 0 |

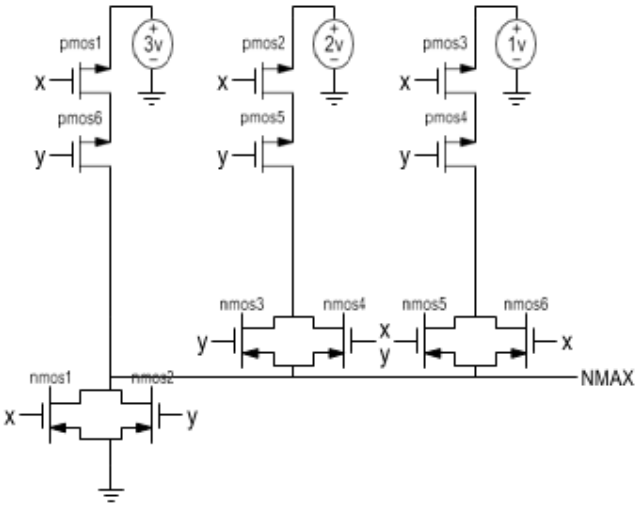


Figure 6. Schematic of Quaternary NMAX gate

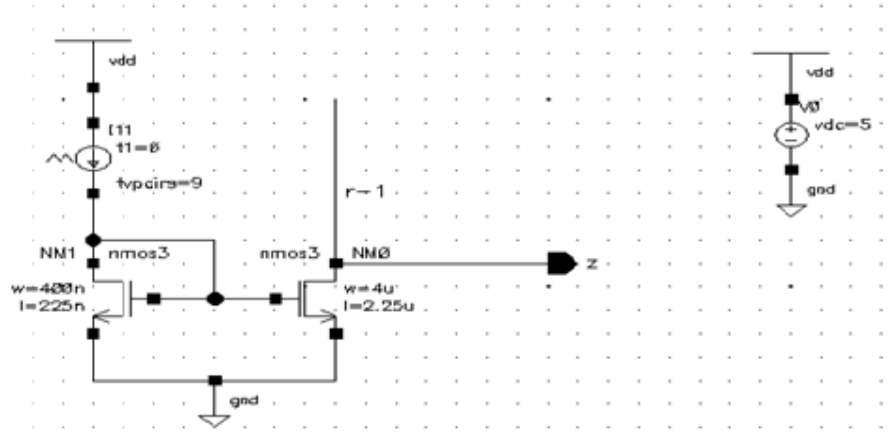


Figure 7.Schematic of complementary operator

### 3.2.2 DESIGN OF MIN GATE

In current mode Min gates [6] act as AND gate, take different input values and give minimum value as an output signal among them. Suppose (x1, x2, x3 …xn) then output we get minimum value among them.

$$\text{Min (in1, in2)} = \text{AND (in1, in2)} = \text{in1} \cap \text{in2} \tag{5}$$

Table 4: Truth Table of Min Gate

| in1 / in2 | 0 | 1 | 2 | 3 |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 |
| 2 | 0 | 1 | 2 | 2 |
| 3 | 0 | 1 | 2 | 3 |

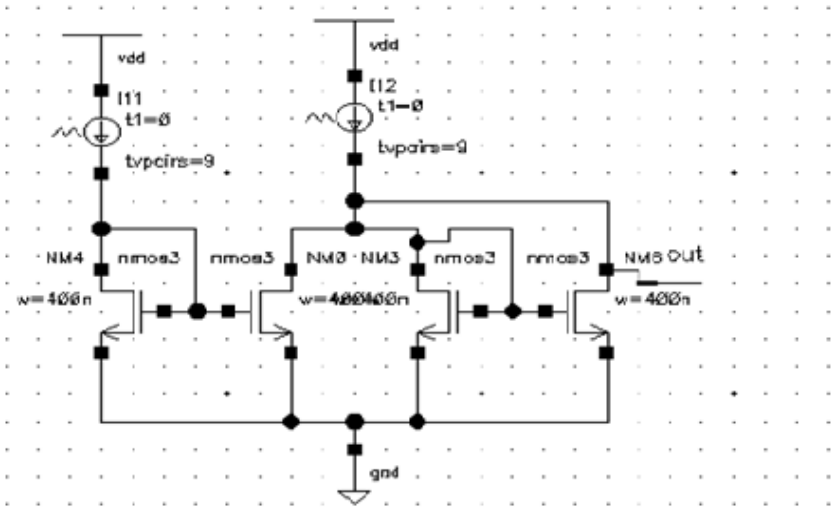


Figure 8. Schematic of Min Gate Circuit

### 3.2.3 DESIGN OF MAX GATE

In current mode Max Gate [6] act as an OR gate, take different input values and give maximum value as a output signal among them. Suppose (x1, x2, x3 …xn) then output we get maximum value among them. Schematic of MAX gate is shown in figure 9.

$$\text{Max}(in1, in2) = \text{OR}(in1, in2) = in1 \cup in2 \quad (6)$$

Table 5. Truth Table of Max Gate

| in1 / in2 | 0 | 1 | 2 | 3 |
|---|---|---|---|---|
| 0 | 0 | 1 | 2 | 3 |
| 1 | 1 | 1 | 2 | 3 |
| 2 | 2 | 2 | 2 | 3 |
| 3 | 3 | 3 | 3 | 3 |

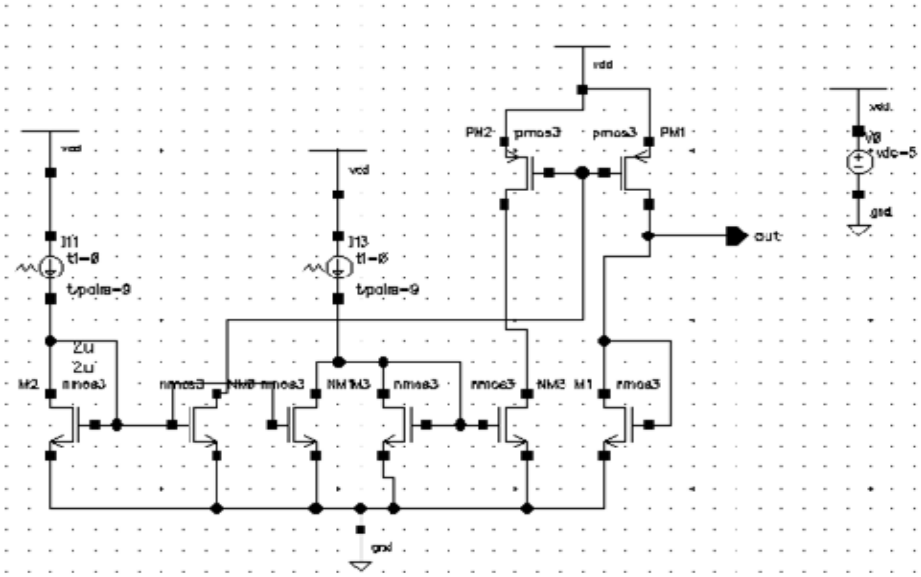


Figure 9. Schematic of Max Gate Circuit

### 3.2.4 DESIGN OF CURRENT COMPARATOR

In Proposed current-comparator Circuits, Input diode-connected NMOS-PMOS transistor pair produces the threshold current. This reference current is mirrored to output as Ith, and input current is mirrored to output as Iin. As the input current is less than the threshold current ,the output of the comparator circuit is at logical HIGH voltage (output node has the same potential with power supply) and As the input current is greater than the threshold current output of the comparator circuit is at logical LOW voltage (output node has the same voltage with the ground). PMOS transistor mirror is applied with the input current, and NMOS with threshold current, produces the inverted version of output voltages, if needed [7].

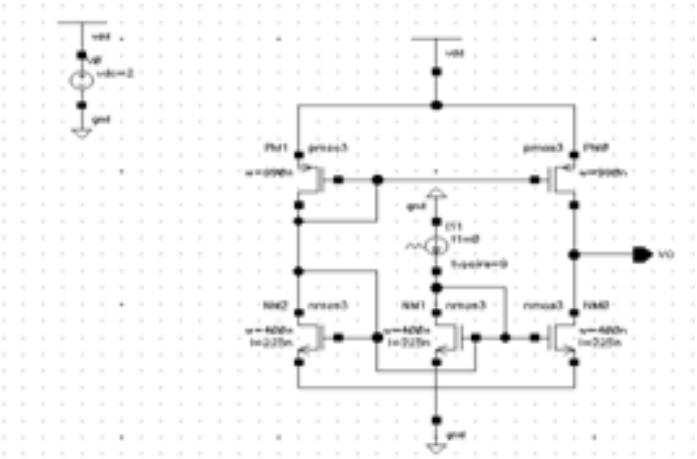

Figure 10. Schematic of comparator Circuit

### 3.3 CAPACITANCE ESTIMATION FOR QUATERNARY INVERTER

The input capacitance of any circuit can be approximated by simply taking the sum of all the gate capacitances which are attached to a particular input signal

Gate Capacitance is given by $C_{gate} = C_{ox} \Sigma_{i=0}^{N}(WL)$ (7)

where Cox is a process parameter

so gate capacitance is calculated as $\frac{C_{gate}}{\Sigma_{i=0}^{N} C_{gate,i}}$ = 0.329fF

Input Capacitance is given by $C_{in}$ = 1.974fF (8)

Gate to drain overlap capacitance is given by $C_{ov}$ = $C_{GDO}$ * W (9)

For PMOS: $C_{ov}$= 7.21fF

For NMOS: $C_{ov}$= 8.06fF

The junction to body capacitance is given by $C_{jb} = \frac{W*D}{VDD}\int_0^{VDD} \frac{C_{J0}}{(1+Vj/Vb)^{mj}}$dVj (10)

For PMOS: $C_{jb}$ = 0.0896fF

For NMOS: $C_{jb}$ = 0.0902fF

Sidewall capacitance For PMOS: $C_{jsw}$ = 0.219fF

For NMOS: $C_{jsw}$ = 0.235fF

Total Capacitance Cl = $C_{in} + C_{ov} + C_{jb} + C_{jsw}$ (11)

= 17.877fF

Dynamic Power for quaternary inverter is given by

$P_{dyn}$ = Cl* $VDD^2$ *f (12)

=2.896nW

## 4. RESULT AND CONCLUSION

The proposed circuit get Extracted by using cadence tool 0.18um technology and the simulation result are as follows,

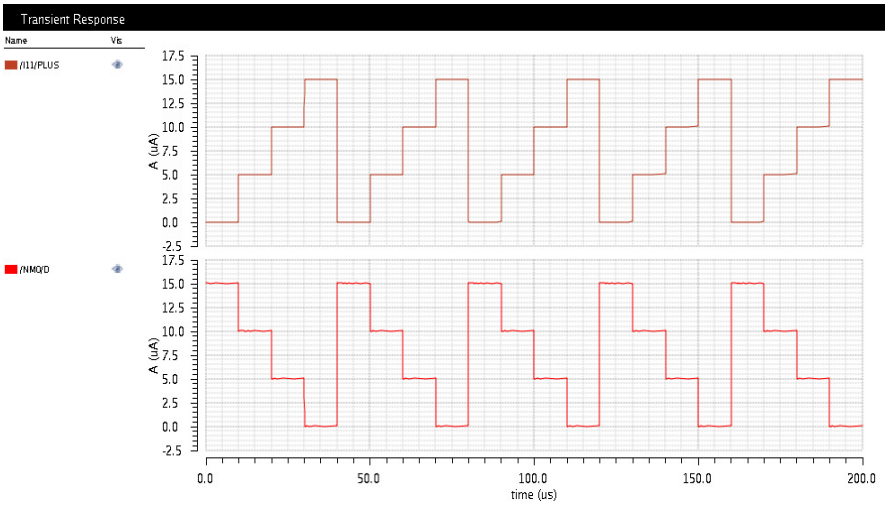


Figure 11. Extraction of Inverter circuit

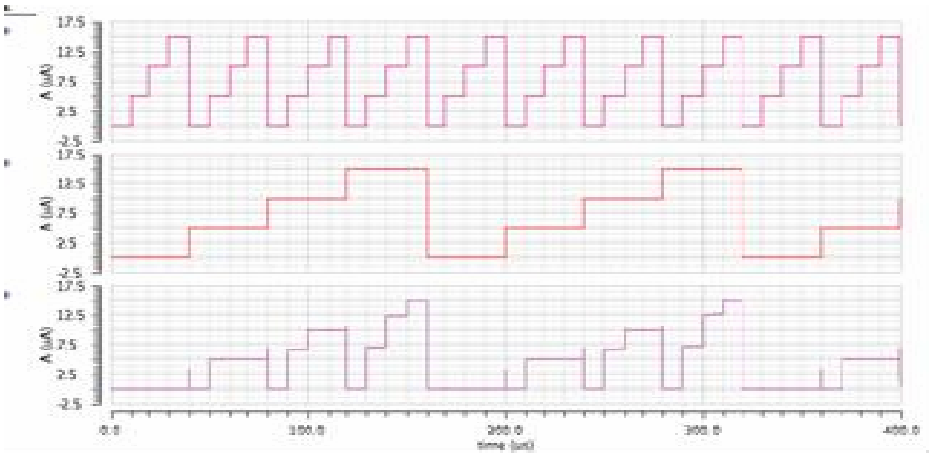

Figure 12. Extraction of min gate circuit

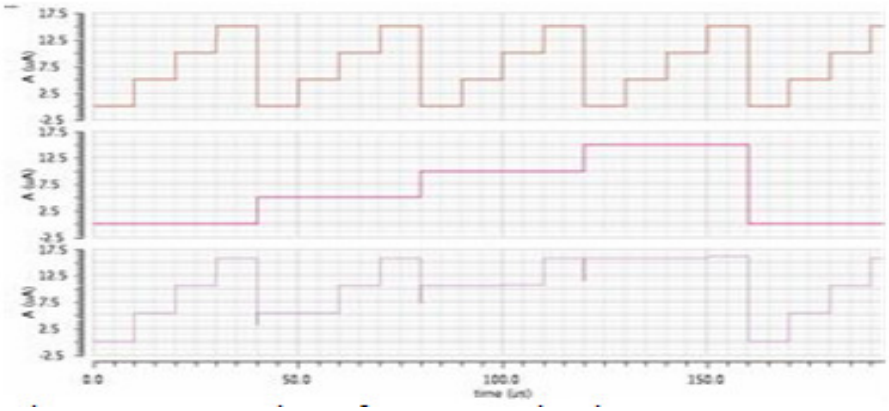

Figure 13. Extraction of max gate circuit

Table 6. Analysis of Average Power Dissipation for Quaternary voltage mode circuit

| Circuit type | Binary[10] | Quaternary |
|---|---|---|
| Inverter | 0.1nw | 27.1pw |
| Min | 38.9uw | 2.1uw |
| Max | 67.1uw | 0.4uw |
| Nmin | 11.5nw | 0.1nw |
| Nmax | 67.1uw | 0.28uw |

Table 7. Analysis of Area for Quaternary voltage mode circuit

| Circuit Type | Binary (Transistor count)[10] | Quaternary(Transistor count) |
|---|---|---|
| Inverter | 2 | 6 |
| Min | 6 | 18 |
| Max | 6 | 18 |
| Nmin | 4 | 12 |
| Nmax | 4 | 12 |

Table 8. Analysis of Area for Quaternary current mode circuit

| Gates | Area(Trans. count) | | |
|---|---|---|---|
| | Conventional[7] | Proposed | Binary |
| Min | 7[7] | 4 | 6 |
| Max | 8 [7] | 8 | 6 |

Table 9. Analysis of Average Power Dissipation for Quaternary current mode circuit

| Gates | Av. Power diss.(mW) | | |
|---|---|---|---|
| | Conventional[7] | Proposed | Binary |
| Min | 0.23 | 0.02 | 0.03 |
| Max | 0.29 | 0.03 | 0.06 |

Comparative analysis of binary, quaternary voltage mode circuit is done based on power consumption and no of transistor. Power consumption required for quaternary voltage mode logic is 51.78 % less as compared to binary as shown in Table 6 . Area in terms of number of transistor required for quaternary voltage mode logic is 3 times more as compared to binary as shown in Table 7. Comparative analysis of quaternary current mode proposed and conventional and binary circuit is done based on power consumption and area. Area required for proposed quaternary current mode circuit is less as compared to conventional and binary circuit as shown in Table 8. Power consumption required for proposed quaternary current mode circuit is less as compared to conventional and binary circuit. As quaternary voltage mode circuit required large area as compared to quaternary current mode circuit but power consumption required in quaternary voltage mode circuit is less than that required in quaternary current mode circuit.

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## AUTHORS

**Yashika Gaidhani** received M. Tech degree in Electronics Engineering from RTMNUNagpur in 2008. Currently she is pursuing PhD from RTMNU Nagpur. She is presently working as Assistant Professor in Electronics Engineering in Yeshwantrao Chavan college of Engg, Nagpur ,India. Her areas of interest is VLSI Design. She is a lifetime member of ISTE . She is having total 11 years of teaching experience .

**Pravin Dakhole** was born in India. He received M. Tech degree in Electronics Engineering from VNIT, Nagpur in 1999 and the Ph. D degree from Sant Gadge BabaAmravati University, Amravati in 2010. He is presently working as Professor in Electronics Engineering & Registrar in Yeshwantrao Chavan college of Engg, Nagpur ,India . His areas of interest are front end & back end VLSI Design. He is trainer to corporate / industries in the field of Verification of HDL based design. Heis recipient of Best paper Award & Best Teacher Award. Currently he is Senate member at RTM Nagpur University. He is a senior Fellow member of IEEE. He is having total 25 years of teaching experience with two years industrial experience. He is having More than 50 research paper publication.