FIVE-TRANSISTOR SINGLE-PORT SRAM BIT CELL WITH HIGH SPEED AND LOW STANDBY CURRENT

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ABSTRACT

In this paper, a new five-transistor (5T) single-port Static Random Access Memory (SRAM) cell with voltage assist is proposed. Amongst them, a word line suppression circuit is designed to provide a voltage of the respective connected word line signal in a selected row cells lower than the power supply voltage V_{DD} by a threshold voltage during a read operation, thereby to improve the read/write-ability of the cell. In addition, a voltage control circuit is coupled to the sources corresponding to driver transistors of each row memory cells. This configuration is aimed to control the source voltages of driver transistors under different operating modes. Specifically, during a read operation, a two-stage reading mechanism is engaged to increase the reading speed. Simulation results for the proposed cell design confirm that there is a conspicuous improvement in reading speed and power saving over the conventional SRAM cells, and fast writing also can be achieved.

KEYWORDS

Single-port, Static random access memory, Assist circuitry, Voltage control circuit, Standby start-up circuit

1. INTRODUCTION

Semiconductor memories can be characterized as volatile random access memories (RAMs) or non-volatile read only memories (ROMs), where RAMs can either be static (SRAM) or dynamic (DRAM) differing mainly in the manner by which they store a state of a bit. In applications of large-scale semiconductor integrated circuits (LSIs), static random access memories (SRAMs) are the widely-used on-chip memories. Typically, SRAM circuits may be single-port or multi-port. In the single-port SRAM, normally, either of read and write operation is performed in one access from one port circuit connected to a pair of bit lines to one memory cell. SRAM is arranged as a matrix of thousands of individual memory cells fabricated in an integrated circuit chip, and address decoding in the chip allows access to each cell for read/write functions. In SRAMs, each memory cell includes transistor-based circuitry that implements a bi-stable latch, which can only assume one of two possible states, namely on (state 1) or off (state 2). The latch can only be induced to change from one state to the other through the application of a voltage or other external stimuli. However, for stabilization of an operation of the conventional six-transistor (6T) SRAM, the current driving capability ratio between the driver and access transistors should be maintained at 2 to 3 or more, and the driver transistor should be designed to have a large gate width, which also causes an increase in size of the memory cell of the SRAM. As such, higher integration and larger capacity cannot be expected with a conventional 6T SRAM. Furthermore, it is apparent that the conventional 6T SRAM suffers from the disadvantage of relying on too many

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transistors. Accordingly, there is an important need to have an SRAM cell that requires fewer than six transistors.

An SRAM cell has three modes of operation, namely read, write and standby [1]. SRAM cells use a write operation to store data in the cell and a read operation to sense the data stored in the cell. In order to perform a write operation, a signal is asserted on word line WL. That is, the voltage on word line WL will go high. This activates the access transistors MA1 and MA2. Under this state, one of the bit lines BL and BLB is driven to the logic low level while the other to the logic high level depending on the data (logical '0' or logical '1') to be written. As a result, the data is written to the cross-coupled inverters. Furthermore, to perform a read operation, the voltage level of the word line WL is raised to the logic high level, activating the transistors MA1 and MA2. This results in producing a voltage level difference between the bit lines BL and BLB depending on the data held in the cross-coupled inverters. This voltage level difference is amplified by a sense amplifier (not shown) so as to read the data. At the end of the read and write operations, the word line voltage is de-asserted to ground allowing the cross-coupled inverters to function normally and hold the logic state of the storage nodes.

In recent years, there has been an increasingly growing trend towards portable devices, which increases a demand for lower power consumption of a large-scale semiconductor integrated circuit (LSI). Leakage current from a memory cell can cause unnecessary power consumption, especially during a standby mode [2-3]. As CMOS technology scales down to 65 nm and below, the power consumption caused by leakage currents is becoming a significant part of the global power consumption [4-5]. Recent researches have shown that the leakage current will become even greater than the dynamic current in the overall power consumption [6-8]. Typically, there are three major sources of leakage in a MOS transistor, namely subthreshold leakage, gate leakage, and reverse bias junction leakage [9-10]. Amongst them, Gate-Induced drain leakage (GIDL) is an unwanted short-channel effect that occurs at higher drain biases in an overdriven off state of a MOS transistor. The GIDL is the result of a deep depletion region that forms in the drain at high drain-to-gate biases. However, Drain-induced barrier lowering (DIBL) is a short-channel effect in MOS transistors referring originally to a reduction of threshold voltage of the transistor at higher drain voltages [11]. With scaling down of the MOS transistor, each of the leakage sources may increase accordingly, thus resulting in the increase of the total leakage current. Therefore, it would clearly be desirable to provide a design for an SRAM cell that has less leakage current than conventional designs when the cell in standby.

The remainder of this paper is organized as follows. Section 2 presents a brief description of conventional 6T and 5T SRAM cell topologies. The proposed 5T SRAM cell with integrated read/write assist is described in Section 3. The simulation results of the proposed 5T SRAM cell are discussed in Section 4. Last section is a conclusion and summary for the paper.

2. CONVENTIONAL 6T AND 5T SRAM CELL TOPOLOGIES

2.1 CONVENTIONAL 6T SRAM CELL

The conventional 6T SRAM cell is formed by a cross-coupled inverters (INV-1 and INV-2) and two access transistors (MA1 and MA2), connecting the cell to the bit lines (BL and BLB), as shown in Fig. 1 [12]. The cross-coupled inverters of the conventional 6T SRAM cell have two stable states functioning to store either a logical '0' or a logical '1'. The reading and writing operations are achieved through the bit line BL and complementary bit line BLB of the memory cell of Fig. 1. Transistors MP1 and MN1 are serially connected between power supply voltage V_{DD} and ground to form a first inverter INV-1 with a storage node A between the two transistors, and, in a similar manner, transistors MP2 and MN2 are likewise connected between V_{DD} and

ground to form a second inverter INV-2 with a storage node B. The gates of transistors of each inverter are connected together and cross-coupled to the storage node of the other inverter. The access transistors MA1 and MA2 are used to selectively couple or decouple the storage nodes (A and B) from the corresponding bit lines. The gates of the access transistors MA1 and MA2 are connected to respective word lines WL. The voltage on word line WL is delivered to the gates of transistors MA1 and MA2 to control whether these transistors are switched on or off, thereby coupling or decoupling the storage nodes from the bit lines.

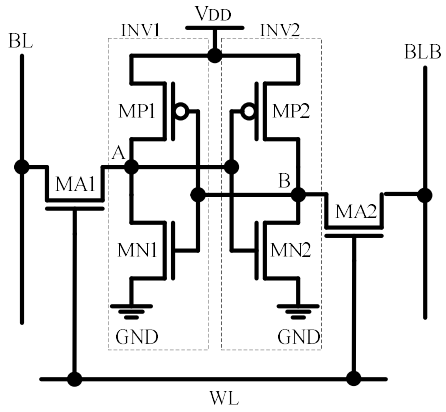

Figure 1. Circuit diagram of conventional 6T SRAM cell.

It is important to note that, in write operation, complementary bit line BLB is pulled to zero using write driver (not shown), while word line WL is asserted. Therefore, the access transistor MA2 is turned on, which results in a voltage drop in the node B holding '1'. When this voltage falls below V_{DD}-$V_{T(MP1)}$, transistor MP1 starts the feedback action, wherein $V_{T(MP1)}$ is the threshold voltage of transistor MP1. For stable write operation, transistor MA2 should be stronger than transistor MP2. In read operation, read disturb may occur after the word line WL is asserted. The voltage at the node A storing a '0' slightly rises due to the voltage divider between the access transistor MA1 and the driver MN1. If the voltage at node A rises above the threshold voltage of transistor MN2, the cell may flip its state. In this case, stable read operation requires that MN1 should be stronger than MA1. Read stability failure increases with process variations, which affect all the transistors in the cell.

It should be noted that since the conventional 6T SRAM circuit needs two bit lines which individually consumes electric power, the power consumption required for the entire memory array becomes large [13]. In general, in order to ensure the stable operation of the memory cell circuit, the voltage level of the bit lines is pulled to a level near the power supply voltage V_{DD} before the start of read/write operations. This allows current to flow through the bit lines BL and BLB, as such increases the power consumption. And thus, more power is consumed by the memory cell circuit using two bit lines. Moreover, according to the memory cell circuit, current always flows through one of the bit lines BL and BLB during the read operation whichever data is held in the cross-coupled inverters. This also causes an increase in the power consumption [14].

2.2 CONVENTIONAL 5T SRAM CELL

Figure 2 is a circuit diagram of a conventional 5T SRAM cell [2]. As shown in Fig. 2, the access transistor MA2 and bit line BLB in Fig. 1 have been removed to make up a five-transistor configuration. The removal of such access transistor allows for an area savings up to 20-30% compared to the conventional 6T SRAM cell, while its power consumption is substantially

reduced by one half [15]. Although the conventional 5T SRAM cells offer such significant reduction in power consumption, a critical drawback is shown that in SRAM cells configured with single-ended bit line, whenever a write operation is performed, a write failure may occur [16-17]. In particular, it is relatively difficult to write a logical '1' to a cell if the cell currently stores a logical '0'. This is because when the bit line BL is logic high and the word line WL is asserted, the transistors MA1 and MN1 fight one another. It is thus necessary to provide a method of resolving write failures in five-transistor (5T) SRAM cells.

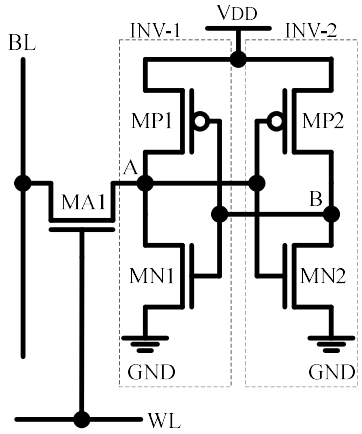

Figure 2. Circuit diagram of conventional 5T SRAM cell.

In order to resolve write '1' issue of 5T SRAM cells, several techniques have been developed. For example, boosting word line gate voltage [18-21], reducing the supply voltage V_{DD} [4], [15], [22-26], sizing cell transistors [15], [27-28], reduced bit line voltage [29-30], and raising the source voltage V_{SS} [31-34]. However, each of these techniques may cause a reduction in the drive current of the transistors and in the operating speed of the cell, or has increased memory cell area and a degradation in the manufacturing accuracy, or requires generation of a voltage above the operating voltage, or requires a more complicated circuit design and more complicated device process [14]. Hence, there is a need for an effective technique to improve the write-ability of 5T SRAM cells which suffer from inability to write '1'.

Another problem with the 5T SRAM cells is that the data stored in the cells may be corrupted when the cells are read [35]. This problem arises from the fact that a higher voltage on the bit line is coupled to a lower voltage in the cell, causing the bit line voltage to drop and the cell voltage to rise. To guarantee a correct write operation will occur, it is important to note that the storage node A must be pulled up (or down) above (or below) the trip-voltage of INV-2 within the word line WL is logic high, otherwise a write failure will occur. In more detail, writing a logical '0' to a cell, when initially storing a logical '1', the high storage node A of the cell has to discharge the bit line BL below the trip-voltage of INV-2. On the contrary, writing a logical '1' to a cell, when initially storing a logical '0', the low storage node A of the cell must be pulled up by the pre-charged bit line BL above the trip-voltage of INV-2. Undoubtedly, to write the wanted bit properly in the cell, it may be necessary that the access transistor should be very conductive to force the cross-coupled inverters to change its equilibrium condition [14]. Accordingly, the SRAM cell should provide more reliable when the cell is written and less likely to be corrupted when the cell is read. However, the access transistor should have a reduced conductivity for good stability in reading and standby operations. These two requirements impose contradicting requirements on cell transistor sizing.

3. THE PROPOSED 5T SRAM CELL

3.1 THE PROPOSED 5T SRAM CELL CONFIGURATION

The proposed 5T SRAM cell with voltage assist circuitries is illustrated in Fig. 3, which is formed by a voltage control circuit, a pre-charging circuit, a standby start-up circuit and a word line suppression circuit. Amongst them, the voltage control circuit is coupled to the sources corresponding to the driver transistors of each row memory cells. This configuration is aimed to control the source voltages of driver transistors under different operating modes. That is, the circuit is employed to control the voltage of nodes L1 and L2 under different operating modes. In the write mode, the voltage of node L1 (hereinafter, V_{L1}) of the selected cell is set to $V_{GS(M23)}$, wherein $V_{GS(M23)}$ is the gate-source voltage of transistor M23, and that of node L2 (hereinafter, V_{L2}) of the selected cell is set to the ground voltage. Thereby, in this manner, it can provide an efficient solution to the writing '1' issue and to improve write operations. In the read mode, a two-stage read mechanism is introduced to speed up the reading speed and thus to avoid unnecessary power consumption. In the first read stage, the voltage V_{L1} is set to a negative voltage RGND to speed-up the reading speed. However, in the second read stage, the voltage V_{L1} is pulled up via transistor MN26 to the ground voltage to reduce power consumption. Under these circumstances, the voltage RGND can effectively improve the reading speed without incurring unnecessary power consumption even in technologies below 10nm. Finally, in the standby mode, the voltage of nodes L1 and L2 are set to $V_{GS(MN23)}$ to reduce the leakage current.

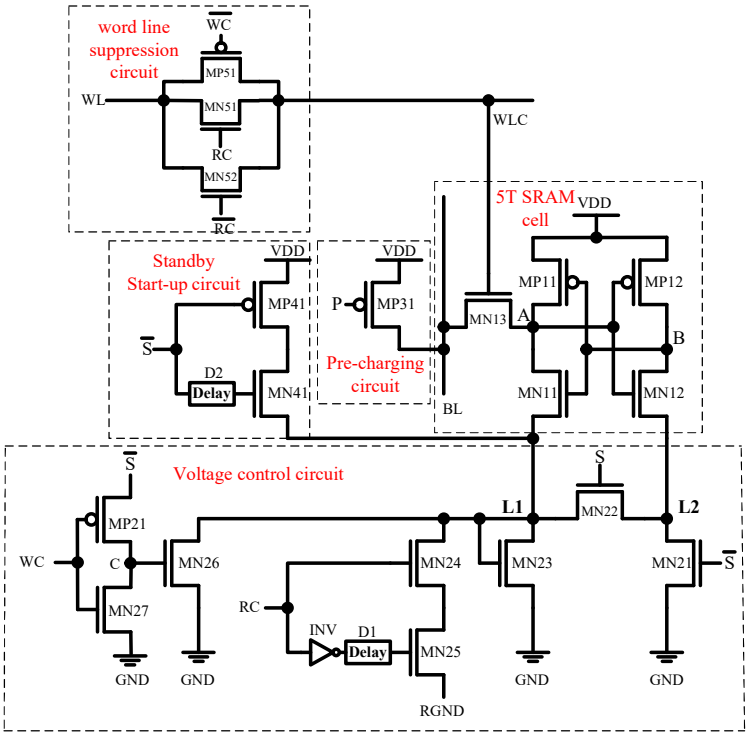

Figure 3. Circuit diagram of the proposed 5T SRAM cell.

Table 1 summaries the operating conditions under different operating modes. In Table 1, the write control signal WC can be achieved by performing the AND operation on the write signal W and its corresponding word line signal WL. Also, the read control signal RC can be achieved by performing the AND operation on the read signal R and its corresponding word line signal WL. It

is worth noting that, in the non-read mode, the voltage of the read control signal RC is set to the voltage RGND to prevent the leakage current caused by the transistor MN24.

Referring to Fig. 3, the pre-charging circuit is connected to the bit line BL in each column. The function of the pre-charging circuit is to pull up the bit line BL of a selected column to power supply voltage V_{DD} before the start of read operation. And also, the standby start-up circuit is to enable the SRAM cell to quickly switch to the standby mode, and thus effectively enhance the standby performance.

Table 1: The operating conditions under different operating modes

RC	WC	S	V_{L1}	V_{L2}	mode
RGND	V_{DD}	0	$V_{GS(MN23)}$	0	write
V_{DD}	0	0	RGND (1st stage) 0 (2nd stage)	0	read
RGND	0	V_{DD}	$V_{GS(MN23)}$	$V_{GS(MN23)}$	standby
RGND	0	0	0	0	hold

Referring again to Fig. 3, the word line suppression circuit is to provide a voltage of the selected word line when the respective word lines are in an active state. Unlike the conventional 5T SRAM cell in Fig. 2, a voltage V_{DD}-$V_{T(MN51)}$ is applied to the word line control signal WLC of the selected row cells so as to improve the cell read/write-ability, wherein $V_{T(MN51)}$ is the threshold voltage of transistor MN51. In more detail, the word line suppression circuit weakens the access transistor MN13 such that the voltage drop across the transistor MN13 increases and the voltage drop between the transistor MN13 and the driver transistor MN11 reduces, thereby increasing the read-ability. It is worth noting that the word line control signal WLC of the selected cell is provided a voltage V_{DD}-$V_{T(MN51)}$ during a read operation, however, the power supply voltage V_{DD} is provided during a write operation. In general, for a given cell size, a higher beta ratio improves cell stability at the expense of lower access speed [17]. Lowering the word line voltage has the effect of increasing the beta ratio.

In this suppression circuit, the read signal RC and the inverse write signal $\overline{WC}$ can be achieved from the memory read/write control pin. When the signal RC is at logic high, it indicates that the cell is in a read operation, and however the inverse write signal $\overline{WC}$ is at logic low indicates a write operation. The voltage level of the signal WLCs under different operating modes is shown in Table 2.

Table 2: Voltage level of the signal WLC under different operating modes

cells	WL	RC	$\overline{WC}$	$\overline{RC}$	WLC	mode
selected row cells	V_{DD}	V_{DD}	V_{DD}	0	V_{DD}-$V_{T(MN51)}$	read
non-selected row cells	0	V_{DD}	V_{DD}	0	0	read
selected row cells	V_{DD}	0	0	V_{DD}	V_{DD}	write
non-selected row cells	0	0	0	V_{DD}	0	write
each cell	0	0	V_{DD}	V_{DD}	0	non-access

It is worth noting that the paper introducing a two-stage reading mechanism to improve the reading speed, as well as to avoid unnecessary power consumption. Furthermore, by using the voltage word line suppression circuit to pull the voltage of the signal WLC in a selected row cells

down to V_{DD}-$V_{T(MN51)}$ during a read operation, thereby to reduce the half-selected cells disturbance. If the write control signal WC is at logic low, the voltage of node C (hereinafter, V_C) will be equal to that of the inverse standby control signal $\bar{S}$. On the contrary, when the write control signal WC is at logic high, voltage V_C is the ground voltage. This allows stable write operations. Furthermore, during the initial period in standby, the standby start-up circuit is designed to rapidly charge the parasitic capacitance of node L1 to the voltage $V_{T(MN23)}$.

3.2 WRITE OPERATION

Refer to Fig. 3, before and during the write operation is performed, the standby start-up control signal S is at logic low, thereby transistor MN26 is turned on, as such the voltage V_{L1} is pulled down to ground. During the writing '0' operation, the voltage of bit line BL (hereinafter, V_{BL}) is pulled down to logic low and the asserted word line WL turns on transistor MN13. Thus, node A is at logic low and node B is at logic high. Conversely, during the writing '1' operation, the voltage V_{BL} is pulled up to logic high and the asserted word line WL turns on transistor MN13. Thus, node A is at logic high and node B is at logic low. In more detail, prior to the write operation is performed, the write control signal WC is at logic low, transistor MP21 is turned on and transistor MN27 is turned off. Thereby, the voltage V_C is at logic high and thus to turn on transistor MN26, as such the voltage V_{L1} is pulled down to the ground voltage. However, during the write operation, the signal WC is at logic high, transistors MP21 is turned off and transistor MN27 is turned on. Subsequently, the voltage V_C is at logic low and thus to turn off transistor MN26, as such the voltage V_{L1} is set to $V_{GS(MN23)}$. Thus, the issue concerning the difficulty of writing '1' can be resolved. Figure 4 shows the simplified circuit diagram during the write operation.

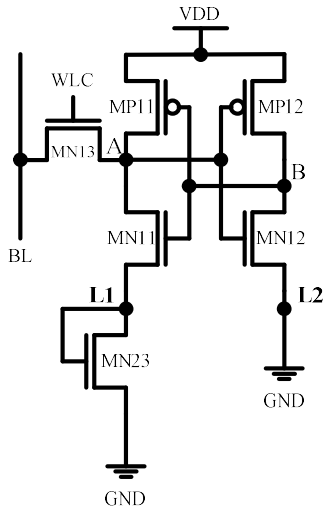

Figure 4. Simplified circuit diagram during the write operation

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The transients associated with a writing operation are detailed described below. Firstly, let us consider the writing '0' operation. Prior to the writing '0' operation, the voltage V_{BL} and that of signal WLC are at logic low. During the writing '0' operation, if a logical '0' is stored previously, the signal WLC transitions from a logic low to a logic high. As the signal WLC exceeds the threshold voltage of transistor MN13 (hereinafter, $V_{T(MN13)}$), transistor MN13 is turned on. Subsequently, owing to the fact voltage V_{BL} is at logic low, the voltage of storage node A (hereinafter, V_A) remains at the ground voltage. On the other hand, if a logical '1' is stored previously, the signal WLC transitions from a logic low to a logic high. As the signal WLC exceeds the threshold voltage $V_{T(MN13)}$, transistor MN13 is turned on. Subsequently, owing to the

fact voltage V_{BL} is at logic low, node A and node L1 will be discharged to ground until the end of the writing '0' operation.

Secondly, consider the writing '1' operation. Prior to the writing '1' operation, the signal WLC is at logic low and the voltage V_{BL} is at logic high. During the writing '1' operation, if a logical '1' is stored previously, the signal WLC transitions from a logic low to a logic high. When the signal WLC exceeds the threshold voltage $V_{T(MN13)}$, transistor MN13 is turned on. Subsequently, owing to the fact voltage V_{BL} is at logic high and transistor MP11 remains on, the voltage V_A will remain at the power supply voltage V_{DD} until the end of the writing '1' operation. On the other hand, if a logical '0' is stored previously, the signal WLC transitions from a logic low to a logic high. Subsequently, with the increase of signal WLC, the voltage V_A will rise. As the signal WLC exceeds the threshold voltage $V_{T(MN13)}$, transistor MN13 is turned on. Subsequently, owing to the voltage V_{BL} is at logic high and transistor MN11 remains on, and the voltage V_B remains at a voltage close to the power supply voltage V_{DD}, transistor MP11 remains off. For a successful write operation, it is desirable to pulling down the voltage V_A (or V_B) which has a stored value '1' below the trip-voltage of the inverter. Meanwhile, the write initial transient voltage V_{AW} of node A must satisfy the following equation:

$$V_{AW} = V_{DD} \times \frac{R_{MN11} + R_{MN23}}{R_{MN11} + R_{MN13} + R_{MN23}} > V_{T(MN12)} \quad (1)$$

wherein $V_{T(MN12)}$ is the threshold voltage of the transistor MN12, R_{MN11}, R_{MN13} and R_{MN23} are the on-resistance of transistors MN11, MN13 and MN23, respectively. Consequently, the writing '1' problem associated with the conventional 5T SRAM cell can be avoided. Now, transistor MN13 is still in the saturation region and transistor MN11 in the triode region. Although R_{MN13} may be greater than R_{MN11}, the NMOS diode MN23 can provide a voltage $V_{GS(MN23)}$ at node L1. As a result, the voltage V_A will rise up due to the voltage division along the driver and access transistors. When the voltage exceeds a threshold, it causes the bit cell to flip due to regenerative feedback. Hence, the writing '1' operation is completed. Consequently, the writing '1' problem associated with the conventional 5T SRAM cell can be resolved. It is worth noting that the voltage V_{L1} is $V_{GS(MN23)}$ when writing a logical '1' to a logical '0' is stored. After completing the writing '1' operation, the voltage V_{L1} will be discharged to ground via transistor MN26. It is worth noting that the W/L ratio of transistor MN11 in Fig. 3 is designed smaller than that of transistor MN1 shown in Fig. 1. Consequently, the writing '1' problem associated with the conventional 5T SRAM cell can be resolved.

3.3 READ OPERATION

As mentioned above, in the read operation, a two-stage reading mechanism is introduced to increase the reading speed and thus to avoid unnecessary power consumption. Prior to a read operation is performed, bit line BL is pre-charged to the power supply voltage V_{DD}. Meanwhile, the standby start-up control signal S, the write control signal WC and the read control signal RC are at logic low, thereby transistors MP21 and MN25 are turned on and transistors MN24 and MN27 are turned off, as such the voltage V_C is at logic high and subsequently turn on the transistor MN26. This leads to the voltage V_{L1} will be pulled down to ground. Figure 5 shows the simplified circuit diagram during the read operation.

In the first reading stage, the read control signal RC is at logic high, thereby transistor MN24 is turned on. At this time, since transistor MN25 would continue to conduct, the voltage V_{L1} will be pulled down to a negative voltage RGND. Under this circumstance, the negative voltage RGND can effectively improve the reading speed. Furthermore, in the second reading stage, the read control signal RC remains at logic high and transistor MN24 remains on. Consequently, the

voltage V_{L1} is pulled up to the ground voltage due to transistor MN25 is turned off, and thus leads to reduce unnecessary power consumption. It is note that the two-stage time interval is measured as the time taken from a logic high on the read control signal RC to transistor MN25 is turned off. This time interval can be adjusted by the falling time of the inverter INV and the delay time of the delay circuit D1. In addition, during the two-stage read operation transistor MN26 is always on.

The transients associated with a reading operation are detailed described below. Firstly, before the reading '1' operation, transistor MN11 is off and transistor MN12 is on, the voltages V_A and V_B are at V_{DD} voltage level and the ground voltage, respectively. The voltage V_{BL} is equal to the power supply voltage V_{DD} due to the pre-charging circuit. During the read operation, since the voltage V_{WLC} is at V_{DD}-V_{TMN51} voltage level, transistor MN13 is on. Thereby the voltage V_{BL} can be effectively kept at V_{DD} until the end of the reading '1' operation. It is worth noting that, in the first stage, the voltage V_{L1} can be expressed as:

$$V_{L1} = RGND \times \frac{R_{MN26}}{R_{MN24} + R_{MN25} + R_{MN26}} \tag{2}$$

wherein RGND is the acceleration read voltage (RGND) which is a negative voltage, R_{MN24}, R_{MN25} and R_{MN26} are the on-resistance of transistors MN24, MN25 and MN26, respectively. While, in the second stage, the voltage V_{L1} can be expressed as:

$$V_{L1} = GND \tag{3}$$

As a result, the unnecessary power consumption can be reduced effectively. Furthermore, in order to effectively reduce the half-selected cell disturbance and the leakage current during the reading '1' operation, the absolute value of the voltage RGND may be set to be lower than the voltage $V_{T(MN11)}$ in reading '1', i.e.,

$$|RGND| < V_{T(MN11)} \tag{4}$$

Wherein, |RGND| denotes the absolute value of the voltage RGND and $V_{T(MN11)}$ is the threshold voltage of transistor MN11.

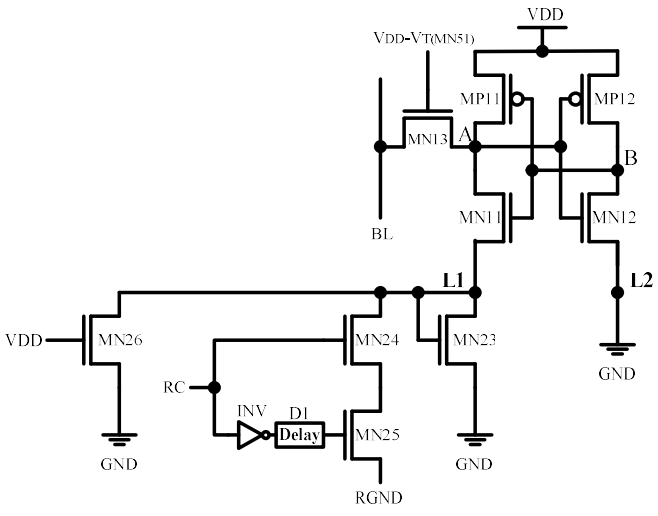


Figure 5. Simplified circuit diagram during the read operation.

Secondly, consider the reading '0' operation. Before the read '0' operation is performed, transistor MN11 is on and transistor MN12 is off, voltage V_A and voltage V_B are ground and V_{DD}, respectively. And also, the voltage V_{BL} is equal to V_{DD} due to the pre-charging circuit. During the reading '0' operation, since the voltage V_{WLC} is at V_{DD}-$V_{T(MN51)}$ voltage level, transistor MN13 is turned on. Meanwhile, the initial transient voltage V_{AR} of node A must satisfy the following equation:

$$V_{AR} = V_{DD} \times \frac{R_{MN11} + (R_{MN24} + R_{MN25}) \,||\, R_{MN26}}{R_{MN13} + R_{MN11} + (R_{MN24} + R_{MN25}) \,||\, R_{MN26}} + RGND \times \frac{(R_{MN11} + R_{MN13}) \,||\, R_{MN26}}{R_{MN24} + R_{MN25} + (R_{MN11} + R_{MN13}) \,||\, R_{MN26}} \times \frac{R_{MN13}}{R_{MN11} + R_{MN13}} < V_{T(MN12)} \quad (5)$$

Where in, V_{AR} is the initial transient voltage of node A, V_{TMN12} is the threshold voltage of transistor MN12, R_{MN11}, R_{MN13}, R_{MN24}, R_{MN25} and R_{MN26} are the on-resistance of transistors MN11, MN13, MN24, MN25 and MN26, respectively. It is worth noting that, the voltage RGND is designed to be lower than the ground voltage and its absolute value is designed to be lower than the voltage $V_{T(MN11)}$. Furthermore, during the read '0' operation, the voltage V_{WLC} is set to a V_{DD}-$V_{T(MN51)}$ voltage level, as such the on-resistance of transistor MN13 can be increased to satisfy the equation (5) and can reduce the half-selected cell disturbance in reading '0' operation.

3.4. STANDBY OPERATION

Refer again to Fig. 3, prior to the standby operation is performed, the standby control signal S is at logic low, and thus, transistor MP41 is turned off and transistor MN41 is turned on. While during the standby operation, since the control signal S is at logic high, transistor MP41 is turned on and transistor MN21 is turned off. In addition, the logic high signal S is also to turn on transistor MN22 which acts as an equalizer. Consequently, with the conduction of transistor MN22, both the V_{L1} and V_{L2} are equal to the threshold voltage of transistor MN23 ($V_{T(MN23)}$). It is worth mentioning that node L1 can be rapidly charged to $V_{T(MN23)}$ at the initial period of the standby mode due to transistor MN41 remains on, and thereby improving the standby efficiency. Note that the initial period is determined as the time taken from a logic high on the signal S to the state of transistor MN41 is turned off. This time interval can be adjusted by the delay time of delay circuit D2. It is worth noting that after the initial period of the standby mode, transistor MN41 is turned off and no current flows. Figure 6 shows the simplified schematic of the proposed design during the standby mode.

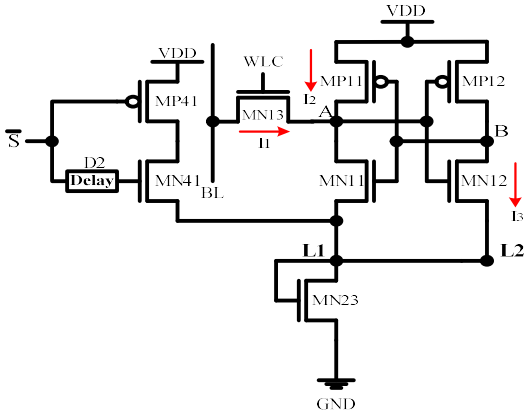
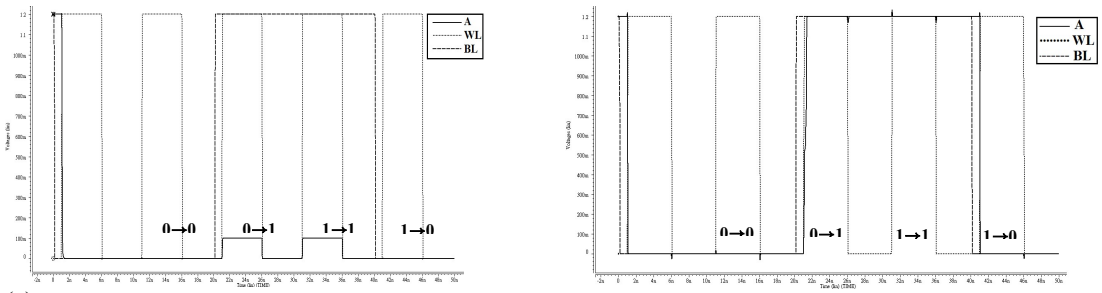


Figure 6. Simplified circuit diagram during the standby operation.

4. SIMULATION RESULTS

To evaluate performance, different SRAM cell structures discussed in this paper were simulated using a 90nm CMOS technology. All simulations were carried out at nominal conditions: V_{DD}=1.2V and at room temperature. In conventional 5T SRAM cell shown in Fig. 2, access transistor MA1 is less conductive than driver transistor MN1, thereby making it more difficult to write a logical '1' to cell over a logical '0' stored. Figure 7(a) shows the simulated waveform of a writing '1' failure. It is worth noting that sizing of MN11 should ensure that inverter INV-2 does not switch causing a destructive read.

To elucidate the improvement in writing '1' issue, suppose that node A stores '0' and it needs to change to '1' during a write cycle. Before the write operation is performed, both transistors MP11 and MN12 are off and both transistors MP12 and MN11 are on. When the writing '1' is performed, if the voltage of word line WL (V_{WL}) exceeding the threshold voltage of transistor MN13 ($V_{T(MN13)}$), transistor MN13 will be turned on. Upon write operation, voltage V_{BL} remains at the pre-charge level as such transistor MN11 remains on and transistor MP11 off. Effectively, transistors MN11 and MN13 make up a voltage divider and have been connected to the input of INV-2, whose output is now no longer at zero. Meanwhile, node A can be charged toward $V_{DD} \times (R_{MN11} / (R_{MN11} + R_{MN13}))$, where R_{MN11} is the on-resistance of transistor MN11, and R_{MN13} is the on-resistance of transistor MN13, respectively. Traditionally, since the W/L ratio of transistor MN11 is designed smaller than that of transistor MN1 shown in Fig. 1, there will be no destructive reading occurs. In addition, it enables the voltage of node A (V_A) higher than the threshold voltage of transistor MN12 ($V_{T(MN12)}$). Consequently, transistor MN12 is on and node B is discharged to a lower voltage level. And then, the voltage V_A rises since transistor MN11 is now possess higher resistance value. This higher resistance value helps pulling up node A toward much higher voltage level. Hereafter, by using of INV-2, this much higher voltage V_A will pull node B down to much lower voltage level. Furthermore, by using of INV-1, this much lower voltage level on node B will pull V_A up to much higher voltage. In this way, such operations are alternately repeated until V_A reaches V_{DD}. Hence, the writing '1' operation of the proposed cell is accomplished. The simulated waveform of a successful writing in the proposed 5T SRAM cell is shown in Fig. 7(b). It is evident that the proposed 5T SRAM cell provides an efficient solution to the writing '1' issue, that is, the proposed 5T SRAM cell enabling a logical '1' to be easily written to the SRAM cell, as compared to the conventional 5T SRAM cells.



(a) (b)

Figure 7. (a) Transient waveforms of a write failure in the conventional 5T SRAM cell, (b) Transient waveforms of a successful writing in the proposed 5T SRAM cell.

Upon read operation, due to a two-stage reading mechanism is introduced to improve the reading speed as well as to avoid unnecessary power consumption. During the first stage of the read operation, the voltage V_{L1} is set to the acceleration read voltage RGND which is lower than the ground voltage, as shown in Fig. 8. As such to effectively increase the reading speed, and the voltage V_{L2} is set to the ground voltage. In the second stage, the voltages V_{L1} and V_{L2} are set to

the ground voltage to reduce unnecessary power consumption. Table 3 shows the reading speed for the proposed design and the conventional 6T SRAM cell in different corner models. An advantage of the proposed design over the conventional 5T SRAM cell is that it is unnecessary to boost the word line signal above V_{DD} to speed up the read operation. Furthermore, this design has the additional advantage of increased current through the driver transistor during a read operation, and consequently lower read delay.

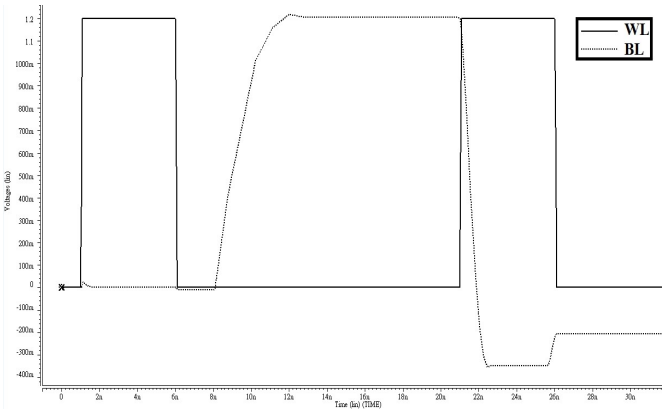


Figure 8. Signal waveforms during a read operation.

Table 3. Reading speed comparisons

Corner model	Conventional 6T SRAM (ns)	Proposed 5T SRAM (ns)	Improvement (%)
TT	0.1205	0.0748	37.9
SS	0.1548	0.1052	32.0
FF	0.1985	0.132	33.5

It can be seen from Table 3, compared with the conventional 6T SRAM cell in different corner models, the reading speed of the proposed design is significantly speed-up to 37.9%, 32.0% and 33.5%, respectively.

Finally, upon standby mode shown in Fig. 6, the voltage V_A remains at $V_{T(MN23)}$, the voltage V_{WL} is set to the ground voltage and the voltage V_{BL} is set to V_{DD}, respectively. Therefore, the gate-source voltage V_{GS} of transistor MN13 is negative. In contrast, the voltage V_{GS} of transistor MA1 in Fig. 1 is equal to zero. For NMOS transistors, according to the GIDL effect, the sub-threshold current at V_{GS}=-0.1 is approximately 1% of that at V_{GS}=0. Accordingly, the leakage current I1 flows through transistor MN13 caused by the GIDL effect is much smaller than that of flowing through transistor MA1 in Fig. 1. Furthermore, the drain-source voltage V_{DS} of transistor MN13 is V_{DD}-V_{TMN23}, whereas the voltage V_{DS} of transistor MA1 in Fig. 1 is V_{DD}. According to the DIBL effect, the leakage current I1 flowing through transistor MN13 is also less than that of flowing through transistor MA1 in Fig. 1. As a result, the leakage current flows through transistor MN13 is much smaller than that flowing through transistor MA1 in Fig. 1. Next, the source-drain voltage V_{SD} of transistor MP11 is V_{DD}-V_{TMN23} in contrast to the V_{SD} = V_{DD} of transistor MP1 in Fig. 1. According to the DIBL effect, the leakage current I2 flowing through transistor MP11 will be less than that of flowing through transistor MP1 in Fig 1. Thus, the base-source voltage V_{BS} of transistor MN12 is negative, and the drain-source voltage V_{DS} of transistor MN12 is V_{DD}-V_{TMN23}. On the contrary, the V_{BS} of transistor MN2 in Fig. 1 is zero, and the V_{DS} of transistor MN2 is V_{DD}. According to the body effect and DIBL effect, the leakage current I3 flows through

transistor MN12 is much smaller than that of flowing through transistor MN2. From the above analysis, it can be seen that the proposed 5T single-port SRAM having a lower leakage current compared with the conventional 6T SRAM. Table 4 shows the standby leakage current for the proposed design and the conventional 6T SRAM cell in different corner models.

Table 4. Leakage current comparisons

Corner model	Proposed 5T SRAM (pA)	Conventional 6T SRAM (pA)	Improvement (%)
TT	2.0536	22.2203	90.8
SS	1.0587	1.6191	34.6
FF	38.3415	309.2402	87.6

As it can be seen from Table 4, compared with the conventional 6T SRAM cell in different corner models, the standby leakage current of the proposed design is significantly reduced 90.8%, 34.6% and 87.6%, respectively.

5. CONCLUSIONS

In this paper, a new 5T single-port SRAM cell with voltage assist is proposed. Firstly, a word line suppression circuit is designed to provide a gate voltage of access transistor of the selected word line lower than the power supply voltage by a threshold voltage, as such to improve the cell read/write-ability. Furthermore, in order to resolve the writing '1' issue, the voltage V_{L1} of the selected cell is set to a gate-source voltage $V_{GS(M23)}$ and the voltage V_{L2} is set to the ground voltage, and consequently fast writing also can be achieved. In addition, in the read operation, a two-stage read mechanism is introduced to speed up the reading speed and to avoid unnecessary power consumption. To speed-up the reading operation, a voltage control circuit facilitates such a read operation by supplying the SRAM cell with a speed-up reading voltage RGND that is lower than the ground voltage during a first-stage read operation. However, during a second-stage read operation, the voltage V_{L1} is pulled up to the ground voltage to reduce unnecessary power consumption. Finally, in the standby mode, the voltages V_{L1} and V_{L2} are set to a gate-source voltage $V_{GS(MN23)}$ to reduce the leakage current.

An advantage of the proposed design over the conventional SRAM cell is that it is unnecessary to boost the word line signal above the power supply voltage V_{DD} to speed up the read operation. This design has the additional advantage of increased current through the driver transistor during a read operation, and thus decreases read delay. Simulation results for the proposed 5T cell design confirm that there is conspicuous improvement over the conventional 6T SRAM cell while it allows writing '1' on the cell with write assist. In addition, with the proposed voltage assist leads to a 37.9%, 32.0% and 33.5% reading speed-up in different corner compared with the conventional 6T SRAM cell. Finally, with the proposed design leads to a 90.8%, 34.6% and 87.6% less standby leakage in different corner compared with the conventional 6T SRAM cell.

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